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Abstract:

Integrated freestanding single-crystal silicon nanowires with typical dimension of 100 nm × 100 nm × 5 μm are fabricated by conventional 1:1 optical lithography and wet chemical silicon etching. The fabrication procedure can lead to wafer-scale integration of silicon nanowires in arrays. The measured electrical transport characteristics of the silicon nanowires covered with/without SiO_2 support a model of Fermi level pinning near the conduction band. The I–V curves of the nanowires reveal a current carrier polarity reversal depending on Si–SiO_2 and Si–H bonds on the nanowire surfaces.

1. Introduction

Silicon is an attractive material for nanoelectronics and nanoscale devices because the fabrication technology is mature and the electrical properties can be controlled by doping. Si nanowires (SiNWs) have been produced by various techniques [1–10]. Broad applications of SiNWs for nanoelectronic or nanothermoelectronic devices or for physical-property testing systems have been proposed [11–13]. The SiNW devices produced by most of the methods so far use single SiNWs that are separately grown and then electrically connected. Rather laborious techniques have been developed to integrate and test these single-SiNW devices [13–15]. Such serial manufacturing is an obstacle not only to obtaining repeatable and reproducible results, but also to expanding practical applications of nanoscale devices. For applications of SiNWs in nanoelectronic devices, a method is needed to achieve integration of thousands of wires, covering entire wafers, with electrical readouts.

To achieve the promise of Si nanowires for electronic devices it is also essential to understand charge carrier transport. The very large surface-to-volume ratio makes it imperative to explore the possible surface-related mechanisms that influence conductivity, and to have well-defined wire shapes and well-characterized contacts.

In this paper, we show the fabrication of integrated freestanding single-crystal SiNWs with electrical contacts, scalable from a single nanowire (NW) to wafer scale in principle. We present measurements and comparisons of electron transport characteristics of a single, freestanding SiNW with and without an oxide (SiO_2) and a SiNW with oxide but not freestanding. We observe current–voltage behaviors that in important aspects contradict prior work on SiNWs or on Si

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nanomembranes (SiNMs) that are attached to and covered by silicon dioxide. We provide possible reasons for these differences.

2. Fabrication

Our SiNWs are fabricated using silicon-on-insulator (SOI) and are, for the current work, 140 nm thick, 120 nm wide, and 3 μm long, but all of these dimensions are readily adjustable to at least 35 nm thick, 50 nm wide, and from 1 to 5 μm long. Only conventional optical lithography (1:1 pattern transfer) and anisotropic wet chemical etching are used in the fabrication. Using 1:1 optical lithography, we have made 100 × 100 arrays of SiNWs with excellent reproducibility and yield. The SiNWs made by this process from SOI (001) can have their long axis along either the Si (100) or (110) crystallographic directions. The side wall crystallographic orientation of the SiNWs is atomically defined by the anisotropic wet chemical etch of single-crystal Si. Such facet definition should reduce electron scattering caused by irregular boundaries [13, 16].

Other researchers [1, 2, 17] have fabricated SiNWs on bulk silicon wafers using e-beam lithography followed by either anisotropic wet chemical etching or reactive ion etching (RIE). On bulk Si, precise control of the thickness of SiNWs on the nanometer scale is difficult to achieve with either anisotropic wet etching or dry etching. Furthermore, once the SiNWs are fabricated and suspended, an integration of electrical leads is a challenge because of the lack of mechanical strength of the suspended SiNWs. SOI has also recently been used as the starting material for SiNW fabrication [9, 12, 18]. In these experiments, the NWs were formed by direct-write e-beam lithography and RIE, a process that is inherently difficult to scale up, and one that also leaves rough side walls unless an extra anisotropic wet etching step is used [9]. Pennelli et al [19] have fabricated SiNWs from SOI using e-beam lithography and wet chemical etching. They have used thermal oxidation to reduce the SiNW sizes further.

The fabrication of our SiNWs begins with thermal oxidation of a SOI (001) wafer with a 200 nm thick top Si layer. The initial thermal oxidation has two purposes, to thin the top Si layer to the desired thickness of SiNWs, and to serve as an etch mask for defining the lateral dimensions of the SiNWs during anisotropic wet chemical etching. The SiO_2 layer is patterned by optical lithography to define the

SiNWs and electrical contact pads, on which metal layers (e.g., Cr, Al, Pt, W, or metal silicides) will be evaporated at the last step of device fabrication. After defining the SiNWs, a 200 nm thick low-stress silicon nitride film (Si_xN_y) is deposited by low-pressure chemical vapor deposition (LPCVD) over the entire wafer without removing the SiO_2 film. The Si_xN_y film is patterned and removed to expose the SiO_2 on the electrical contact pads only. Finally, the SiO_2 on the contact pads is removed in diluted HF (10%) to expose the underlying Si, upon which metal layers are evaporated. The Si_xN_y film elsewhere serves as a shadow mask for the SiNWs during the metallization for electrical leads. Two SiNW fabrication approaches are shown in figures 1(a)–(d). In the first approach (figure 1(a)), the corners A and B are slightly offset (~0.5 μm) with respect to the (110) direction, resulting in atomically defined SiNW formation when the {111} crystal planes are developed during the anisotropic wet chemical (e.g., 30% KOH) etching (dotted lines). The side wall is 54.7° slanted with respect to the (001) planes, resulting in an isosceles-trapezoid cross-sectional SiNW having two {100} and two {111} faces. Its final width is determined by the offset of points A and B. TheSiO2 is undercut to expose the Si. One can also pattern the SiNWs along (100) as shown in figures 1(c) and (d). This approach gives an atomically defined rectangular-cross-sectional SiNW with {100} side walls. Figures 1(e) and (f) show fabricated SiNWs. At this stage of fabrication, the tops and bottoms of the SiNWs are covered with SiO2 and the SiNW is still attached to the buried oxide (BOX). In later stages, the oxide is removed and the SiNW is made freestanding, connected only at the contacts. Furthermore, the SiNW can be re-oxidized, but remain freestanding, as the BOX has been removed under the SiNW.

3. Measurements of electrical characteristics of individual SiNWs

We have made I–V measurements of individual SiNWs fabricated from p-type, 10^{15} cm^{-3} boron doped Si template layers on SOI (001), as a function of the SiNW surface condition. This doping is low compared to most of the current work on SiNWs. The number of dopants in our SiNW is less than 50, which equals the number of mobile charges at room temperature. I–V curves on 13 devices are measured in this work. All the devices have I–V characteristics similar to those shown in figures 3, 5, 6. At least three I–V curves are

measured on each device to confirm the reproducibility of the I–V characteristics. As mentioned, the individual SiNWs are 140 nm thick, 120 nm wide, and 3 μm long, along the (100) direction, hence with all {100} faces. Figure 2 shows schematic measurement setups for two situations: a SiNW still attached to the BOX (for comparison with prior literature) and a freestanding SiNW that can either be re-oxidized or H-terminated.

Figure 3 shows measurements that correspond to the wire configuration shown in the center panel of figure 2, a SiNW still attached to the BOX covered with SiO_2, i.e., oxide all around. The bias voltage is applied between the SiNW contact pads, and the back-gate voltage is applied on the back of the substrate wafer. While the top and bottom of the SiNW are covered with thermally grown SiO_2 (due to SOI top-layer thinning and BOX below), the side walls of the SiNW are covered with SiO_2 formed by the chemical cleaning of the sample in a mixture of sulfuric acid and hydrogen peroxide. As shown in figure 3 (inset), the electrical conductivity drops when the back-gate voltage (Vbg) increases to positive values, which is a typical p-type SiNW FET operating in accumulation mode: holes as majority carriers [20–22].

Prior electrical transport measurements reported on various semiconductor NWs with effective diameters between 45 and 200 nm show several distinct I–V characteristics that depend on the type of metal–semiconductor (M–S) junction formed at the contacts, which are typical electrical-contact configurations of NWs [23, 24]. The SiNW I–V characteristic in our work is consistent with a metal–semiconductor–metal (M–S–M) junction with two back-to-back Schottky barriers. This conclusion is reasonable because chromium is evaporated on the SiNW contact pads (as shown in figure 2, the same p-type, 10^{15} cm^{-3} boron doped Si), i.e., the work function of Cr is 4.5 eV and that of Si is 4.05 eV, resulting in a barrier height of 0.45 eV. However, the barrier height can be affected by the physical conditions of the metal–semiconductor interface. The M–S–M junction model, based on thermionic field emission across the Schottky barriers, has been applied for various nanowire configurations to extract electrical properties of NWs from measured I–V curves with good agreement [24]. Typical M–S–M junction nanowire I– V characteristics are either asymmetric or symmetric, depending on the built-in potential and contact areas at the M–S junction at each end of the NWs [24]. We

apply the M–S–M junction model (using Matlab-based PKUMSM software [24]) to fit our SiNW I–V curve data. The inputs for the PKUMSM software are the physical dimensions of our SiNW, and parameters of the effective mass and relative permittivity of bulk silicon, 0.98 for electron, 0.49 for hole, and 11.8, respectively. The fit is excellent, as shown in figure 4. The fit can be used to extract electrical parameters of the SiNW, such as carrier mobility and Schottky barrier height. The extracted mobility and barrier height values as a function of the back-gate voltages from the fit in figure 4 are shown in table 1. The mobility values are very close to 2.4 $cm^2\ V^{-1}\ s^{-1}$, which are similar to the values from synthesized SiNWs consisting of crystalline cores covered with an amorphous oxide sheath [20]. The mobility is lower than that in bulk silicon because of the scattering and electrical contact conditions on a SiNW [20]. A comparison of the extracted parameters of the SiNW with the surface conditions of thermally grown SiO_2, HF-dipped, and re-oxidized is shown in table 2. Our I–V characteristics clearly show asymmetry that indicates that the Cr/Si contacts are Schottky contacts and the barrier at each contact is slightly different. Because substantial quantum size effects require a SiNW effective diameter of less than ~5nm [24, 25], the M–S–M junction model is suitable for extracting the semiconductor parameters of our SiNWs.

4. Surface modification of the SiNW

The electrical characteristics of a single SiNW show a strong dependence on surface condition. After measuring the I–V characteristics shown in figure 3, we dipped the SiNW into dilute HF (10% HF) for 5 min for SiO_2 removal, resulting in nominally hydrogen (H) terminated Si(001) surfaces on all four sides of the SiNW. The SiNW now also becomes freestanding at some distance (~300 nm) above the BOX (3 μm thick) as shown in figure 2 (HF-dipped). The SiNW is suspended because the HF solution undercuts the SiO_2 underneath the SiNW. The etch rate of SiO_2 in 10% HF solution is approximately 80 nm min^{-1}. The I–V characteristics of the freestanding H-terminated SiNW are shown in figure 5. The HF treated SiNWs show an inversion of electronic conduction from the original p-type to n-type, and approximately one order of magnitude lower current at the same back-gate voltage than that for the same SiNW attached to the BOX and covered on all sides by SiO_2. For example, the current is ~23

nA with 0 V gate voltage at 3 V bias for a SiNW attached to the BOX covered with SiO_2 all around, as shown in figure 3. For a H-terminated freestanding SiNW, the current, shown in figure 5 for various gate voltages, is ~2 nA with 0 V gate voltage at 3 V bias. Note that the electrical current change with the back-gate voltage change is relatively small because the dielectric constant of air is smaller than that of other materials such as SiO_2. It is clear from the I–V curves that the conductance change of the SiNW is a function of not only the back-gate voltage, but also the surface conditions.

The inversion of carriers has been observed in HF treated ultrathin silicon membranes [26] and is also a result of bulk studies [26–30]. The inversion of electronic conduction from p-type to n-type depending on the surface condition of the SiNW can be described by Fermi energy pinning [31, 32] as we will discuss later.

The nominally H-terminated freestanding SiNW was subsequently re-oxidized in a hot sulfuric acid and hydrogen peroxide mixture (4:1 ratio), leaving a freestanding SiNW covered on all sides by an ~1–3 nm thick oxide [33]. I–V curves for this situation are shown in figure 6. The quality (density) of the SiO_2 will be lower than thermally grown SiO_2. It is clear that the SiNW reverts to p-type FET characteristics, as in figure 3, indicating that the effect of the Fermi energy pinning is removed.

5. Discussion

Because of the very large surface-to-volume ratio of nanowires and nanomembranes, the surface chemical condition can significantly influence electronic transport. Recent work on very thin Si template layers (sheets that correspond in thickness to our SiNWs but are laterally much larger) has demonstrated the complexity caused by even a very simple surface chemical modification and also reviews past work [26]. The two surface conditions of the current work, oxide termination and nominal H-termination produced by HF etching of the oxide, are similar to those of [26], but here we have a freestanding-wire configuration and all surfaces have the same orientation.

The most consistent result in response to surface condition modification is that H-termination produces n-type behavior. It is reported in all cases that H-termination of Si(001) by HF etching creates significant band bending due to trace chemical elements such

as fluorine (F) [25, 31, 34, 35]. The effective n-type behavior is caused by a gating with the surface charge, although the details of the bending and charge transfer mechanism are not well understood [31, 36]. It has been suggested that the surface states created by the HF-dip pin the Fermi energy level ~0.2–0.3 eV below the conduction band minimum [31]. In the present situation, the effect (at least at zero applied gate voltage) is similar to having a gate all around the SiNW, with the potential on the gate provided by surface charges. At room temperature this position of the Fermi energy level can produce sufficient electron population in the conduction band to outnumber the majority carrier concentration in p-type silicon. The Fermi energy pinning explains the n-type FET-like I–V characteristics as shown in figure 5 (inset).

The lowered conductivity in the H-terminated SiNW, in contrast to the behavior on SiNMs, for which the conductivity dramatically increases, may be explainable in the following way. An electron carrier concentration of the order of 1.3×10^{14} cm^{-3} near the Si surface of the HF treated thin Si membrane due to the Fermi energy pinning has been reported [26, 31, 32]. In [26], only one side is HF treated. Our SiNW has all four sides H-terminated with the method used in [26]. Because the Debye length is ~130 nm, the induced electrons may be located throughout the volume of the SiNW. This electron density is comparable to the hole concentration in the initial p-type Si, and may make the SiNW almost intrinsic, leading to the lower current while still giving n-type FET characteristics. It also has been reported that the carrier mobility is sensitive to the electrical contacts between a metal and semiconductor [20]. The M–S–M model [23, 24] applied to fit the data in figure 5 shows twofold lower carrier mobility than the annealed case [20]. The lower effective mobile-carrier density and mobility may explain the discrepancy between our work and [26], where the electrical contacts are Ohmic.

Explanation of the behavior with oxide termination is more challenging. Various effects of Si/SiO_2 interface states on SiNW (attached to BOX) electrical conduction mechanisms have been reported [37, 38]. The interface state density could be in the range of 10^{10}–10^{12} cm^{-2} eV^{-1} [37]. The mobile-carrier concentration in our SiNW (N_A is ~10^{15} cm^{-3}, cross-sectional dimension 140 nm × 120 nm) could be reduced significantly. For example, Niklas et al [38] have reported

an ambipolar behavior of a SiNW (fabricated from p-type SOI and with Schottky contacts) depending on back-gate voltages, while Pennelle et al [19] have reported n-type FET behavior of a SiNW (fabricated from p-type SOI and with effective Ohmic contacts). All of these investigations are based on a SiNW sitting on the BOX layer of SOI with thermally grown SiO_2 covering the other surfaces. Oxide terminated SiNMs with thicknesses from ~20 to >200 nm and effective Ohmic contacts show n-type behavior, both before HF etching and upon re-oxidation [26].

Our SiNWs are suspended, unique with respect to any prior work measuring electrical transport. The conditions are well defined and reproducible. The current transport is in accumulation mode (hole carrier) when SiO_2-covered (figure 6), and inversion mode (electron carrier) when nominally H-terminated (figure 5). Although they cannot be directly compared, the inversion with H-termination that occurs for our SiNWs is consistent with other studies on attached SiNWs and sheets. The oxide termination is not; yet it is internally consistent: for both attached and freestanding we obtain p-type behavior when all surfaces are terminated with oxide. There is nothing to compare with our freestanding oxidized wires. The literature for attached oxidized SiNWs is inconsistent, as indicated above.

6. Summary and conclusions

We demonstrate a process for fabricating integrated freestanding single-crystal SiNWs using conventional optical lithography and anisotropic wet chemical Si etching that is readily scalable from a single SiNW to the integration of wafer-scale arrays of SiNWs. Because the SiNWs are freestanding, complexities associated with a substrate are removed. We perform electronic-transport measurements for two surface conditions, oxide all around and H-terminated all around, and compare the former with results for attached SiNWs. The purpose of such measurements is to establish quantitative and consistent baselines for potential future SiNW chemical sensors based on modification of the Si surface. Prior work in this regard has generally used highly doped Si, in which many of the effects that could be of interest simply become overwhelmed by the NW 'bulk' conductivity.

A comparison of the current carrier reversal and magnitude of conductivity with surface condition in a SiNW (here the replacement of H-termination with SiO_2/SiO [39, 40]), as well as a quantitative determination of interface states with other measurements, should allow the development of a better understanding of the influence of individual surface bonds on creating surface fields that affect conductivity. In addition, the effects of Schottky contacts with various metals and annealing on SiNW electrical conduction need to be further investigated for reliable and reproducible performance in potential sensor applications. Our experimental results suggest that p-type and n-type SiNW FET devices can be integrated by selectively growing SiO_2 on the SiNW without complex CMOS processes such as extra lithography and selective doping. Ultimately, utilizing the high surface sensitivity of the SiNW could make possible much more sensitive chemical identification [41] if proper surface terminations can be developed. The characteristics of inversion can be utilized to make large-scale complementary logic circuitry with the integrated SiNWs by conditioning the surfaces.

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Notes

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Appendix

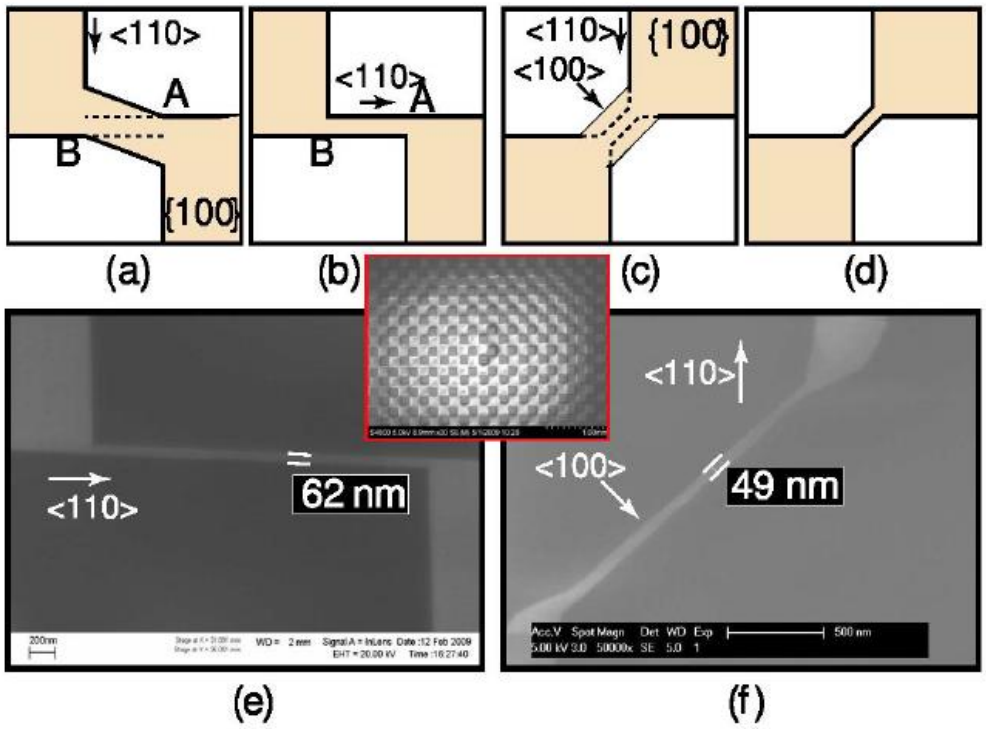
Table 1 Extracted parameters of a SiNW covered with SiO_2.

	V_{bg}					
	0 V	2 V	4 V	6 V	8 V	10 V
Mobility ($cm^2\ V^{-1}\ s^{-1}$)	2.80	2.27	2.29	2.12	2.44	2.56
Barrier (ϕ_1, eV)	0.435	0.458	0.468	0.479	0.472	0.471
Barrier (ϕ_2, eV)	0.438	0.461	0.469	0.478	0.471	0.469
Resistance (Ω)	1.8×10^7	1.4×10^7	1.2×10^7	1.1×10^7	1.0×10^7	9.9×10^6

Table 2 Comparison of extracted parameters for a SiNW covered with thermally grown SiO_2, HF-dipped, and re-oxidized.

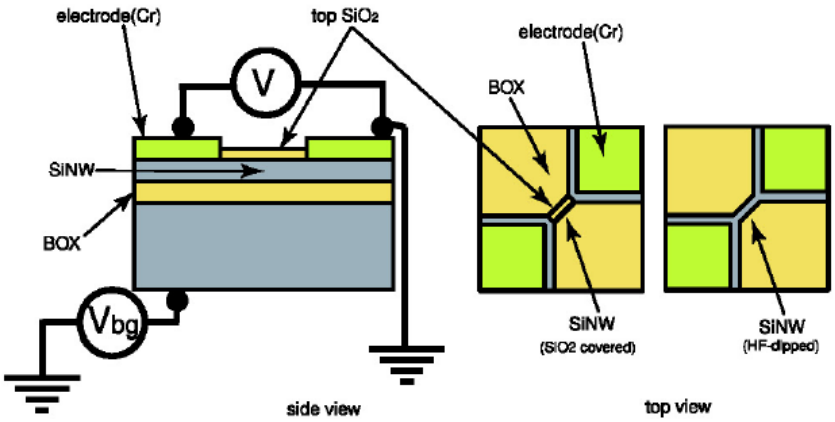
	Barrier (ϕ_1, eV)	Barrier (ϕ_2, eV)	Mobility ($cm^2\ V^{-1}\ s^{-1}$)	Resistance (Ω)	R_{sh1} (Ω)	R_{sh2} (Ω)
Thermally grown SiO_2	0.471	0.469	2.56	9.9×10^6	1.7×10^9	9.9×10^8
HF-dipped	0.697	0.639	0.22	8.4×10^7	9.0×10^8	9.8×10^8
Re-oxidized	0.569	0.570	0.30	4.9×10^7	3.3×10^9	5.2×10^{12}

Figure 1



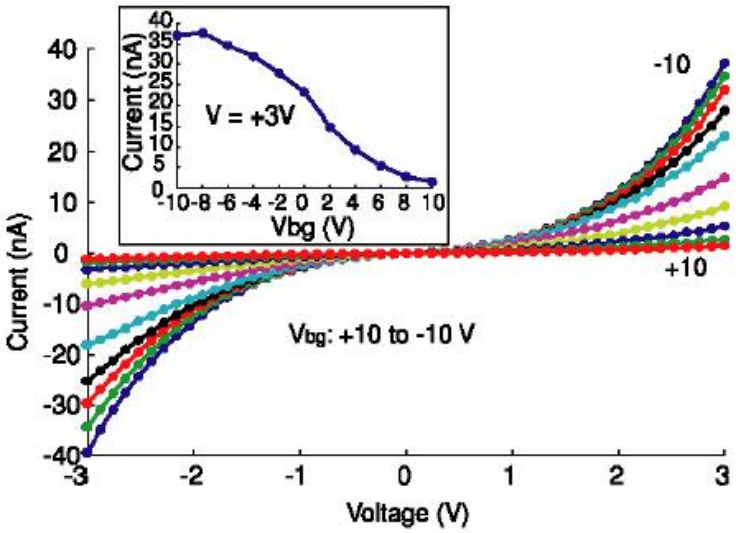
Fabrication of individual SiNWs on a SOI wafer. (a) Patterning SiO_2 for SiNW integration along the (110) crystal direction; the offset of points A and B determines the final width of the SiNW; (b) final (110) oriented SiNW; (c) patterning SiO_2 for SiNW integration along the ⟨100⟩ crystal direction. (d) The width of the SiNW is determined by the anisotropic wet chemical etch time; (e) and (f) SEM images of fabricated SiNWs. All SEM images are taken before Si_xN_y deposition. The SiNW in (e) is along the ⟨110⟩ direction as in (b), and the SiNW in (f) is along the ⟨100⟩ direction as in (d). The inset shows a portion of the integrated SiNWs on a quarter piece of 6" wafer.

Figure 2



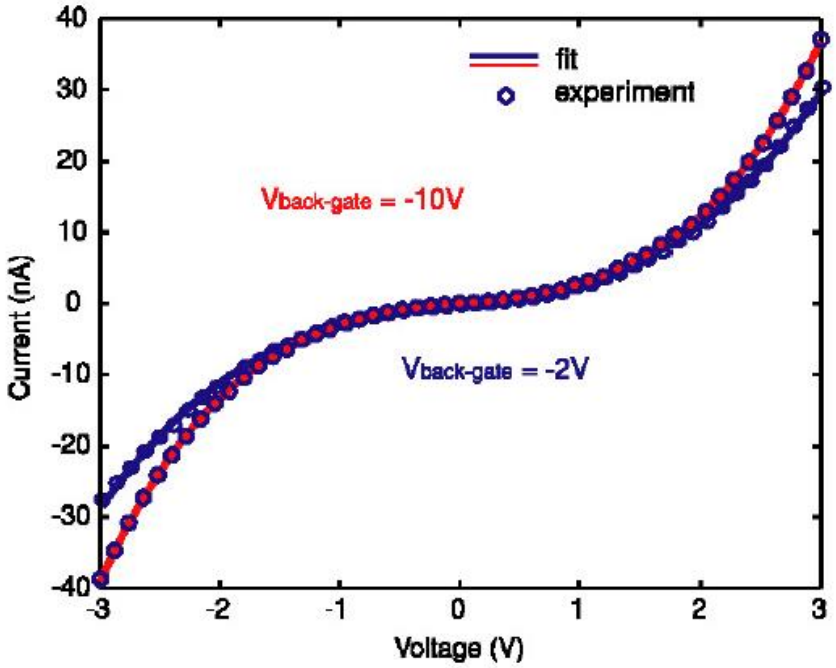
I–V measurement setup. Chromium is directly evaporated on SiNW contact pads immediately after SiO_2 etch in 10% HF. V_{bg} is applied to the backside of the wafer through a chuck on which it is sitting.
Measurement setup with the SiO_2 covered SiNW along the ⟨100⟩ direction and for the suspended SiNW (here shown without oxide) along the ⟨100⟩ direction.

Figure 3



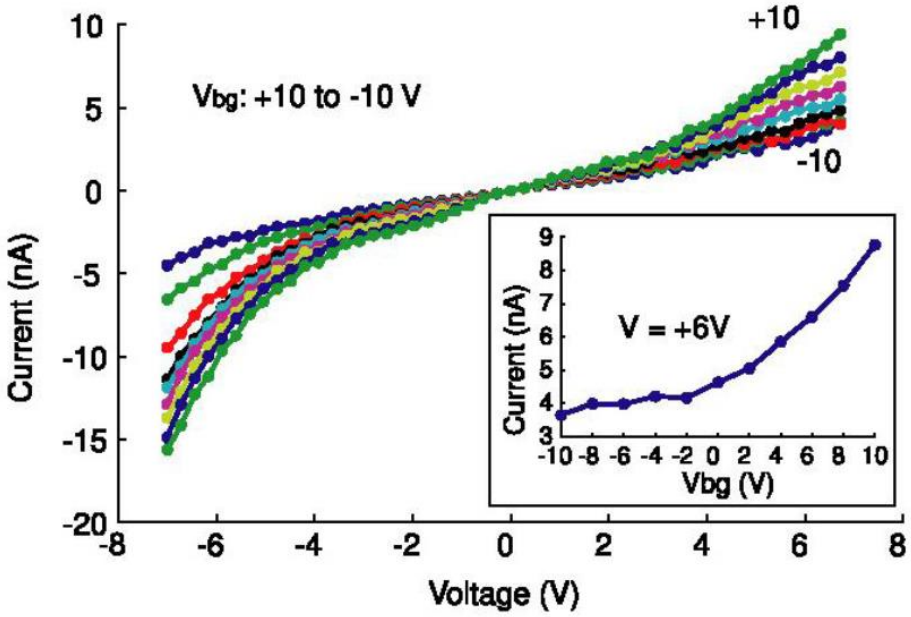
I–V characteristics of a 140 nm thick, 120 nm wide, and 3 μm long SiNW in the ⟨100⟩ direction with a native oxide on all sides, attached to the BOX. Different I–V curves correspond to applied back-gate voltages from -10 to 10 V relative to zero bias, with 2 V increments. As the gate voltage increases, the electrical conductivity drops (inset), similar to that of a p-type field effect transistor (FET) operating in accumulation mode.

Figure 4



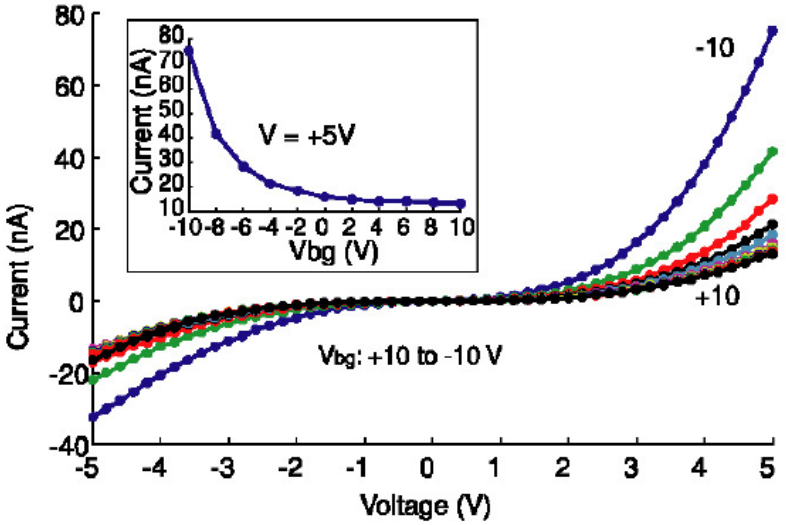
Two selected measured data sets (V_{bg} = -2 and -10 V) selected from figure 3 as examples to show the M– S–M model fit. Measured I–V curves and fits for a SiNW covered on all sides with SiO_2 and still attached to the BOX. The SiNW is 140 nm thick, 120 nm wide, and 3 μm long in the ⟨100⟩ direction. The fit uses Matlab for M–S–M junction analysis [23, 24]. The circles are data, the solid line is a fit. Note that the current only weakly depends on the gate voltage in this range.

Figure 5



I–V characteristics of a suspended 140 nm thick, 120 nm wide, and 3 μm long SiNW in the ⟨100⟩ direction with H-termination on all four sides. The measurements were made within 5 min of the HF etch. The I–V curves indicate n-type FET-like characteristics, i.e., the SiNW shows reversed carrier polarity relative to the oxide covered surfaces, indicating the formation of inversion layers near the surfaces. Note that the bias voltage range is greater here than that in figures 3, 4 and 6.

Figure 6.



I–V characteristics of a suspended, re-oxidized 140 nm thick, 120 nm wide, and 3 μm long SiNW in the ⟨100⟩ direction. The SiNW is re-oxidized in a hot sulfuric acid and hydrogen peroxide mixture for 10 min. The I–V curves indicate a carrier polarity that reverts back from n-type (figure 5) to p-type FET-like characteristics. The conductivity increases again, relative to the H-termination, to almost the values of the original oxidized SiNW.