

# Comparison of Three Space Vector PWM Methods for a Three-Level Inverter with a Permanent Magnet Machine Load

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## Recommended Citation

Strandt, Alia Rebecca, "Comparison of Three Space Vector PWM Methods for a Three-Level Inverter with a Permanent Magnet Machine Load" (2013). *Master's Theses (2009 -)*. Paper 234.  
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COMPARISON OF THREE SPACE VECTOR PWM METHODS FOR A  
THREE-LEVEL INVERTER WITH A PERMANENT  
MAGNET MACHINE LOAD

by  
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A Thesis Submitted to the Faculty of the  
Graduate School, Marquette University,  
in Partial Fulfillment of the Requirements for the  
Degree of Master of Science

Milwaukee, Wisconsin

December 2013

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## **PREFACE**

### COMPARISON OF THREE SPACE VECTOR PWM METHODS FOR A THREE-LEVEL INVERTER WITH A PERMANENT MAGNET MACHINE LOAD

Alia Rebecca Strandt, B.S.

Under the supervision of Professor Nabeel A.O. Demerdash

Marquette University, 2013

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*To my husband and my family*

**ABSTRACT**  
COMPARISON OF THREE SPACE VECTOR PWM METHODS FOR A  
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MAGNET MACHINE LOAD

Alia Rebecca Strandt

Marquette University, 2013

Much work exists on multilevel space vector pulse width modulation (PWM) to drive induction machines, in which the rotor currents are induced by stator rotating field effects. However, there are few investigations that analyze these modulation methods applied to permanent magnet (PM) and wound-field synchronous machines, in which the rotor induces a back emf in the stator. In this thesis, three different three-level space vector PWM switching sequences are applied to a three-level neutral-point-clamped (NPC) inverter driving an internal permanent magnet (IPM) machine load. The inherent qualities of each of the switching sequences when under the influence of a forcing function (the back emf) created by the permanent magnets of the machine are investigated. In particular, output voltage quality, output current quality, and dc bus neutral point balance are analyzed and compared. Two machine operating conditions are considered: rated speed, rated load and half speed, rated load. By considering these two different operating speeds, the three switching sequences may be analyzed under both two-level operation and three-level operation of the inverter. A circuit model based on the machine state space model in the abc current frame of reference is used to model the IPM machine load.

First, a short introduction to two-level inverters and a theoretical development of two-level space vector PWM are presented to introduce these basic principles. Then, an overview of the three main multilevel inverter topologies including their associated advantages and disadvantages is presented. A theoretical development of three-level space vector PWM is built upon the concepts introduced in the two-level case, and the three switching sequences under investigation are explained. The system model, including the IPM machine load, the three-level NPC inverter, and the space vector PWM algorithms, is implemented using MATLAB Simulink. All simulation results are analyzed based on output voltage and current distortion and neutral point imbalance, and a comparison between the three switching sequences is presented.

## ACKNOWLEDGEMENTS

Alia Rebecca Strandt

Throughout my time at Marquette University, I have had the opportunity to work with many wonderful people. This work would not have been possible without their love, support, and guidance.

First, I would like to thank my adviser and my committee for their guidance throughout my studies. My adviser Dr. Nabeel Demerdash has been very helpful as he shared his vast knowledge of electric machines and provided overall guidance in my research. I also want to thank Dr. Edwin Yaz for his helpful input and for always encouraging my curiosity and creativity in his wonderful classes. I am very grateful for the incredibly insightful comments and advice from Dr. Dan Ionel as well. Last, but not least, I want to thank Dr. Ahmed Sayed Ahmed. He has been an extremely helpful resource for PWM theory and a constant source of encouragement and perspective.

I also want to thank my family for their patience, love, and support as I completed my work. My husband Andrew Strandt was my constant support throughout my studies, and without his encouragement, this work would not have been completed. I want to thank my parents, John and Margarita Manarik, for their constant love and support. Their encouragement throughout my life has brought me to this point. I also thank my two siblings, Selina and Craig Manarik. Whether discussing math and engineering or simply watching a movie together, it is a great joy to spend time with them. My father-in-law and mother-in-law, Carl and Linda Strandt, have been a great help over the years, and I thank them for their generosity. I also thank my siblings-in-law, Mary Strandt, Daniel Strandt, Timothy Strandt, Peter Strandt, Michael Strandt, and Therese Strandt, for all of the fun times. My love and appreciation go out to all of my extended family as well.

I also want to thank all of the members of the Electric Machines and Drives lab at Marquette University, particularly Dr. Gennadi Sizov, Dr. Peng Zhang, and Mr. Jiangbiao He. Everyone has provided good suggestions and discussions over the years. It has been a pleasure working with all of them.

Finally, I would like to thank The Greater Milwaukee Foundation for the Frank Rogers Bacon Research Assistantship, NSF-GOALI grant number 1028348, and

the Wisconsin Energy Research Consortium for their financial support. Likewise, I thank A.O. Smith Corporation and ANSYS for their generous donation of equipment and simulation software. Both Dr. Marius Rosu and Mr. Mark Solveson of ANSYS provided excellent Simplorer modeling advice, for which I am very grateful.

There are many others who have been a tremendous support to me over the years. Though you may not be mentioned here, my thanks and appreciation go out to all of you.

## Table of Contents

<b>List of Tables</b>	<b>v</b>
<b>List of Figures</b>	<b>vii</b>
<b>1 Introduction</b>	<b>1</b>
1.1 Background of the Problem . . . . .	1
1.2 Review of Literature . . . . .	2
1.2.1 Two-Level PWM . . . . .	2
1.2.2 Multilevel PWM . . . . .	6
1.3 Statement of the Problem . . . . .	14
<b>2 Theoretical Development of Two-Level Inverters and SVPWM</b>	<b>15</b>
2.1 Two-Level Inverters . . . . .	15
2.2 Two-Level Space Vector PWM . . . . .	20
<b>3 Theoretical Development of Three-Level Inverters and SVPWM</b>	<b>41</b>
3.1 Three-Level Inverter Topologies . . . . .	42
3.2 Three-Level SVPWM . . . . .	47
3.2.1 SVPWM Method 1 . . . . .	60
3.2.2 SVPWM Method 2 . . . . .	61
3.2.3 SVPWM Method 3 . . . . .	63
<b>4 Development of System Models and Simulations</b>	<b>67</b>
4.1 Introduction to Machine State Space Models . . . . .	68

4.2	The Machine to be Used in Simulation . . . . .	69
4.2.1	Machine Specifications . . . . .	69
4.2.2	Machine Model . . . . .	72
4.3	Space Vector PWM Simulation Models . . . . .	75
4.4	Three-Level NPC Inverter System Model . . . . .	77
<b>5</b>	<b>Simulation Results and Analysis</b>	<b>80</b>
5.1	Space Vector PWM Analysis Tools . . . . .	80
5.2	Results and Analysis for Method 1 . . . . .	83
5.2.1	Rated Speed, Rated Load Results and Analysis . . . . .	83
5.2.2	Half Rated Speed, Rated Load Results and Analysis . . . . .	90
5.3	Results and Analysis for Method 2 . . . . .	97
5.3.1	Rated Speed, Rated Load Results and Analysis . . . . .	97
5.3.2	Half Rated Speed, Rated Load Results and Analysis . . . . .	111
5.4	Results and Analysis for Method 3 . . . . .	124
5.4.1	Rated Speed, Rated Load Results and Analysis . . . . .	124
5.4.2	Half Rated Speed, Rated Load Results and Analysis . . . . .	131
5.5	Comparison of the Three Methods . . . . .	138
5.5.1	Operation at Rated Speed, Rated Load . . . . .	138
5.5.2	Operation at Half Speed, Rated Load . . . . .	142
<b>6</b>	<b>Conclusions and Recommendations for Future Work</b>	<b>148</b>
6.1	Conclusions . . . . .	148
6.2	Recommendations for Future Work . . . . .	150
	<b>Bibliography</b>	<b>153</b>
<b>A</b>	<b>Space Vector PWM Switching Tables</b>	<b>161</b>
A.1	Switching Tables for Method 1 . . . . .	161
A.2	Switching Tables for Method 2 . . . . .	174
A.3	Switching Tables for Method 3 . . . . .	186

## List of Tables

2.1	State table representing all switching combinations. . . . .	21
2.2	Voltages corresponding to the various switching states in Volts. . . .	23
2.3	Switching voltages in space vector form. . . . .	24
3.1	Representation of switching states for a switching combination where $x = \{a, b, c\}$ . . . . .	48
3.2	Line-to-line and line-to-neutral voltages in Volts corresponding to the 27 switching states. . . . .	51
3.3	Three-level switching voltages in space vector form. . . . .	52
4.1	Ratings of the IPM machine under investigation. . . . .	70
4.2	Harmonic components of the back emf for the IPM machine under investigation found using FEA. . . . .	71
4.3	Phase resistance and inductances of the IPM machine under investiga- tion found using FEA. . . . .	71
5.1	Summary of line-to-neutral voltage THD for all three methods at rated speed, rated load. . . . .	138
5.2	Summary of line-to-line voltage THD for all three methods at rated speed, rated load. . . . .	139
5.3	Summary of phase current THD and RMS value of neutral point current for all three methods at rated speed, rated load. . . . .	140
5.4	Summary of the 2-norm of the drift of the voltage vectors for all three methods at rated speed, rated load. . . . .	141

5.5	Summary of line-to-neutral voltage THD for all three methods at half speed, rated load. . . . .	143
5.6	Summary of line-to-line voltage THD for all three methods at half speed, rated load. . . . .	144
5.7	Summary of phase current THD and RMS value of neutral point current for all three methods at half speed, rated load. . . . .	145
5.8	Summary of the 2-norm of the drift of the voltage vectors for all three methods at half speed, rated load. . . . .	146

## List of Figures

2.1	Generic two-level, three-phase inverter. . . . .	16
2.2	Basic two-level voltage source inverter. . . . .	18
2.3	Basic two-level current source inverter. . . . .	19
2.4	The equivalent load circuit for a switching state of $S_1 = (1\ 0\ 0)$ . . . . .	22
2.5	The voltage vectors plotted in the $(\alpha - \beta)$ plane. . . . .	25
2.6	The reference space vector with the voltage vectors in the $(\alpha - \beta)$ plane. . . . .	27
2.7	The maximum reference vector magnitude for linear modulation in the $(\alpha - \beta)$ plane. . . . .	28
2.8	The division of the switching states in Sector I. . . . .	37
2.9	The division of the switching states in Sector II. . . . .	37
2.10	The division of the switching states in Sector III. . . . .	37
2.11	The division of the switching states in Sector IV. . . . .	37
2.12	The division of the switching states in Sector V. . . . .	37
2.13	The division of the switching states in Sector VI. . . . .	37
2.14	Time domain plot of the line-to-line voltages for an RL load using Two-Level SVM. . . . .	38
2.15	Time domain plot of the line-to-neutral voltages for an RL load using Two-Level SVM. . . . .	38
2.16	Time domain plot of the phase currents for an RL load using Two-Level SVM. . . . .	39
2.17	Space vector representation of the line-to-neutral voltage in the $(\alpha - \beta)$ plane. . . . .	40
2.18	Space vector representation of the phase current in the $(\alpha - \beta)$ plane. . . . .	40

3.1	Three-level neutral-point-clamped inverter. . . . .	43
3.2	Three-level flying capacitor inverter. . . . .	45
3.3	Three-level cascaded H-bridge inverter. . . . .	46
3.4	The three-level voltage vectors plotted in the $(\alpha - \beta)$ plane. . . . .	53
3.5	Two-level hexagons within the three-level hexagon. . . . .	57
3.6	The division of the three-level hexagon into sectors. . . . .	58
3.7	Sector I with its corresponding hexagon. . . . .	58
3.8	Mapping of the three-level voltage reference into the sector I two-level hexagon. . . . .	59
3.9	Mapping of the three-level voltage reference into the sector I two-level hexagon (enlarged). . . . .	59
3.10	Method 1 switching pattern in Sector I, two-level sector I. . . . .	62
3.11	Method 1 switching pattern in Sector I, two-level sector II. . . . .	62
3.12	Method 2 switching pattern in Sector I, two-level sector I. . . . .	63
3.13	Method 2 switching pattern in Sector I, two-level sector II. . . . .	63
3.14	Method 3 switching pattern in Sector I, two-level sector II. . . . .	65
3.15	Method 3 switching pattern in Sector I, two-level sector III. . . . .	65
4.1	Circuit representation of the state space equations for the given IPM machine. . . . .	73
4.2	Simulated open circuit back emf of the IPM machine. . . . .	74
4.3	The generic space vector PWM pulse generator model. . . . .	76
4.4	System model including inverter, space vector PWM generator, and PM machine. . . . .	78
5.1	Line-to-neutral voltage $v_{An}$ for Method 1 rated speed, rated load. . .	84
5.2	FFT of line-to-neutral voltage $v_{An}$ for Method 1 rated speed, rated load. . .	84
5.3	Line-to-neutral voltage $v_{Bn}$ for Method 1 rated speed, rated load. . .	84
5.4	FFT of line-to-neutral voltage $v_{Bn}$ for Method 1 rated speed, rated load. . .	84
5.5	Line-to-neutral voltage $v_{Cn}$ for Method 1 rated speed, rated load. . .	84

5.6	FFT of line-to-neutral voltage $v_{Cn}$ for Method 1 rated speed, rated load.	84
5.7	Line-to-line voltage $v_{AB}$ for Method 1 rated speed, rated load. . . . .	86
5.8	FFT of line-to-line voltage $v_{AB}$ for Method 1 rated speed, rated load.	86
5.9	Line-to-line voltage $v_{BC}$ for Method 1 rated speed, rated load. . . . .	86
5.10	FFT of line-to-line voltage $v_{BC}$ for Method 1 rated speed, rated load.	86
5.11	Line-to-line voltage $v_{CA}$ for Method 1 rated speed, rated load. . . . .	86
5.12	FFT of line-to-line voltage $v_{CA}$ for Method 1 rated speed, rated load.	86
5.13	Phase current $i_A$ for Method 1 rated speed, rated load. . . . .	87
5.14	FFT of phase current $i_A$ for Method 1 rated speed, rated load. . . . .	87
5.15	Phase current $i_B$ for Method 1 rated speed, rated load. . . . .	87
5.16	FFT of phase current $i_B$ for Method 1 rated speed, rated load. . . . .	87
5.17	Phase current $i_C$ for Method 1 rated speed, rated load. . . . .	87
5.18	FFT of phase current $i_C$ for Method 1 rated speed, rated load. . . . .	87
5.19	Space vector of line-to-neutral voltages for Method 1 rated speed, rated load. . . . .	89
5.20	Space vector of phase currents for Method 1 rated speed, rated load.	89
5.21	Neutral point current $i_{NP}$ for Method 1 rated speed, rated load. . . . .	89
5.22	Line-to-neutral voltage $v_{An}$ for Method 1 half rated speed, rated load.	91
5.23	FFT of line-to-neutral voltage $v_{An}$ for Method 1 half rated speed, rated load. . . . .	91
5.24	Line-to-neutral voltage $v_{Bn}$ for Method 1 half rated speed, rated load.	91
5.25	FFT of line-to-neutral voltage $v_{Bn}$ for Method 1 half rated speed, rated load. . . . .	91
5.26	Line-to-neutral voltage $v_{Cn}$ for Method 1 half rated speed, rated load.	91
5.27	FFT of line-to-neutral voltage $v_{Cn}$ for Method 1 half rated speed, rated load. . . . .	91
5.28	Line-to-line voltage $v_{AB}$ for Method 1 half rated speed, rated load. . . . .	93
5.29	FFT of line-to-line voltage $v_{AB}$ for Method 1 half rated speed, rated load. . . . .	93

5.30	Line-to-line voltage $v_{BC}$ for Method 1 half rated speed, rated load. . .	93
5.31	FFT of line-to-line voltage $v_{BC}$ for Method 1 half rated speed, rated load. . . . .	93
5.32	Line-to-line voltage $v_{CA}$ for Method 1 half rated speed, rated load. . .	93
5.33	FFT of line-to-line voltage $v_{CA}$ for Method 1 half rated speed, rated load. . . . .	93
5.34	Phase current $i_A$ for Method 1 half rated speed, rated load. . . . .	94
5.35	FFT of phase current $i_A$ for Method 1 half rated speed, rated load. . .	94
5.36	Phase current $i_B$ for Method 1 half rated speed, rated load. . . . .	94
5.37	FFT of phase current $i_B$ for Method 1 half rated speed, rated load. . .	94
5.38	Phase current $i_C$ for Method 1 half rated speed, rated load. . . . .	94
5.39	FFT of phase current $i_C$ for Method 1 half rated speed, rated load. . .	94
5.40	Space vector of line-to-neutral voltages for Method 1 half rated speed, rated load. . . . .	96
5.41	Space vector of phase currents for Method 1 half rated speed, rated load.	96
5.42	Neutral point current $i_{NP}$ for Method 1 half rated speed, rated load.	96
5.43	Line-to-neutral voltage $v_{An}$ for Method 2 rated speed, rated load. . .	98
5.44	FFT of line-to-neutral voltage $v_{An}$ for Method 2 rated speed, rated load.	98
5.45	Line-to-neutral voltage $v_{Bn}$ for Method 2 rated speed, rated load. . .	98
5.46	FFT of line-to-neutral voltage $v_{Bn}$ for Method 2 rated speed, rated load.	98
5.47	Line-to-neutral voltage $v_{Cn}$ for Method 2 rated speed, rated load. . .	98
5.48	FFT of line-to-neutral voltage $v_{Cn}$ for Method 2 rated speed, rated load.	98
5.49	Line-to-line voltage $v_{AB}$ for Method 2 rated speed, rated load. . . . .	100
5.50	FFT of line-to-line voltage $v_{AB}$ for Method 2 rated speed, rated load.	100
5.51	Line-to-line voltage $v_{BC}$ for Method 2 rated speed, rated load. . . . .	100
5.52	FFT of line-to-line voltage $v_{BC}$ for Method 2 rated speed, rated load.	100
5.53	Line-to-line voltage $v_{CA}$ for Method 2 rated speed, rated load. . . . .	100
5.54	FFT of line-to-line voltage $v_{CA}$ for Method 2 rated speed, rated load.	100
5.55	Phase current $i_A$ for Method 2 rated speed, rated load. . . . .	101

5.56	FFT of phase current $i_A$ for Method 2 rated speed, rated load. . . .	101
5.57	Phase current $i_B$ for Method 2 rated speed, rated load. . . . .	101
5.58	FFT of phase current $i_B$ for Method 2 rated speed, rated load. . . .	101
5.59	Phase current $i_C$ for Method 2 rated speed, rated load. . . . .	101
5.60	FFT of phase current $i_C$ for Method 2 rated speed, rated load. . . .	101
5.61	Space vector of line-to-neutral voltages for Method 2 rated speed, rated load. . . . .	103
5.62	Space vector of phase currents for Method 2 rated speed, rated load.	103
5.63	Neutral point current $i_{NP}$ for Method 2 rated speed, rated load. . .	103
5.64	Line-to-neutral voltage $v_{An}$ for Method 2 rated speed, rated load and $C_{bus} = 400mF$ . . . . .	105
5.65	FFT of line-to-neutral voltage $v_{An}$ for Method 2 rated speed, rated load and $C_{bus} = 400mF$ . . . . .	105
5.66	Line-to-neutral voltage $v_{Bn}$ for Method 2 rated speed, rated load and $C_{bus} = 400mF$ . . . . .	105
5.67	FFT of line-to-neutral voltage $v_{Bn}$ for Method 2 rated speed, rated load and $C_{bus} = 400mF$ . . . . .	105
5.68	Line-to-neutral voltage $v_{Cn}$ for Method 2 rated speed, rated load and $C_{bus} = 400mF$ . . . . .	105
5.69	FFT of line-to-neutral voltage $v_{Cn}$ for Method 2 rated speed, rated load and $C_{bus} = 400mF$ . . . . .	105
5.70	Line-to-line voltage $v_{AB}$ for Method 2 rated speed, rated load and $C_{bus} = 400mF$ . . . . .	106
5.71	FFT of line-to-line voltage $v_{AB}$ for Method 2 rated speed, rated load and $C_{bus} = 400mF$ . . . . .	106
5.72	Line-to-line voltage $v_{BC}$ for Method 2 rated speed, rated load and $C_{bus} = 400mF$ . . . . .	106
5.73	FFT of line-to-line voltage $v_{BC}$ for Method 2 rated speed, rated load and $C_{bus} = 400mF$ . . . . .	106

5.74	Line-to-line voltage $v_{CA}$ for Method 2 rated speed, rated load and $C_{bus} = 400mF$ . . . . .	106
5.75	FFT of line-to-line voltage $v_{CA}$ for Method 2 rated speed, rated load and $C_{bus} = 400mF$ . . . . .	106
5.76	Phase current $i_A$ for Method 2 rated speed, rated load and $C_{bus} = 400mF$ .108	
5.77	FFT of phase current $i_A$ for Method 2 rated speed, rated load and $C_{bus} = 400mF$ . . . . .	108
5.78	Phase current $i_B$ for Method 2 rated speed, rated load and $C_{bus} = 400mF$ .108	
5.79	FFT of phase current $i_B$ for Method 2 rated speed, rated load and $C_{bus} = 400mF$ . . . . .	108
5.80	Phase current $i_C$ for Method 2 rated speed, rated load and $C_{bus} = 400mF$ .108	
5.81	FFT of phase current $i_C$ for Method 2 rated speed, rated load and $C_{bus} = 400mF$ . . . . .	108
5.82	Space vector of line-to-neutral voltages for Method 2 rated speed, rated load and $C_{bus} = 400mF$ . . . . .	109
5.83	Space vector of phase currents for Method 2 rated speed, rated load and $C_{bus} = 400mF$ . . . . .	109
5.84	Neutral point current $i_{NP}$ for Method 2 rated speed, rated load and $C_{bus} = 400mF$ . . . . .	110
5.85	Line-to-neutral voltage $v_{An}$ for Method 2 half rated speed, rated load.112	
5.86	FFT of line-to-neutral voltage $v_{An}$ for Method 2 half rated speed, rated load. . . . .	112
5.87	Line-to-neutral voltage $v_{Bn}$ for Method 2 half rated speed, rated load.112	
5.88	FFT of line-to-neutral voltage $v_{Bn}$ for Method 2 half rated speed, rated load. . . . .	112
5.89	Line-to-neutral voltage $v_{Cn}$ for Method 2 half rated speed, rated load.112	
5.90	FFT of line-to-neutral voltage $v_{Cn}$ for Method 2 half rated speed, rated load. . . . .	112
5.91	Line-to-line voltage $v_{AB}$ for Method 2 half rated speed, rated load. .	114

5.92	FFT of line-to-line voltage $v_{AB}$ for Method 2 half rated speed, rated load. . . . .	114
5.93	Line-to-line voltage $v_{BC}$ for Method 2 half rated speed, rated load. .	114
5.94	FFT of line-to-line voltage $v_{BC}$ for Method 2 half rated speed, rated load. . . . .	114
5.95	Line-to-line voltage $v_{CA}$ for Method 2 half rated speed, rated load. .	114
5.96	FFT of line-to-line voltage $v_{CA}$ for Method 2 half rated speed, rated load. . . . .	114
5.97	Phase current $i_A$ for Method 2 half rated speed, rated load. . . . .	115
5.98	FFT of phase current $i_A$ for Method 2 half rated speed, rated load. .	115
5.99	Phase current $i_B$ for Method 2 half rated speed, rated load. . . . .	115
5.100	FFT of phase current $i_B$ for Method 2 half rated speed, rated load. .	115
5.101	Phase current $i_C$ for Method 2 half rated speed, rated load. . . . .	115
5.102	FFT of phase current $i_C$ for Method 2 half rated speed, rated load. .	115
5.103	Space vector of line-to-neutral voltages for Method 2 half rated speed, rated load. . . . .	116
5.104	Space vector of phase currents for Method 2 half rated speed, rated load.	116
5.105	Neutral point current $i_{NP}$ for Method 2 half rated speed, rated load.	117
5.106	Line-to-neutral voltage $v_{An}$ for Method 2 half rated speed, rated load and $C_{bus} = 400mF$ . . . . .	118
5.107	FFT of line-to-neutral voltage $v_{An}$ for Method 2 half rated speed, rated load and $C_{bus} = 400mF$ . . . . .	118
5.108	Line-to-neutral voltage $v_{Bn}$ for Method 2 half rated speed, rated load and $C_{bus} = 400mF$ . . . . .	118
5.109	FFT of line-to-neutral voltage $v_{Bn}$ for Method 2 half rated speed, rated load and $C_{bus} = 400mF$ . . . . .	118
5.110	Line-to-neutral voltage $v_{Cn}$ for Method 2 half rated speed, rated load and $C_{bus} = 400mF$ . . . . .	118

5.111	FFT of line-to-neutral voltage $v_{Cn}$ for Method 2 half rated speed, rated load and $C_{bus} = 400mF$ . . . . .	118
5.112	Line-to-line voltage $v_{AB}$ for Method 2 half rated speed, rated load and $C_{bus} = 400mF$ . . . . .	120
5.113	FFT of line-to-line voltage $v_{AB}$ for Method 2 half rated speed, rated load and $C_{bus} = 400mF$ . . . . .	120
5.114	Line-to-line voltage $v_{BC}$ for Method 2 half rated speed, rated load and $C_{bus} = 400mF$ . . . . .	120
5.115	FFT of line-to-line voltage $v_{BC}$ for Method 2 half rated speed, rated load and $C_{bus} = 400mF$ . . . . .	120
5.116	Line-to-line voltage $v_{CA}$ for Method 2 half rated speed, rated load and $C_{bus} = 400mF$ . . . . .	120
5.117	FFT of line-to-line voltage $v_{CA}$ for Method 2 half rated speed, rated load and $C_{bus} = 400mF$ . . . . .	120
5.118	Phase current $i_A$ for Method 2 half rated speed, rated load and $C_{bus} = 400mF$ . . . . .	121
5.119	FFT of phase current $i_A$ for Method 2 half rated speed, rated load and $C_{bus} = 400mF$ . . . . .	121
5.120	Phase current $i_B$ for Method 2 half rated speed, rated load and $C_{bus} = 400mF$ . . . . .	121
5.121	FFT of phase current $i_B$ for Method 2 half rated speed, rated load and $C_{bus} = 400mF$ . . . . .	121
5.122	Phase current $i_C$ for Method 2 half rated speed, rated load and $C_{bus} = 400mF$ . . . . .	121
5.123	FFT of phase current $i_C$ for Method 2 half rated speed, rated load and $C_{bus} = 400mF$ . . . . .	121
5.124	Space vector of line-to-neutral voltages for Method 2 half rated speed, rated load and $C_{bus} = 400mF$ . . . . .	123

5.125	Space vector of phase currents for Method 2 half rated speed, rated load and $C_{bus} = 400mF$ . . . . .	123
5.126	Neutral point current $i_{NP}$ for Method 2 half rated speed, rated load and $C_{bus} = 400mF$ . . . . .	123
5.127	Line-to-neutral voltage $v_{An}$ for Method 3 rated speed, rated load. . .	125
5.128	FFT of line-to-neutral voltage $v_{An}$ for Method 3 rated speed, rated load.	125
5.129	Line-to-neutral voltage $v_{Bn}$ for Method 3 rated speed, rated load. . .	125
5.130	FFT of line-to-neutral voltage $v_{Bn}$ for Method 3 rated speed, rated load.	125
5.131	Line-to-neutral voltage $v_{Cn}$ for Method 3 rated speed, rated load. . .	125
5.132	FFT of line-to-neutral voltage $v_{Cn}$ for Method 3 rated speed, rated load.	125
5.133	Line-to-line voltage $v_{AB}$ for Method 3 rated speed, rated load. . . . .	127
5.134	FFT of line-to-line voltage $v_{AB}$ for Method 3 rated speed, rated load.	127
5.135	Line-to-line voltage $v_{BC}$ for Method 3 rated speed, rated load. . . . .	127
5.136	FFT of line-to-line voltage $v_{BC}$ for Method 3 rated speed, rated load.	127
5.137	Line-to-line voltage $v_{CA}$ for Method 3 rated speed, rated load. . . . .	127
5.138	FFT of line-to-line voltage $v_{CA}$ for Method 3 rated speed, rated load.	127
5.139	Phase current $i_A$ for Method 3 rated speed, rated load. . . . .	128
5.140	FFT of phase current $i_A$ for Method 3 rated speed, rated load. . . . .	128
5.141	Phase current $i_B$ for Method 3 rated speed, rated load. . . . .	128
5.142	FFT of phase current $i_B$ for Method 3 rated speed, rated load. . . . .	128
5.143	Phase current $i_C$ for Method 3 rated speed, rated load. . . . .	128
5.144	FFT of phase current $i_C$ for Method 3 rated speed, rated load. . . . .	128
5.145	Space vector of line-to-neutral voltages for Method 3 rated speed, rated load. . . . .	130
5.146	Space vector of phase currents for Method 3 rated speed, rated load.	130
5.147	Neutral point current $i_{NP}$ for Method 3 rated speed, rated load. . .	130
5.148	Line-to-neutral voltage $v_{An}$ for Method 3 half rated speed, rated load.	132
5.149	FFT of line-to-neutral voltage $v_{An}$ for Method 3 half rated speed, rated load. . . . .	132

5.150	Line-to-neutral voltage $v_{Bn}$ for Method 3 half rated speed, rated load.	132
5.151	FFT of line-to-neutral voltage $v_{Bn}$ for Method 3 half rated speed, rated load. . . . .	132
5.152	Line-to-neutral voltage $v_{Cn}$ for Method 3 half rated speed, rated load.	132
5.153	FFT of line-to-neutral voltage $v_{Cn}$ for Method 3 half rated speed, rated load. . . . .	132
5.154	Line-to-line voltage $v_{AB}$ for Method 3 half rated speed, rated load. .	134
5.155	FFT of line-to-line voltage $v_{AB}$ for Method 3 half rated speed, rated load. . . . .	134
5.156	Line-to-line voltage $v_{BC}$ for Method 3 half rated speed, rated load. .	134
5.157	FFT of line-to-line voltage $v_{BC}$ for Method 3 half rated speed, rated load. . . . .	134
5.158	Line-to-line voltage $v_{CA}$ for Method 3 half rated speed, rated load. .	134
5.159	FFT of line-to-line voltage $v_{CA}$ for Method 3 half rated speed, rated load. . . . .	134
5.160	Phase current $i_A$ for Method 3 half rated speed, rated load. . . . .	135
5.161	FFT of phase current $i_A$ for Method 3 half rated speed, rated load. .	135
5.162	Phase current $i_B$ for Method 3 half rated speed, rated load. . . . .	135
5.163	FFT of phase current $i_B$ for Method 3 half rated speed, rated load. .	135
5.164	Phase current $i_C$ for Method 3 half rated speed, rated load. . . . .	135
5.165	FFT of phase current $i_C$ for Method 3 half rated speed, rated load. .	135
5.166	Space vector of line-to-neutral voltages for Method 3 half rated speed, rated load. . . . .	137
5.167	Space vector of phase currents for Method 3 half rated speed, rated load.	137
5.168	Neutral point current $i_{NP}$ for Method 3 half rated speed, rated load.	137
A.1	Method 1 switching table Sector I, equivalent two-level sector I. . . .	161
A.2	Method 1 switching table Sector I, equivalent two-level sector II. . .	162
A.3	Method 1 switching table Sector I, equivalent two-level sector III. . .	162
A.4	Method 1 switching table Sector I, equivalent two-level sector IV. . .	163

A.5	Method 1 switching table Sector I, equivalent two-level sector V. . .	163
A.6	Method 1 switching table Sector I, equivalent two-level sector VI. . .	163
A.7	Method 1 switching table Sector II, equivalent two-level sector I. . .	164
A.8	Method 1 switching table Sector II, equivalent two-level sector II. . .	164
A.9	Method 1 switching table Sector II, equivalent two-level sector III. . .	164
A.10	Method 1 switching table Sector II, equivalent two-level sector IV. . .	165
A.11	Method 1 switching table Sector II, equivalent two-level sector V. . .	165
A.12	Method 1 switching table Sector II, equivalent two-level sector VI. . .	165
A.13	Method 1 switching table Sector III, equivalent two-level sector I. . .	166
A.14	Method 1 switching table Sector III, equivalent two-level sector II. . .	166
A.15	Method 1 switching table Sector III, equivalent two-level sector III. . .	166
A.16	Method 1 switching table Sector III, equivalent two-level sector IV. . .	167
A.17	Method 1 switching table Sector III, equivalent two-level sector V. . .	167
A.18	Method 1 switching table Sector III, equivalent two-level sector VI. . .	167
A.19	Method 1 switching table Sector IV, equivalent two-level sector I. . .	168
A.20	Method 1 switching table Sector IV, equivalent two-level sector II. . .	168
A.21	Method 1 switching table Sector IV, equivalent two-level sector III. . .	168
A.22	Method 1 switching table Sector IV, equivalent two-level sector IV. . .	169
A.23	Method 1 switching table Sector IV, equivalent two-level sector V. . .	169
A.24	Method 1 switching table Sector IV, equivalent two-level sector VI. . .	169
A.25	Method 1 switching table Sector V, equivalent two-level sector I. . .	170
A.26	Method 1 switching table Sector V, equivalent two-level sector II. . .	170
A.27	Method 1 switching table Sector V, equivalent two-level sector III. . .	170
A.28	Method 1 switching table Sector V, equivalent two-level sector IV. . .	171
A.29	Method 1 switching table Sector V, equivalent two-level sector V. . .	171
A.30	Method 1 switching table Sector V, equivalent two-level sector VI. . .	171
A.31	Method 1 switching table Sector VI, equivalent two-level sector I. . .	172
A.32	Method 1 switching table Sector VI, equivalent two-level sector II. . .	172
A.33	Method 1 switching table Sector VI, equivalent two-level sector III. . .	172

A.34	Method 1 switching table Sector VI, equivalent two-level sector IV. . .	173
A.35	Method 1 switching table Sector VI, equivalent two-level sector V. . .	173
A.36	Method 1 switching table Sector VI, equivalent two-level sector VI. . .	173
A.37	Method 2 switching table Sector I, equivalent two-level sector I. . . .	174
A.38	Method 2 switching table Sector I, equivalent two-level sector II. . .	174
A.39	Method 2 switching table Sector I, equivalent two-level sector III. . .	174
A.40	Method 2 switching table Sector I, equivalent two-level sector IV. . .	175
A.41	Method 2 switching table Sector I, equivalent two-level sector V. . .	175
A.42	Method 2 switching table Sector I, equivalent two-level sector VI. . .	175
A.43	Method 2 switching table Sector II, equivalent two-level sector I. . .	176
A.44	Method 2 switching table Sector II, equivalent two-level sector II. . .	176
A.45	Method 2 switching table Sector II, equivalent two-level sector III. . .	176
A.46	Method 2 switching table Sector II, equivalent two-level sector IV. . .	177
A.47	Method 2 switching table Sector II, equivalent two-level sector V. . .	177
A.48	Method 2 switching table Sector II, equivalent two-level sector VI. . .	177
A.49	Method 2 switching table Sector III, equivalent two-level sector I. . .	178
A.50	Method 2 switching table Sector III, equivalent two-level sector II. . .	178
A.51	Method 2 switching table Sector III, equivalent two-level sector III. . .	178
A.52	Method 2 switching table Sector III, equivalent two-level sector IV. . .	179
A.53	Method 2 switching table Sector III, equivalent two-level sector V. . .	179
A.54	Method 2 switching table Sector III, equivalent two-level sector VI. . .	179
A.55	Method 2 switching table Sector IV, equivalent two-level sector I. . .	180
A.56	Method 2 switching table Sector IV, equivalent two-level sector II. . .	180
A.57	Method 2 switching table Sector IV, equivalent two-level sector III. . .	180
A.58	Method 2 switching table Sector IV, equivalent two-level sector IV. . .	181
A.59	Method 2 switching table Sector IV, equivalent two-level sector V. . .	181
A.60	Method 2 switching table Sector IV, equivalent two-level sector VI. . .	181
A.61	Method 2 switching table Sector V, equivalent two-level sector I. . .	182
A.62	Method 2 switching table Sector V, equivalent two-level sector II. . .	182

A.63	Method 2 switching table Sector V, equivalent two-level sector III. . .	182
A.64	Method 2 switching table Sector V, equivalent two-level sector IV. . .	183
A.65	Method 2 switching table Sector V, equivalent two-level sector V. . .	183
A.66	Method 2 switching table Sector V, equivalent two-level sector VI. . .	183
A.67	Method 2 switching table Sector VI, equivalent two-level sector I. . .	184
A.68	Method 2 switching table Sector VI, equivalent two-level sector II. . .	184
A.69	Method 2 switching table Sector VI, equivalent two-level sector III. . .	184
A.70	Method 2 switching table Sector VI, equivalent two-level sector IV. . .	185
A.71	Method 2 switching table Sector VI, equivalent two-level sector V. . .	185
A.72	Method 2 switching table Sector VI, equivalent two-level sector VI. . .	185
A.73	Method 3 switching table Sector I, equivalent two-level sector I. . . .	186
A.74	Method 3 switching table Sector I, equivalent two-level sector II. . . .	186
A.75	Method 3 switching table Sector I, equivalent two-level sector III. . . .	186
A.76	Method 3 switching table Sector I, equivalent two-level sector IV. . . .	187
A.77	Method 3 switching table Sector I, equivalent two-level sector V. . . .	187
A.78	Method 3 switching table Sector I, equivalent two-level sector VI. . . .	187
A.79	Method 3 switching table Sector II, equivalent two-level sector I. . . .	188
A.80	Method 3 switching table Sector II, equivalent two-level sector II. . . .	188
A.81	Method 3 switching table Sector II, equivalent two-level sector III. . . .	188
A.82	Method 3 switching table Sector II, equivalent two-level sector IV. . . .	189
A.83	Method 3 switching table Sector II, equivalent two-level sector V. . . .	189
A.84	Method 3 switching table Sector II, equivalent two-level sector VI. . . .	189
A.85	Method 3 switching table Sector III, equivalent two-level sector I. . . .	190
A.86	Method 3 switching table Sector III, equivalent two-level sector II. . . .	190
A.87	Method 3 switching table Sector III, equivalent two-level sector III. . . .	190
A.88	Method 3 switching table Sector III, equivalent two-level sector IV. . . .	191
A.89	Method 3 switching table Sector III, equivalent two-level sector V. . . .	191
A.90	Method 3 switching table Sector III, equivalent two-level sector VI. . . .	191
A.91	Method 3 switching table Sector IV, equivalent two-level sector I. . . .	192

A.92	Method 3 switching table Sector IV, equivalent two-level sector II. . .	192
A.93	Method 3 switching table Sector IV, equivalent two-level sector III. . .	192
A.94	Method 3 switching table Sector IV, equivalent two-level sector IV. . .	193
A.95	Method 3 switching table Sector IV, equivalent two-level sector V. . .	193
A.96	Method 3 switching table Sector IV, equivalent two-level sector VI. . .	193
A.97	Method 3 switching table Sector V, equivalent two-level sector I. . .	194
A.98	Method 3 switching table Sector V, equivalent two-level sector II. . .	194
A.99	Method 3 switching table Sector V, equivalent two-level sector III. . .	194
A.100	Method 3 switching table Sector V, equivalent two-level sector IV. . .	195
A.101	Method 3 switching table Sector V, equivalent two-level sector V. . .	195
A.102	Method 3 switching table Sector V, equivalent two-level sector VI. . .	195
A.103	Method 3 switching table Sector VI, equivalent two-level sector I. . .	196
A.104	Method 3 switching table Sector VI, equivalent two-level sector II. . .	196
A.105	Method 3 switching table Sector VI, equivalent two-level sector III. . .	196
A.106	Method 3 switching table Sector VI, equivalent two-level sector IV. . .	197
A.107	Method 3 switching table Sector VI, equivalent two-level sector V. . .	197
A.108	Method 3 switching table Sector VI, equivalent two-level sector VI. . .	197

## Chapter 1

### Introduction

#### 1.1 Background of the Problem

Two-level voltage source inverters have been widely used in industry for dc to ac power conversion since the early 1960s [1]. However, an increase in the number of high power applications has led to the development of multilevel inverters [2]. In addition to higher power ratings, multilevel inverters produce better quality output voltages which thus improve drive efficiency [3]. Despite the improvements in output quality and power ratings, multilevel inverters beyond the three-level inverter have not been widely adopted due to the increase in design and control complexity as the number of levels increases. Thus, the three-level inverter has received much attention since it produces improved output waveforms over the two-level inverter with only a minor increase in complexity [4].

In an attempt to make multilevel inverters, and in particular three-level inverters, more viable in industry, there has been much research into various control schemes for these inverters. Many of the pulse width modulation (PWM) methods

that have been developed for two-level inverters have been extended to multilevel inverters, including carrier-based PWM (CBPWM) and space vector PWM (SVPWM). Many methods have also been developed that address some of the weaknesses of the major multilevel inverter topologies, particularly the possibility of bus neutral point imbalance. The following section outlines several of the major developments in two-level PWM and multilevel PWM from the last few decades.

## **1.2 Review of Literature**

### **1.2.1 Two-Level PWM**

One of the most basic PWM methods is known as carrier-based PWM, which generates the control pulses by comparing a high frequency carrier signal to a low frequency reference signal. In the simplest version, a sinusoidal reference representing the desired line-to-neutral voltage is compared to a triangular carrier signal. A popular research area for carrier-based PWM is to develop different signals to add to the reference signal. This is known as zero-sequence injection because the injected signal disappears from the line-to-line signals. In [5], sinusoidal PWM with the injection of a third harmonic is analyzed in terms of its voltage harmonic spectrum and its associated harmonic losses. The more general case of non-sinusoidal zero-sequence harmonic injection is also considered. The extension of the linear modulation region of two-level sinusoidal PWM by injecting a rectangular zero-sequence component

is presented in [6]. This method extends the dynamic range of the PWM control and eliminates the need for the overmodulation region since six-step operation may be achieved within the linear modulation region. Another interesting application of carrier-based PWM is presented in [7]. Three-level voltage waveforms are produced using two two-level voltage source inverters with phase-shifted two-level carrier-based PWM.

Beyond carrier-based PWM, space vector PWM has been popular due to its simple digital implementation and its naturally higher possible output voltage in the linear modulation region. In [8], basic two-level space vector PWM theory is explained in detail. The treatment of the switches of a two-level inverter as a binary system is presented, and the concept of a space vector is provided. The representation of a space vector reference signal in terms of the different combinations of conducting switches is developed in detail, and several space vector PWM methods based on these concepts are introduced. The MATLAB Simulink simulation of a common two-level space vector PWM switching pattern for an inverter is presented in [9]. A method for smooth transitions between the linear modulation range and the overmodulation range up to six-step operation in two-level space vector PWM was presented in [10]. In this application, three modes of operation are defined: the linear modulation region, overmodulation mode I, and overmodulation mode II. The linear modulation region corresponds to the reference voltage vector lying completely

within the hexagon formed by the active voltage vectors. Overmodulation mode I corresponds to the reference voltage vector lying within the active voltage vector hexagon for part of the fundamental period and lying outside the active voltage vector hexagon for the remainder of the fundamental period. Overmodulation mode II corresponds to the reference voltage vector lying completely outside the active voltage vector hexagon. The output pulses are generated in the usual fashion within the linear modulation region, but for operation in the two overmodulation modes, the output pulses are generated with the use of a Fourier series expansion. The applied method was shown to reduce the total harmonic distortion of the output voltages in the overmodulation regions compared to traditional methods. In [11], a Fourier series-based analytical development of the harmonic spectra of space vector PWM output voltages is presented. The analytically calculated voltage spectrum is shown to closely match the experimental voltage spectrum found using the Discrete Fourier Transform.

Although the implementation of the two methods is different, it has been shown that carrier-based PWM can create identical switching patterns to those produced from space vector PWM. In [12], carrier-based PWM and space vector PWM are developed independent of load type. It is also shown that carrier-based PWM can produce switching patterns, and thus output waveforms, identical to space vector PWM using a sinusoidal reference with a properly selected zero-sequence signal. The

relationships developed are applicable to space vector PWM methods beyond the basic zero vector distribution. The relationship between carrier-based PWM and space vector PWM is confirmed in [13], which derives the zero-sequence component for carrier-based PWM and compares the output pulses to those from space vector PWM. The results are verified through both simulation and experimentation.

Much work has been done that summarizes and analyzes the wide variety of PWM methods for two-level inverters. In [14], basic PWM performance criteria are introduced, and an analysis of several major PWM schemes including carrier-based PWM, carrierless PWM, and feedback PWM control is provided. Guidelines for PWM method selection based on application type are provided as well. An analysis of PWM methods that minimize common mode voltage was performed in [15]. The cause of common mode voltage at the output of two-level inverters is described, and various space vector PWM techniques that minimize common mode voltage are compared. Several techniques, both analytical and graphical, for the performance evaluation of PWM methods are presented in [16]. Taking advantage of the equivalence between space vector methods and carrier-based methods, ten of the most popular PWM methods are presented in terms of a sinusoidal reference and a zero-sequence injected signal. Using the proposed techniques, the PWM methods are compared based on waveform quality, inverter input current harmonics, and switching losses. It is apparent from the above discussion that two-level PWM is a very broad topic that has received

much attention in the literature over the years.

### 1.2.2 Multilevel PWM

One of the first PWM methods to be adapted to multilevel inverters was carrier-based PWM. This was achieved by using offset carrier signals to control the different levels of switches. The reference signal remained the same. Three different multilevel sinusoidal PWM methods based on the relative phases of the triangular carriers were presented in [17]. In the first method, the phases of carrier signals of different levels are alternately in opposition (APO disposition). In the second method, the carrier signals above the zero reference are all in phase, which are  $180^\circ$  out of phase with the carrier signals below the zero reference (PO disposition). In the third method, all carrier signals are in phase (PH disposition). All three methods are analyzed based on their output harmonic content and their operation in the overmodulation region. In [18], a short analysis of the neutral point imbalance problem in multilevel inverters is provided. A method for balancing the neutral point potential based on injecting an analytically-calculated zero-sequence voltage into the reference is proposed and verified in simulation. However, this method requires knowledge of the power factor of the motor currents. Another method is proposed in [19] that attempts to address this weakness and provide good results for all modes of operation. This method uses measurements of the capacitor voltages and motor currents alone to

generate the injected zero-sequence signal. The method was experimentally verified, and its performance was comparable to space vector PWM. In [20], a carrier-based PWM method for balancing the neutral point voltage was derived using the duality of carrier-based PWM and space vector PWM. This method was shown via simulation and experiment to balance the neutral point voltage while reducing switching power losses compared to other carrier-based PWM methods.

Space vector PWM was also adapted for multilevel inverters. In [21], a multilevel space vector PWM algorithm is developed based on the equations for a two-level space vector PWM inverter. All of the small triangles that form the hexagon of active vectors are classified based on their orientation. Based on their orientation, each triangle is treated as a certain sector in a two-level inverter, and the calculation of dwell times for the voltage vectors may be found. The algorithm is verified experimentally in a five-level inverter. Another approach to implementing multilevel space vector PWM is presented in [22]. In this method, a change of basis is performed to change from an orthogonal coordinate system for the space vectors to a coordinate system that aligns with the active vectors. By projecting the voltage vectors and reference vector into the new coordinate system, the calculation of the dwell times for the voltage vectors is simplified. In [23], a three-level space vector PWM method is proposed which considers the three-level active vector hexagon as a combination of six two-level active vector hexagons. The reference vector is projected into the nearest two-level active

vector hexagon, which allows basic two-level space vector PWM methods to be applied. This method may be extended to higher level inverters as well, though computational complexity increases as the number of levels increases. A space vector PWM algorithm that reduces computation time is presented in [24]. In this algorithm, the three sinusoidal reference signals are not transformed into a reference space vector. Instead, a lookup table based on the relative values of the references is used to determine the sector, and the value of the dwell times of the voltage vectors are written in terms of the values of the references. From experimental results, it was found that the time taken to sample the three reference signals was longer than conventional algorithms, but computation time was improved for sector identification and dwell time calculation. In [25], general guidelines for selecting the switching sequence in a multilevel inverter are provided, and both continuous and discontinuous PWM are discussed. In the case of continuous PWM, it is shown that minimal current distortion occurs when the redundant vector dwell time is split evenly between the redundant vectors. In both [26] and [27], optimized multilevel PWM control strategies are proposed. The creation of the switching sequence by minimizing a cost function representing the flux error is proposed in [26], while in [27] a real-time algorithm is used to generate the PWM sequence that minimizes current total harmonic distortion. Space vector PWM algorithms based on the ability to subdivide sectors of the active vector hexagon structure of a multilevel inverter into smaller triangles are proposed in both [28] and

[29]. A space vector PWM switching pattern that minimizes switching losses for an inverter is presented in [30]. In this switching pattern, the switch in the phase leg that is operating near the maximum and minimum of the current waveform will not change state. In [31], several multilevel space vector PWM switching sequences are proposed. All of the proposed methods use some active vector other than the redundant vector as the repeated vector in the sequence. Some of these sequences produce improved current total harmonic distortion for an induction machine load than the more common switching sequences. A space vector PWM algorithm is proposed in [32] that takes advantage of the symmetry of the desired output waveforms to improve inverter operation at low switching frequencies. In particular, the method was created for a wide variety of ratios of the switching frequency to the fundamental frequency. It was shown through experimentation that this method produces reduced distortion at pulse ratios as low as ten pulses per period. In [33], [34], and [35], multilevel space vector PWM operation was extended into the overmodulation region.

Space vector PWM in closed loop systems has also been heavily investigated. In [36], feedback control is used to adjust the ratio between the redundant vectors in three-level space vector PWM in order to balance the neutral point voltage. The authors concluded that although control of the neutral point voltage is possible to a limited extent on the inverter side of the drive, better control can be achieved through an active rectifier. A hysteresis PWM controller based on space vector PWM is proposed

in [37]. The proposed controller keeps many of the advantages of space vector PWM and gains some of the advantages of hysteresis controllers including a quick dynamic response and simple implementation. In [4], a closed loop multilevel space vector PWM control scheme that stabilizes the neutral point potential is proposed. A switching sequence is used that takes advantages of all redundant vectors, which allows for more flexibility in controlling the neutral point. In the proposed method, the output current polarities and the voltage vector are used to adjust the ratio of the redundant vectors in each switching cycle to minimize neutral point drift. A PWM method is proposed in [38] that combines aspects of space vector PWM and spread spectrum modulation. In this method, a parallel is drawn between the approximation of the reference signals using discrete switching states and oversampling analog to digital conversion. Properties of analog to digital converters are applied to generate the switching patterns of the inverter independent of the switching frequency. The output voltage harmonics produced by this method are spread throughout the frequency spectrum with few distinctive peaks. In [39], a controller using a space vector PWM method generated using artificial neural networks is proposed. The neural network is trained offline on data from a simulated digital signal processing based modulator. Although the results were promising in simulation, as of the time of the authors' work, there was no controller commercially available that could be economically used to implement the method. A method using only three switching states per sampling

period is proposed in [40]. In this method, the output voltages are forced to balance despite neutral point drift. This is achieved by adjusting the values of the active vectors as they drift in the  $(\alpha - \beta)$  plane due to neutral point imbalance. In [41], a different neutral point balancing technique is presented. Linear combinations of the active voltage vectors are produced that do not affect the neutral point balance, and these new vectors, called virtual space vectors, are used to represent the reference vector. Although with this method the neutral point remains balanced, it has several weaknesses including complexity of implementation, higher switching frequency, and higher harmonic distortion. The method proposed in [42] attempts to improve the virtual space vector method. In this method, a controller is created that alternates between the virtual space vector method and the typical space vector method, which reduces the switching frequency. In [43] and [44], a circuit topology that produces eighteen-sided polygonal voltage vectors as opposed to the usual hexagonal voltage vectors is proposed. The eighteen-sided polygon more closely resembles a circle than does the hexagon, which produces output voltages with lower harmonics with proper switching. Two space vector PWM control algorithms for the topology are proposed as well.

As was the case with two-level inverters, it has been shown that the multilevel carrier-based PWM method known as phase disposition PWM (PD-PWM) and multilevel space vector PWM can create the same switching patterns. In [45], the

equivalence of space vector PWM and sinusoidal PWM in three-level inverters is presented by deriving the space vector dwell times that produce pulses identical to sinusoidal PWM. It is also shown that three-level carrier-based PWM can achieve identical results to space vector PWM through proper zero-sequence injection. These results are expanded in [46] to general multilevel inverters including the overmodulation region. A PWM method using both space vector PWM and discontinuous PWM is also proposed. The method was shown to improve the balance of the switching losses among the IGBTs of the inverter. The relationship between space vector PWM and carrier-based PWM for five-level inverters is further investigated in [47]. A PWM method based on three-level space vector PWM and multilevel carrier-based PWM is proposed which maintains many advantages of multilevel space vector PWM while gaining the ease of implementation of multilevel carrier-based PWM. In [48], three carrier-based PWM algorithms and two space vector PWM algorithms are compared for a three-level five-phase inverter. The performance of each method is classified based on voltage and current quality, common mode voltage, and algorithm complexity. Of the five methods investigated, one space vector PWM method is shown to produce identical results to one carrier-based PWM method. A quantitative comparison of three PWM techniques for three-level inverters is presented in [49]. Included in the analysis are phase disposition PWM, switching-loss minimization PWM, and selective harmonic elimination PWM. Long cable effects are also investigated for each of the

three methods. In [50], two PWM methods for active NPC inverters are analyzed based on the distribution of the power losses among the IGBTs, and a third PWM method called Adjustable Losses Distribution is proposed. The intent of this method is to balance the power losses evenly among all of the IGBTs in the inverter. The method, which was verified in simulation, was shown to balance the loss distribution for many values of power factor and modulation index.

In an effort to increase the viability of higher level inverters through lower hardware cost and complexity, the multilevel-clamped multilevel inverter has been proposed in recent years [51]. In this multilevel inverter topology, dedicated switching units are used to create the various output voltage levels. This arrangement reduces the number of components in the inverter. Though the hardware complexity of this topology is reduced, the control methods applied to other multilevel inverter topologies are not directly applicable to multilevel-clamped multilevel inverters. This is because the number of active voltage vectors of this topology is reduced as well. In [52], one example of a space vector PWM algorithm for multilevel-clamped multilevel inverters is presented. This method is similar to the virtual vector method discussed previously. The missing active vectors are represented as linear combinations of existing active vectors. The inverter is then controlled in the same manner as the multilevel NPC inverter using these virtual vectors and the existing active vectors.

### 1.3 Statement of the Problem

Although much work exists on space vector PWM methods, little investigation exists for different switching sequences and inverters with permanent magnet (PM) machine loads. In this thesis, three space vector PWM switching sequences found in the literature for three-level NPC inverters ([4], [25], [31]) are simulated with a PM machine load. To gain insight into the inherent qualities of each of the three switching sequences, only open loop control is considered in this investigation. The use of a PM machine load shows some of the effects of the presence of a fixed back emf on the different space vector modulation methods. Simulation results are presented for rated speed, rated load and half speed, rated load conditions. The three methods are compared based on their output voltage quality, their output current quality, and their neutral point current.

## Chapter 2

### Theoretical Development of Two-Level Inverters and SVPWM

This chapter presents an introduction to several two-level inverter topologies as well as a theoretical development of two-level space vector PWM (SVPWM), also called space vector modulation (SVM). Section 2.1 introduces the basic two-level inverter topologies. Section 2.2 presents the theoretical development of the basic two-level SVPWM method.

#### 2.1 Two-Level Inverters

A dc-ac converter, or inverter, is an electric circuit that converts dc voltages and currents to ac voltages and currents through the use of semiconductor switches [53]. The basic two-level, three-phase inverter, presented in Figure 2.1, consists of three branches of two series-connected switches. Each branch produces a single phase (A, B, or C) of the output signal. The input is a dc bus with a voltage of  $V_{bus}$ , with a positive rail P and a negative rail N. The point O is the neutral point of the dc bus. The three-phase output is generated through proper sequencing of conducting periods

and open periods of the switches in each phase. It is important to note that only one switch in each phase may conduct at any given moment to prevent short-circuiting the dc bus. However, both switches may remain open at the same moment.

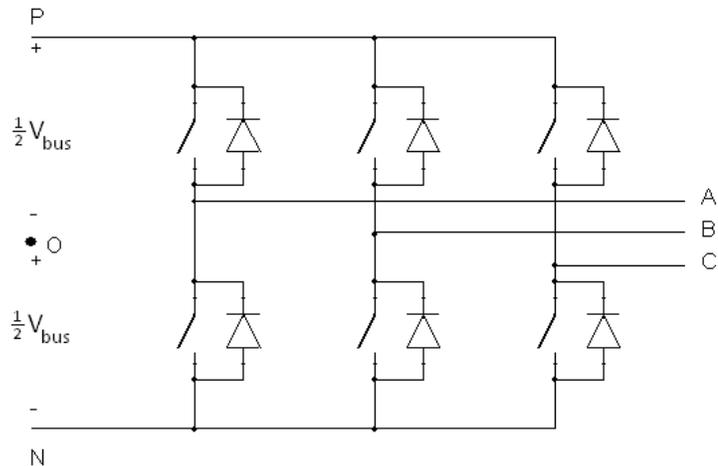


Figure 2.1: Generic two-level, three-phase inverter.

There are two primary classes of three-phase inverters: voltage source/stiff inverters and current source/stiff inverters. If the dc side of an inverter is produced from some type of source that does not change with load such as a battery, it is called a voltage/current “source” inverter. Likewise, if the dc side of an inverter is produced from some sort of temporary energy storage component such as a capacitor or inductor, it is called a voltage/current “stiff” inverter [53]. The stiff designation indicates that the component resists changes to the dc bus, but its value may be affected under heavy load conditions [53].

A voltage source inverter converts the dc bus to ac by properly controlling the

switches so that each phase is sequentially connected to the positive and negative rails of the dc bus, which produces time-varying voltage pulses at the load independent of the load current. The basic two-level voltage source inverter topology is shown in Figure 2.2. There are a few differences between this topology and the generic three-phase inverter presented in Figure 2.1 previously. The main difference is that the ideal switches of the generic inverter have been replaced with the parallel combination of an IGBT and an antiparallel diode. Unlike ideal switches, IGBTs have short, but not instantaneous, switching speeds that may differ between the IGBT transitioning from conducting to open or vice versa. To avoid short-circuiting the dc bus, a short dead time that accounts for the switching speed of the IGBTs should be allowed between switching the top and bottom IGBTs within a phase. The antiparallel diodes behave similarly to the freewheeling diode of buck and boost converters, essentially preventing an instantaneous change in the load current for inductive loads during the dead time at the switching transitions within each phase [54].

Beyond the basic voltage source inverter discussed here, there are several variations on this basic topology as well as techniques to design these inverters for specific design objectives [55]. Many of these variations simply include some sort of circuitry which allows control of the value of the dc bus. A detailed discussion about these variations is beyond the scope of this thesis.

Voltage source/stiff inverters are among the most commonly selected inverter

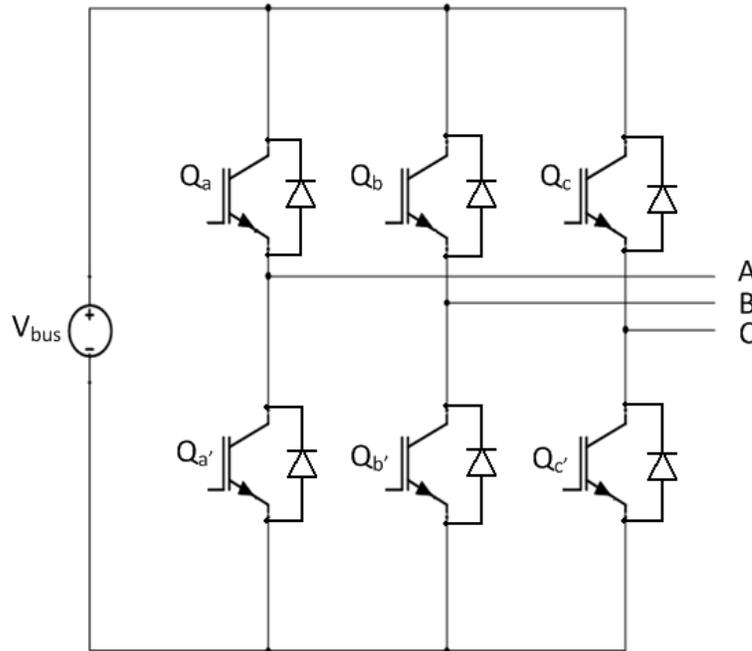


Figure 2.2: Basic two-level voltage source inverter.

types for electric drives. However, it has a dual topology based on a current source producing the dc component in the inverter. A short discussion about current source/stiff inverters is provided for completeness, but only voltage source inverters will be considered in detail in this thesis.

The current source inverter is similar to the voltage source inverter, except that instead of producing time-varying voltage pulses at the load, it produces time-varying current pulses through the load independent of load voltage. The basic two-level current source inverter topology is shown in Figure 2.3. Again, there are a few major differences between this topology and the generic three-phase inverter presented in

Figure 2.1. Here, each ideal switch is replaced with a series-connected IGBT and diode with a second diode antiparallel to the series combination. The additional series-connected diode protects the IGBT from voltage spikes that occur at the switching transitions caused by the high current transients, assuming a predominantly inductive load such as a motor. If allowed to pass that diode, the voltage spikes could force the IGBT to become reverse biased [56]. The antiparallel diode performs the same function as in the voltage source inverter topology.

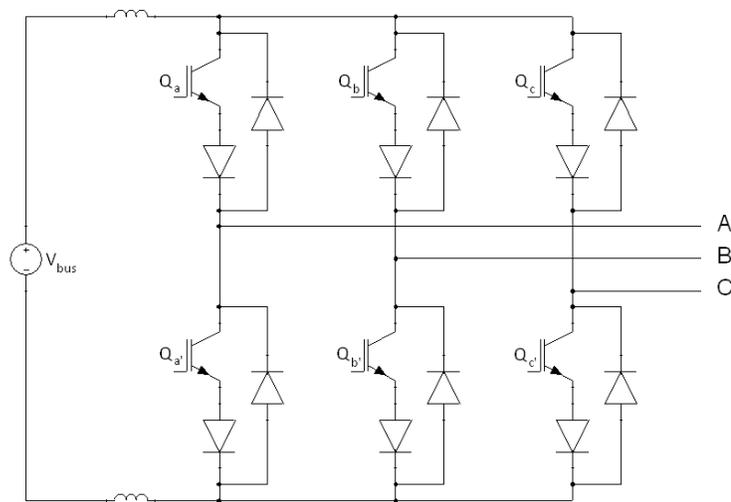


Figure 2.3: Basic two-level current source inverter.

Over the years, there have been many methods for controlling two-level inverters. One of the earliest and most basic methods controlled the switches in each inverter leg so that in each phase a rectangular wave with an amplitude of the dc bus voltage

at the fundamental frequency was produced [57]. The six distinct switching intervals led to inverters implementing this method being called six-step inverters. Since the generated output voltage is essentially a rectangular wave, this method naturally produces a large number of harmonics beyond the fundamental. For a machine load, this results in poor output waveform quality and thus stresses the machine through additional torque pulsations and increased ohmic and core losses [58]. Concerns about this poor waveform quality led to the development of several methods for shortening the lengths of the long pulses by using a series of shorter pulses with the same rms value, such as in fixed width modulation. One class of methods that produces better harmonic results is the set of pulse width modulation (PWM) methods. Some of these methods include carrier-based PWM, selected harmonic elimination (SHE) PWM, and random PWM (RPWM) [58]. Each of these types of PWM methods have their own advantages and disadvantages. One of the most widely used type of PWM methods is known as space vector PWM (SVPWM) (or more simply space vector modulation), which offers many advantages in digital implementation. Space vector modulation is developed more fully in the following section.

## **2.2 Two-Level Space Vector PWM**

Recall the basic two-level voltage source inverter topology presented in Figure 2.2. Since both switches within a single phase may not conduct at the same time

without short-circuiting the dc bus, the top and bottom switches within a phase may be taken as complementary with a short dead time as discussed previously, similar to  $180^\circ$  conduction in a six-step inverter. Thus, instead of having six independent switches, there are only three independent switches. The state of each bottom switch is determined by the state of the top switch in that phase. Each top switch has two possible states, ON or OFF, which produces a total of eight different switching states,  $S_0$  through  $S_7$ , which are presented in Table 2.1. Here, the number “1” corresponds to a switch in its ON state, and the number “0” corresponds to a switch in its OFF state.

	$Q_a$	$Q_b$	$Q_c$
$S_0$	0	0	0
$S_1$	1	0	0
$S_2$	1	1	0
$S_3$	0	1	0
$S_4$	0	1	1
$S_5$	0	0	1
$S_6$	1	0	1
$S_7$	1	1	1

Table 2.1: State table representing all switching combinations.

Each switching state produces a set of line-to-line voltages that is independent of the load type [12]. Thus, for ease of derivation, a balanced Y-connected load will be assumed. The line-to-neutral voltages for each phase are found using voltage division for each switching state. For example, in the case of the switching state  $S_1 = (1\ 0\ 0)$ , the switches  $Q_a$ ,  $Q_{b'}$ , and  $Q_{c'}$  are conducting, and the switches  $Q_{a'}$ ,  $Q_b$ , and  $Q_c$  are

open. This produces an equivalent circuit such as in Figure 2.4, where  $Z_{phase}$  is the load impedance within each phase. In this case, the phase A load impedance is in series with the parallel combination of the phase B and phase C load impedances. Using this information, the line-to-neutral load voltages may be found as follows

$$v_{An} = V_{bus} \cdot \frac{Z_{phase}}{Z_{phase} + \frac{1}{2}Z_{phase}} = \frac{2}{3}V_{bus} \quad (2.1)$$

$$v_{Bn} = v_{Cn} = -V_{bus} \cdot \frac{\frac{1}{2}Z_{phase}}{\frac{1}{2}Z_{phase} + Z_{phase}} = -\frac{1}{3}V_{bus} \quad (2.2)$$

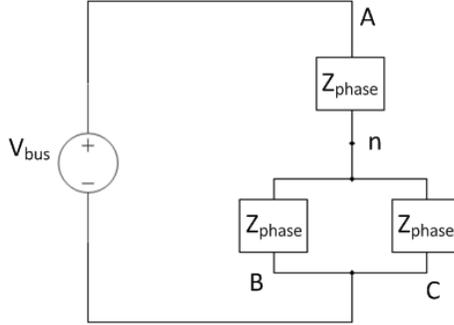


Figure 2.4: The equivalent load circuit for a switching state of  $S_1 = (1\ 0\ 0)$ .

The remaining line-to-neutral voltages may be found in a similar fashion. The line-to-line voltages are then found from the line-to-neutral voltages. For example, the line-to-line voltage  $v_{AB}$  may be found as  $v_{AB} = v_{An} - v_{Bn}$ . The complete set of voltages for each switching state are presented in Table 2.2.

The line-to-neutral voltages associated with each switching state may be

	$v_{An}$	$v_{Bn}$	$v_{Cn}$	$v_{AB}$	$v_{BC}$	$v_{CA}$
$S_0$	0	0	0	0	0	0
$S_1$	$\frac{2}{3}V_{bus}$	$-\frac{1}{3}V_{bus}$	$-\frac{1}{3}V_{bus}$	$V_{bus}$	0	$-V_{bus}$
$S_2$	$\frac{1}{3}V_{bus}$	$\frac{1}{3}V_{bus}$	$-\frac{2}{3}V_{bus}$	0	$V_{bus}$	$-V_{bus}$
$S_3$	$-\frac{1}{3}V_{bus}$	$\frac{2}{3}V_{bus}$	$-\frac{1}{3}V_{bus}$	$-V_{bus}$	$V_{bus}$	0
$S_4$	$-\frac{2}{3}V_{bus}$	$\frac{1}{3}V_{bus}$	$\frac{1}{3}V_{bus}$	$-V_{bus}$	0	$V_{bus}$
$S_5$	$-\frac{1}{3}V_{bus}$	$-\frac{1}{3}V_{bus}$	$\frac{2}{3}V_{bus}$	0	$-V_{bus}$	$V_{bus}$
$S_6$	$\frac{1}{3}V_{bus}$	$-\frac{2}{3}V_{bus}$	$\frac{1}{3}V_{bus}$	$V_{bus}$	$-V_{bus}$	0
$S_7$	0	0	0	0	0	0

Table 2.2: Voltages corresponding to the various switching states in Volts.

compactly represented using space vector notation. The space vector transform is presented in Equation 2.3. Note that the space vector transform presented here is equivalent to the  $(\alpha - \beta)$  transform [59] presented in Equation 2.4 when the  $\alpha$  component is plotted along the real axis and the  $\beta$  component is plotted along the imaginary axis. The space vector transform may be considered polar form while the  $(\alpha - \beta)$  transform may be considered rectangular form.

$$\bar{V} = \frac{2}{3}(v_{An} + av_{Bn} + a^2v_{Cn}), \quad \text{where } a = e^{j\frac{2\pi}{3}} \quad (2.3)$$

$$\begin{aligned} V_\alpha &= \frac{2}{3}v_A - \frac{1}{3}v_B - \frac{1}{3}v_C \\ V_\beta &= \frac{\sqrt{3}}{3}v_B - \frac{\sqrt{3}}{3}v_C \\ V_\gamma &= \frac{1}{3}v_A + \frac{1}{3}v_B + \frac{1}{3}v_C \end{aligned} \quad (2.4)$$

The  $(\alpha - \beta)$  transformation may be condensed in matrix form as follows:

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_\gamma \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} \quad (2.5)$$

Applying the space vector transform to the line-to-neutral switching voltages produces eight voltage vectors corresponding to the eight switching states. These vectors are presented in both polar form and rectangular form in Table 2.3. The nonzero vectors  $\bar{V}_1$  through  $\bar{V}_6$  are called active vectors because they correspond to nonzero output phase voltages. Likewise, the two remaining vectors  $\bar{V}_0$  and  $\bar{V}_7$  are called zero vectors because they correspond to zero output voltage. The set of voltage vectors compactly represents the possible output phase voltages the inverter can produce.

	Polar Form	Rectangular Form
$\bar{V}_0$	0	0
$\bar{V}_1$	$\frac{2}{3}V_{bus}e^{j0}$	$\frac{2}{3}V_{bus}$
$\bar{V}_2$	$\frac{2}{3}V_{bus}e^{j\pi/3}$	$\frac{1}{3}V_{bus} + j\frac{\sqrt{3}}{3}V_{bus}$
$\bar{V}_3$	$\frac{2}{3}V_{bus}e^{j2\pi/3}$	$-\frac{1}{3}V_{bus} + j\frac{\sqrt{3}}{3}V_{bus}$
$\bar{V}_4$	$\frac{2}{3}V_{bus}e^{j\pi}$	$-\frac{2}{3}V_{bus}$
$\bar{V}_5$	$\frac{2}{3}V_{bus}e^{j4\pi/3}$	$-\frac{1}{3}V_{bus} - j\frac{\sqrt{3}}{3}V_{bus}$
$\bar{V}_6$	$\frac{2}{3}V_{bus}e^{j5\pi/3}$	$\frac{1}{3}V_{bus} - j\frac{\sqrt{3}}{3}V_{bus}$
$\bar{V}_7$	0	0

Table 2.3: Switching voltages in space vector form.

By plotting the voltage vectors in the  $(\alpha - \beta)$  plane as in Figure 2.5, the relationship between the different voltage vectors may easily be seen. All six active voltage vectors have the same magnitude, and adjacent vectors are spaced at an angle

of  $60^\circ$  electrical. The two zero vectors have a magnitude of zero and lie at the origin. A hexagon is formed by connecting the tips of the active vectors as seen in Figure 2.5. Each adjacent pair of active vectors can be seen as the boundaries of an equilateral triangle, which is called a sector. There are six sectors in all, labeled I through VI. The area within each sector represents the set of average output voltages that can be produced over some period of time by the inverter using a linear combination of the two active vectors that form the sector boundary and the zero vectors.

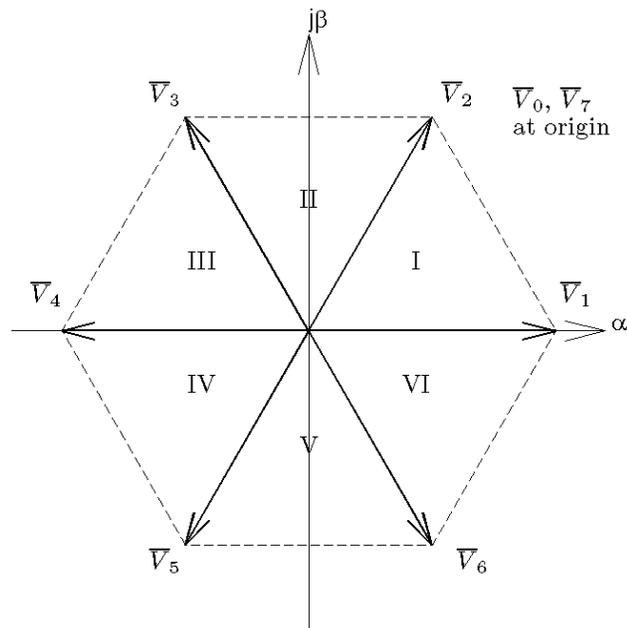


Figure 2.5: The voltage vectors plotted in the  $(\alpha - \beta)$  plane.

Create three balanced sinusoidal positive sequence 3-phase signals representing

the desired fundamental output line-to-neutral voltage as defined in Equation 2.6. The magnitude  $V_{ref}$  of the three sinusoidal references is equal to the desired output line-to-neutral voltage peak. The frequency of the reference signals  $\omega_e = 2\pi f_{fundamental}$  is equal to the desired output frequency in electrical radians per second (e.rad/s), and  $f_{fundamental}$  is the desired output frequency in Hertz. The term  $\phi$  is a general relative phase shift in electrical radians that may be applied to the signals.

$$\begin{aligned} v_{A,ref} &= V_{ref} \cos(\omega_e t + \phi) \\ v_{B,ref} &= V_{ref} \cos(\omega_e t + \phi - 2\pi/3) \\ v_{C,ref} &= V_{ref} \cos(\omega_e t + \phi - 4\pi/3) \end{aligned} \quad (2.6)$$

Applying the space vector transform to the three reference signals produces a reference space vector  $\bar{V}_{ref}$  rotating in the  $(\alpha - \beta)$  plane with an angular speed of  $\omega_e$  e.rad/s and an angular position of  $\theta$  radians as defined in Equation 2.7.

$$\bar{V}_{ref} = V_{ref} e^{j\theta}, \quad \text{where } \theta = \omega_e t + \phi \quad (2.7)$$

Figure 2.6 presents the reference vector in the  $(\alpha - \beta)$  plane along with the previously mentioned eight voltage vectors. To generate the desired fundamental output voltage, a sufficiently small sampling period  $T_s$  is chosen over which the rotating reference vector may be approximated as fixed in the  $(\alpha - \beta)$  plane. Generally, the sampling period is much smaller than the fundamental period of the reference vector; some common values for the sampling period are one thirty-third or one thirty-ninth

of the period of the fundamental frequency [53].

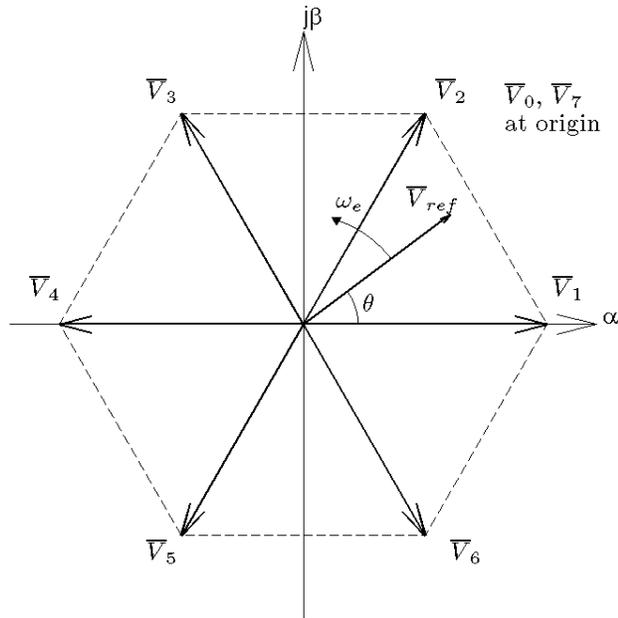


Figure 2.6: The reference space vector with the voltage vectors in the  $(\alpha - \beta)$  plane.

As long as the reference vector lies within the hexagon formed by the voltage vectors, it may be exactly represented as its sampled value using a linear combination of the two nearest active vectors and the zero vectors over some period of time. This is known as the linear modulation region, which is the focus of this thesis. For sinusoidal references, the reference vector traces a circle in the  $(\alpha - \beta)$  plane. Thus, the radius of the largest circle that can be inscribed in the hexagon marks the upper limit of the linear modulation region. Geometrically, this circle has a radius equal to the height of the equilateral triangles that form the sectors as seen in Figure 2.7. From basic

trigonometry, the maximum reference magnitude in the linear modulation region can be calculated as  $\frac{1}{\sqrt{3}}V_{bus}$ .

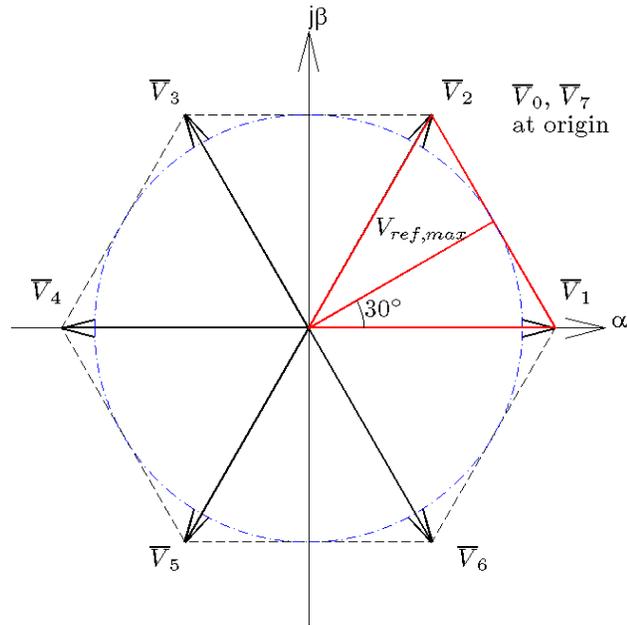


Figure 2.7: The maximum reference vector magnitude for linear modulation in the  $(\alpha - \beta)$  plane.

If the reference vector extends beyond the hexagon, it cannot be represented exactly within a single sampling period. In this case, the magnitude of the reference vector is reduced until the reference lies on the hexagon boundary. When the reference vector extends beyond the hexagon boundary in whole or in part, the inverter enters the overmodulation region. The overmodulation region extends from a reference vector magnitude of  $(\frac{1}{\sqrt{3}}V_{bus})$  to  $\frac{2}{3}V_{bus}$ . The upper limit of the overmodulation region

produces output voltages identical to the  $180^\circ e$  conduction in a six-step inverter, and the reference vector traces the border of the hexagon. Inverter operation in the overmodulation region has several advantages and disadvantages, but this is beyond the scope of this thesis. For more information on overmodulation operation, see references [10], [14], and [53].

As stated previously, in the linear modulation region, the reference vector at each sampling point may be represented over a sampling period as a linear combination of the two nearest active voltage vectors and the zero vectors. For instance, in Sector I,

$$\bar{V}_{ref} = \frac{T_1}{T_s}\bar{V}_1 + \frac{T_2}{T_s}\bar{V}_2 + \frac{T_0}{T_s}\bar{V}_0 + \frac{T_7}{T_s}\bar{V}_7 \quad (2.8)$$

where  $\frac{T_1}{T_s}$  is the fraction of the sampling period that the voltage vector  $\bar{V}_1$  is selected,  $\frac{T_2}{T_s}$  is the fraction of the sampling period that the voltage vector  $\bar{V}_2$  is selected,  $\frac{T_0}{T_s}$  is the fraction of the sampling period that  $\bar{V}_0$  is selected, and  $\frac{T_7}{T_s}$  is the fraction of the sampling period that  $\bar{V}_7$  is selected. The inverter stays in the switching states corresponding to each of the voltage vectors according to the fractions of the sampling period, which when averaged over the switching period, creates the desired output voltage. However, the zero vectors  $\bar{V}_0$  and  $\bar{V}_7$  have no magnitude and thus do not contribute to representing the reference vector. They simply fill any remaining portion

of the sampling period not used by the two active vectors. Thus Equation 2.8 may be rewritten as follows:

$$\bar{V}_{ref} = \frac{T_1}{T_s} \bar{V}_1 + \frac{T_2}{T_s} \bar{V}_2 \quad (2.9)$$

Equation 2.9 is written in polar form with two unknowns  $T_1$  and  $T_2$ . However, by converting the equation to rectangular form and equating the real components and equating the imaginary components, a system of two equations and two unknowns is produced as in Equation 2.10 and Equation 2.11.

$$V_{ref} \cos(\theta) = \frac{T_1}{T_s} \cdot \frac{2}{3} V_{bus} \cos(0) + \frac{T_2}{T_s} \cdot \frac{2}{3} V_{bus} \cos\left(\frac{\pi}{3}\right) \quad (2.10)$$

$$V_{ref} \sin(\theta) = \frac{T_1}{T_s} \cdot \frac{2}{3} V_{bus} \sin(0) + \frac{T_2}{T_s} \cdot \frac{2}{3} V_{bus} \sin\left(\frac{\pi}{3}\right) \quad (2.11)$$

This system may be solved by first finding  $T_2$  from Equation 2.11 as follows:

$$V_{ref} \sin(\theta) = \frac{T_1}{T_s} \cdot \frac{2}{3} V_{bus} \sin(0) + \frac{T_2}{T_s} \cdot \frac{2}{3} V_{bus} \sin\left(\frac{\pi}{3}\right) \quad (2.12)$$

Hence,

$$3T_s V_{ref} \sin(\theta) = 2T_2 V_{bus} \cdot \frac{\sqrt{3}}{2} \quad (2.13)$$

Thus,

$$T_2 = \sqrt{3} \frac{V_{ref}}{V_{bus}} T_s \sin(\theta) \quad (2.14)$$

By substituting  $T_2$  into Equation 2.10,  $T_1$  may also be found as follows:

$$V_{ref} \cos(\theta) = \frac{T_1}{T_s} \cdot \frac{2}{3} V_{bus} \cos(0) + \frac{T_2}{T_s} \cdot \frac{2}{3} V_{bus} \cos\left(\frac{\pi}{3}\right) \quad (2.15)$$

Hence,

$$3T_s V_{ref} \cos(\theta) = 2T_1 V_{bus} + 2T_2 V_{bus} \cdot \frac{1}{2} \quad (2.16)$$

$$T_1 = \frac{3T_s V_{ref} \cos(\theta) - T_2 V_{bus}}{2V_{bus}} \quad (2.17)$$

$$T_1 = \frac{3}{2} \frac{V_{ref}}{V_{bus}} T_s \cos(\theta) - \frac{1}{2} T_2 \quad (2.18)$$

Thus, substituting Equation 2.14 into Equation 2.18 yields the following

$$T_1 = \frac{\sqrt{3}}{2} \frac{V_{ref}}{V_{bus}} T_s \left( \sqrt{3} \cos(\theta) - \sin(\theta) \right) \quad (2.19)$$

To further simplify  $T_1$ , the following trigonometric identity must be applied:

$$a \sin x + b \cos x = \sqrt{a^2 + b^2} \sin(x + \psi) \quad (2.20)$$

where

$$\psi = \begin{cases} \arcsin\left(\frac{b}{\sqrt{a^2 + b^2}}\right), & \text{if } a \geq 0 \\ \pi - \arcsin\left(\frac{b}{\sqrt{a^2 + b^2}}\right), & \text{if } a < 0 \end{cases} \quad (2.21)$$

Accordingly,  $T_1$  may be simplified as follows:

$$T_1 = \frac{\sqrt{3} V_{ref}}{2 V_{bus}} T_s \left( \sqrt{3} \cos(\theta) - \sin(\theta) \right) \quad (2.22)$$

$$= \frac{\sqrt{3} V_{ref}}{2 V_{bus}} T_s \cdot \sqrt{4} \sin \left( \theta + \pi - \arcsin \left( \frac{\sqrt{3}}{\sqrt{4}} \right) \right) \quad (2.23)$$

Hence,

$$T_1 = \sqrt{3} \frac{V_{ref}}{V_{bus}} T_s \sin \left( \theta + \pi - \frac{\pi}{3} \right) \quad (2.24)$$

or

$$T_1 = \sqrt{3} \frac{V_{ref}}{V_{bus}} T_s \sin \left( \frac{\pi}{3} - \theta \right) \quad (2.25)$$

The times corresponding to the zero vectors is found by subtracting  $T_1$  and  $T_2$  from  $T_s$ . The remaining time is divided between  $T_0$  and  $T_7$ . The division of the remaining time between  $\bar{V}_0$  and  $\bar{V}_7$  allows for different space vector modulation methods to be produced by adjusting the ratio of  $T_0$  to  $T_7$ , though one of the most common divisions is to equate  $T_0$  and  $T_7$ . Reference [8] provides a more detailed description of several common zero vector divisions.

The linear combination of active vectors representing the reference vector may be found in the same fashion for any of the remaining sectors as well. It is simple to develop generalized equations for the two times associated with the selected voltage vectors in each sector. Let  $u \in \{1, 2, 3, 4, 5, 6\}$  represent one of the six sectors, where  $u = 1$  represents sector I,  $u = 2$  represents sector II, and so forth, up to  $u = 6$

representing sector VI. Also, let  $v$  represent the sector immediately following  $u$  when rotating counterclockwise in the  $(\alpha - \beta)$  plane. For example, if  $u = 1$ , then  $v = 2$ , and if  $u = 6$ , then  $v$  loops back around so that  $v = 1$ . The equations for the times in the active states may be generalized for a reference vector within any sector  $u$  as follows:

$$T_u = \sqrt{3} \frac{V_{ref}}{V_{bus}} T_s \sin \left( u \frac{\pi}{3} - \theta \right) \quad (2.26)$$

and

$$T_v = \sqrt{3} \frac{V_{ref}}{V_{bus}} T_s \sin \left( (u + 2) \frac{\pi}{3} - \theta \right) \quad (2.27)$$

For clarity in writing these expressions, the terms  $V_{ref}$  and  $V_{bus}$  are often replaced by a term referred to as the modulation index  $m$ . The concept of a modulation index was originally developed for sinusoidal PWM, in which the modulation index is defined as the ratio between the magnitude of the reference signal and the magnitude of the carrier signal. In the linear modulation region of sinusoidal PWM, the modulation index is bounded between the values of 0 and 1. A similar definition may be used in space vector modulation. Here, the space vector modulation index is defined as follows:

$$m = 2 \frac{V_{ref}}{V_{bus}} \quad (2.28)$$

Then Equation 2.26 and Equation 2.27 may be rewritten in terms of the

modulation index as follows:

$$T_u = \frac{\sqrt{3}}{2} m T_s \sin \left( u \frac{\pi}{3} - \theta \right) \quad (2.29)$$

and

$$T_v = \frac{\sqrt{3}}{2} m T_s \sin \left( (u + 2) \frac{\pi}{3} - \theta \right) \quad (2.30)$$

Recall that previously, it was stated that the maximum reference vector magnitude is  $V_{ref,max} = \frac{1}{\sqrt{3}} V_{bus}$ . This may be used to find the maximum modulation index  $m_{max}$  by substituting  $V_{ref,max}$  into Equation 2.28:

$$m_{max} = 2 \frac{V_{ref,max}}{V_{bus}} \quad (2.31)$$

$$= 2 \frac{\frac{1}{\sqrt{3}} V_{bus}}{V_{bus}} \quad (2.32)$$

$$= \frac{2}{\sqrt{3}} \approx 1.155 \quad (2.33)$$

Note that the maximum modulation index available in the linear modulation region of space vector modulation is approximately 1.155, which is 15.5% larger than the maximum modulation index in the linear region of sinusoidal PWM. This indicates that space vector modulation is able to produce a larger fundamental output voltage than sinusoidal PWM. This is one important advantage space vector modulation has

over traditional sinusoidal PWM.

With Equation 2.29 and Equation 2.30, the general expression for the reference vector in any sector  $u$  may be written as:

$$\bar{V}_{ref} = \frac{T_u}{T_s} \bar{V}_u + \frac{T_v}{T_s} \bar{V}_v + \frac{T_0}{T_s} \bar{V}_0 + \frac{T_7}{T_s} \bar{V}_7 \quad (2.34)$$

However, this expression provides no information on the order in which the four voltage vectors, and their corresponding switching states, should be selected. It is well-known in the literature [8], [13], [53], that when selecting the order of the switching states within a sampling period, the designer should avoid more than one inverter leg changing between 0 and 1 during any transition between switching states. This helps minimize switching losses by minimizing the output switching frequency. For instance, in the transition from  $S_1 = (1\ 0\ 0)$  to  $S_2 = (1\ 1\ 0)$ , only the switching state associated with the phase B leg changes from 0 to 1 while the switching states associated with the phase A and phase C legs remain the same. In contrast, in the transition from  $S_2 = (1\ 1\ 0)$  to  $S_0 = (0\ 0\ 0)$ , both switching states associated with phase A and phase B change. The second case would have higher switching losses because more switching actions in the IGBTs occur in this case than the first. Similarly, centering the high pulses within a sampling period for each phase leg minimizes the harmonic distortion of the inverter currents [12],[53]. To meet these conditions, the pattern of

the switching states is often performed once in the first half of the sampling period and then reversed for the second half of the sampling period, and  $T_0$  is set equal to  $T_7$ . For example, the switching state pattern in each sampling period of sector I is  $S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_7 \rightarrow S_2 \rightarrow S_1 \rightarrow S_0$ , where  $S_7$  is centered in the sampling period.

Figure 2.8 through Figure 2.13 present the division of the switching states within each sampling period for each of the six sectors as well as a representation of the IGBT control signals for each phase leg of the inverter. In each sector, only one leg changes state at a time, and the sampling period always begins in the switching state  $S_0 = (0\ 0\ 0)$  to ensure a smooth transition between sectors.

When these switching patterns are implemented in an inverter with an R-L, Y-connected load, the line-to-line voltages and the line-to-neutral voltages follow a distinctive pattern. These patterns are shown in Figure 2.14 and Figure 2.15 which demonstrate typical line-to-line and line-to-neutral voltages. In this example, the modulation index is equal to 1.089, which corresponds to a reference magnitude of  $0.5443V_{bus}$ . The voltages are scaled by the bus voltage, and time is scaled by the fundamental period. The line-to-line voltage switches between  $-V_{bus}$ , 0, and  $V_{bus}$ , while the line-to-neutral voltage assumes values of  $\pm\frac{1}{3}V_{bus}$ ,  $\pm\frac{2}{3}V_{bus}$ , and 0.

Typical phase currents for an R-L load are shown in Figure 2.16. Again, time has been scaled by the fundamental period of the signal, and the current magnitude was scaled by the amplitude of the fundamental current. This figure shows that space

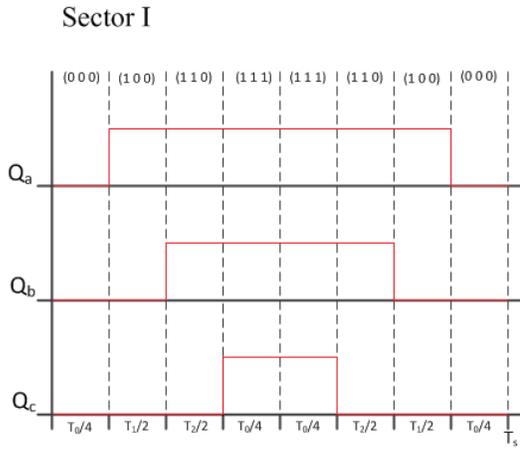


Figure 2.8: The division of the switching states in Sector I.

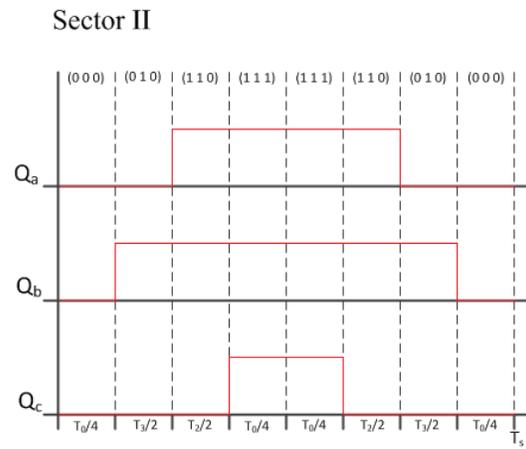


Figure 2.9: The division of the switching states in Sector II.

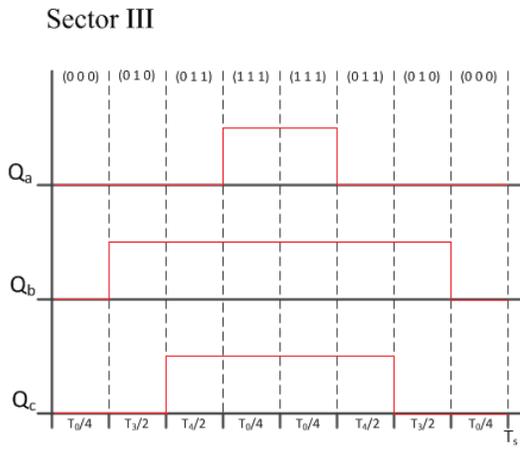


Figure 2.10: The division of the switching states in Sector III.

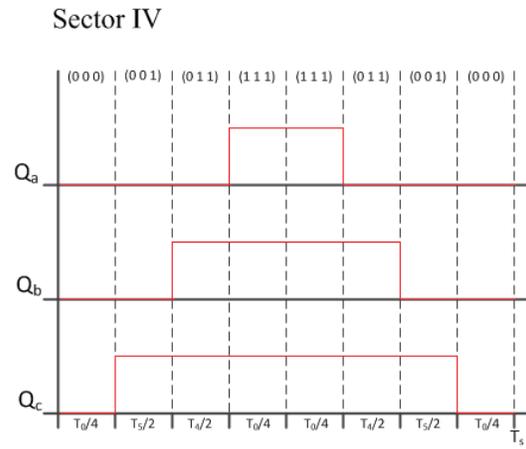


Figure 2.11: The division of the switching states in Sector IV.

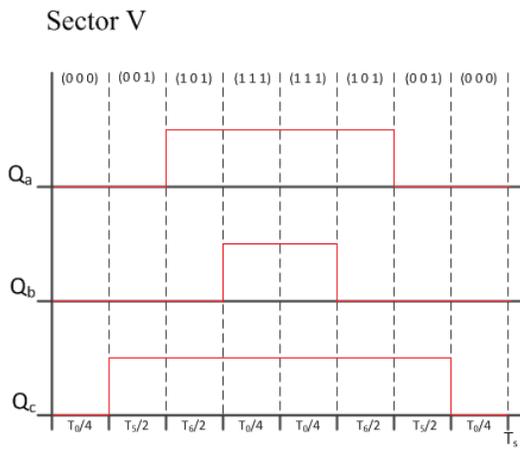


Figure 2.12: The division of the switching states in Sector V.

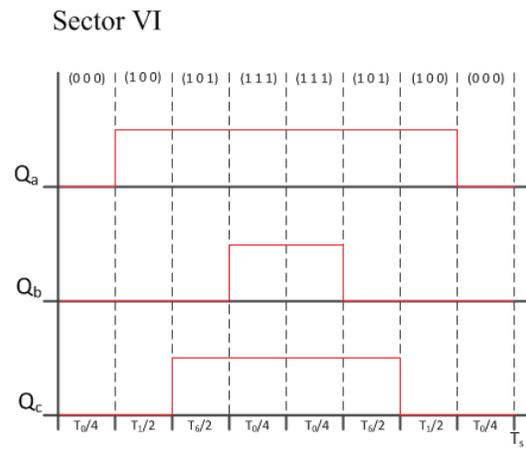


Figure 2.13: The division of the switching states in Sector VI.

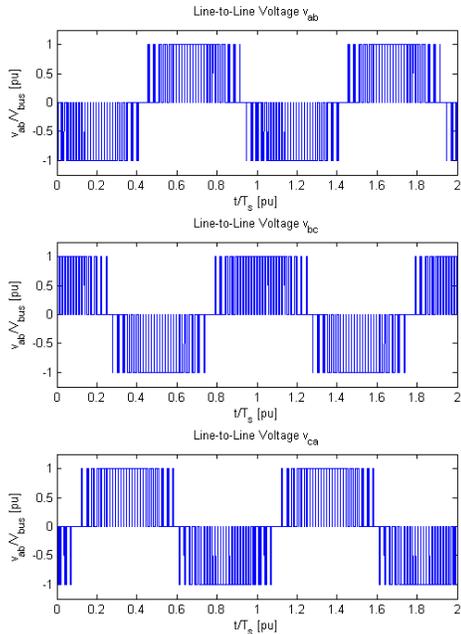


Figure 2.14: Time domain plot of the line-to-line voltages for an RL load using Two-Level SVM.

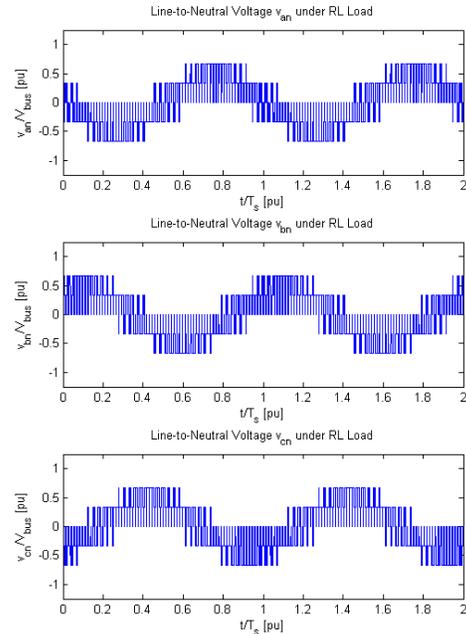


Figure 2.15: Time domain plot of the line-to-neutral voltages for an RL load using Two-Level SVM.

vector modulation is capable of producing essentially sinusoidal output currents with most of the distortion resulting from the fast switching of the IGBTs.

Figure 2.17 and Figure 2.18 present the line-to-neutral voltages and the phase currents presented in Figure 2.15 and Figure 2.16 under the space vector transform and plotted in the  $(\alpha - \beta)$  plane. Note that the transform of the line-to-neutral voltage has only 7 unique space vectors: the six active vectors and the zero vector (since  $\bar{V}_0$  and  $\bar{V}_7$  are redundant). If the plot were to be viewed as the voltage vectors switch in time, the vectors would appear to switch back and forth between the active vectors and the

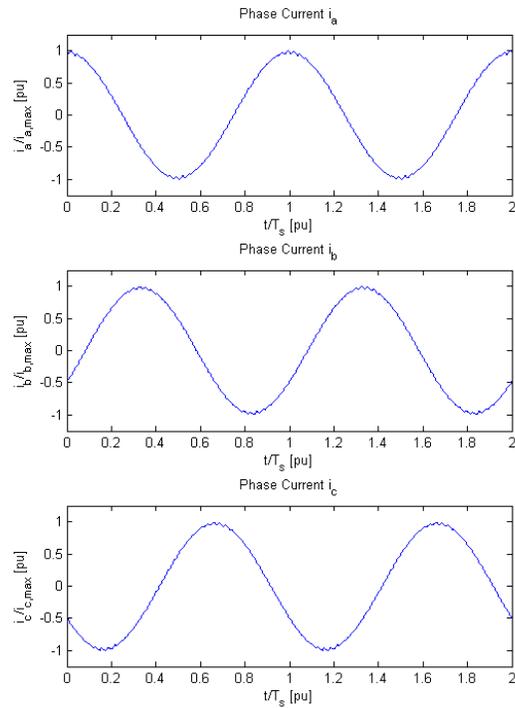


Figure 2.16: Time domain plot of the phase currents for an RL load using Two-Level SVM.

zero vector. In contrast, the phase current space vector is nearly circular with short deviations from the circle's path due to the switching of the IGBTs. This provides another indication that the phase currents produced by space vector modulation are nearly sinusoidal.

The basic two-level inverter topologies were presented in Chapter 2, and a short overview of a few PWM methods was provided. Space vector modulation was developed in detail, and the basic output signals were presented for reference.

In Chapter 3, three common three-level inverter topologies will be introduced, and three-level space vector modulation will be developed in detail.

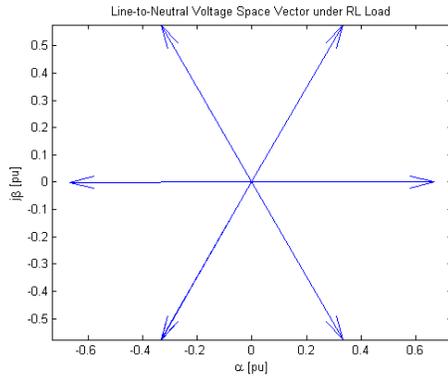


Figure 2.17: Space vector representation of the line-to-neutral voltage in the  $(\alpha - \beta)$  plane.

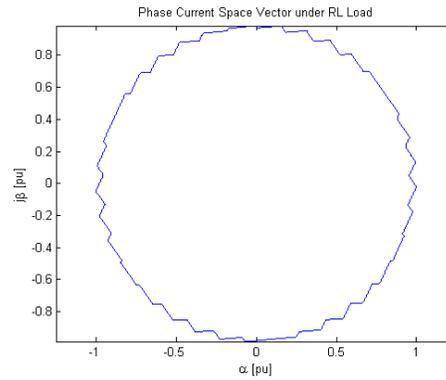


Figure 2.18: Space vector representation of the phase current in the  $(\alpha - \beta)$  plane.

## Chapter 3

### Theoretical Development of Three-Level Inverters and SVPWM

The two-level voltage source inverter has been very popular in drives for many years due to its ease of implementation and control. However, two-level inverters can be limited by the voltage ratings of the semiconductor devices, particularly in high power applications [58]. Multilevel inverters were developed to help address this concern as well as other limitations of two-level inverters. In particular, three-level inverters have been popular due to their improvement in output waveforms without overly complicating the design and control of the inverter. In this chapter, an introduction to the three main three-level inverter topologies as well as a theoretical development of three-level space vector modulation (SVM) will be presented. Section 3.1 introduces the three basic three-level inverter topologies. The strengths and weaknesses of the each of these topologies will be discussed. Section 3.2 presents the theoretical development of three-level SVM and introduces the three different methods that will be investigated in this thesis. All of the developments in this chapter may be extended to higher-level inverters, which are beyond the scope of this work.

### 3.1 Three-Level Inverter Topologies

The basic function of the three-level inverter is very similar to the two-level inverter. While the two-level inverter switches the output phases between the positive dc bus and the negative dc bus, the three-level inverter switches the output phases between the positive dc bus, the negative dc bus, and the neutral point of the bus. This arrangement has several advantages. First, the addition of the neutral point connection reduces the output voltage distortion and lowers the voltage rise time at the motor terminals [4], [21]. The improved output voltage also reduces common mode voltage, which in turn reduces stresses on motor bearings [21], [60]. Finally, the additional voltage level allows operation with a lower switching frequency [60], [61]. Although the three-level inverter has several advantages over the two-level inverter, it also has a few disadvantages. Three-level inverters generally require more switches than two-level inverters, which depending on the switch rating, can increase the cost of the inverter. This disadvantage only grows as the number of levels in the inverter increases. Likewise, the additional voltage levels increase modulation complexity, but as memory and computation costs decrease through improved digital signal processors, the modulation complexity will become more manageable. Overall, the three-level inverter appears to be a viable alternative to the two-level inverter, particularly in high power, medium voltage applications [60], [62].

There are three main three-level inverter topologies: the neutral-point-clamped (NPC) inverter [3], the flying capacitor inverter [2], and the cascaded H-bridge inverter [63]. One early topology that is widely investigated is the NPC inverter, shown in Figure 3.1. Compared to the two-level inverter, the three-level NPC inverter uses two additional series-connected IGBTs within each phase leg. For each phase leg  $x = \{a, b, c\}$ , the two middle IGBTs  $Q_{x2}$  and  $Q_{x3}$  are clamped to the neutral point of the dc bus by the two diodes  $D_{x5}$  and  $D_{x6}$ . Through different patterns of conducting periods and open periods of the IGBTs within a phase leg, each output phase may be switched between the positive rail P, the negative rail N, and the neutral point O of the dc bus. Proper sequencing of the conducting periods and the open periods of the IGBTs within each phase leg creates the three-phase output voltage.

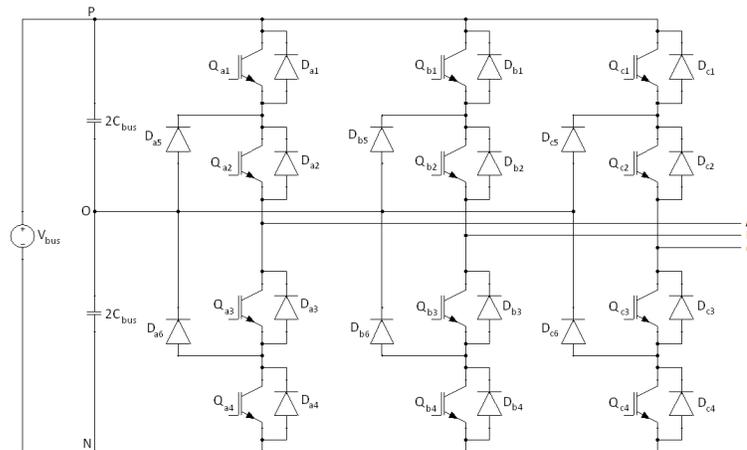


Figure 3.1: Three-level neutral-point-clamped inverter.

In addition to the advantages over two-level inverters that most three-level

inverter topologies share, the IGBTs of the NPC inverter have a reduced voltage rating since they must only block half of the dc bus voltage [3], [58]. However, despite the reduced IGBT rating, the reverse voltage rating of the clamping diodes must be higher since these components must block a larger percentage of the bus voltage [60]. This becomes more apparent as the number of voltage levels in the inverter increases. Another weakness of this inverter topology is that the outer IGBTs are not loaded as heavily as the inner IGBTs, resulting in unsymmetrical losses among the devices [53], [62]. The final important weakness of this topology is that the voltage of the two bus capacitances becomes imbalanced by connecting the individual output phases to the bus neutral point [53]. If severe, this imbalance can negatively affect the inverter control and cause additional voltage stresses to various components. Neutral point balance is generally achieved through various control loops and constitutes its own field of research [4], [34], [40]. However, it has been shown that most methods cannot completely control neutral point imbalance for all load conditions [64]. Despite its weaknesses, the neutral-point-clamped inverter remains one of the most widely used multilevel inverter topologies [62] because it is easily built using standard IGBT modules. This thesis focuses on three space vector modulation methods for a three-level NPC inverter due to the design simplicity of the NPC inverter and its wide use in multilevel inverter applications.

The three-level flying capacitor inverter topology presented in Figure 3.2 is

similar in function to the NPC inverter topology and shares many of its advantages. Like the NPC inverter, the flying capacitor inverter adds two IGBTs per phase leg. However, the two diodes that clamp the inner IGBTs to the neutral point of the dc bus in the NPC inverter are replaced by a capacitor charged to a certain voltage level, often half of the dc bus voltage. Proper sequencing of the conducting periods and the open periods of the IGBTs within each phase leg creates the three-phase output voltage.

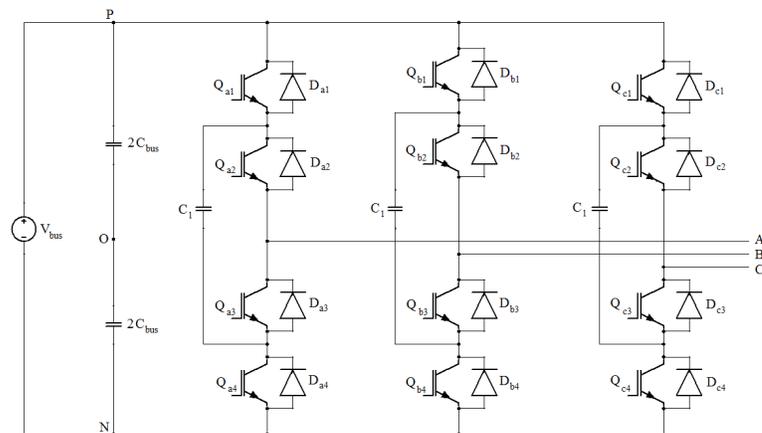


Figure 3.2: Three-level flying capacitor inverter.

The flying capacitor inverter's primary advantage over the NPC inverter is that it uses fewer diodes. This leads to lower drive cost and higher efficiency [58]. However, replacing the clamping diodes with capacitors creates several weaknesses with this topology. Similar to the bus capacitors of the NPC inverter, the clamping capacitors can become imbalanced during normal operation. The clamping capacitors

must also have a high enough voltage rating to withstand large percentages of the dc bus voltage [53]. This is especially important as the number of voltage levels in the inverter increases. Finally, inverter initialization is difficult for this topology because the clamping capacitors need to be precharged to the correct voltage level before inverter modulation begins. This complicates the modulation method and can negatively affect the drive's ability to withstand source voltage dips and ride-through conditions [53]. Capacitor sizing and initialization are the two main factors that have limited the applications in which flying capacitor inverters are used [53].

The final three-level inverter topology to be considered is the cascaded H-bridge inverter presented in Figure 3.3. This topology is significantly different than the two previously presented topologies. Instead of adding two IGBTs to each leg of a two-level inverter and clamping the voltage of the inner IGBTs, this topology cascades three single-phase H-bridges to produce the phase legs. Each H-bridge has its own isolated dc voltage source  $V_{dc}$  and can switch between  $-V_{dc}$ , 0, and  $V_{dc}$ . Proper control of the three H-bridges produces the three-phase output voltage.

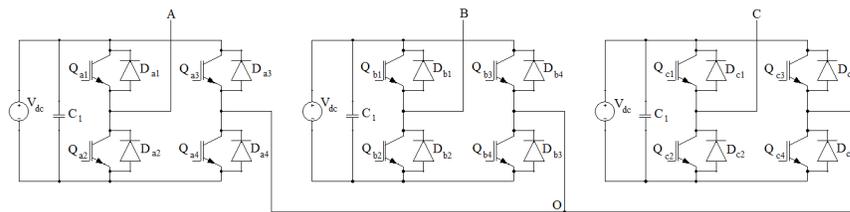


Figure 3.3: Three-level cascaded H-bridge inverter.

One major advantage of this topology is that each H-bridge can be controlled independently. This offers a large amount of flexibility in modulation as well as a simpler control structure since the controller can be distributed [53], [58]. This flexibility in modulation also allows the average power flow through each bridge to be balanced through the modulation method [53], which is difficult to achieve in the two previous inverter topologies. Another advantage is that the capacitors are inherently balanced since each is supplied from an independent dc source [53]. However, providing separate dc sources for each H-bridge might not be feasible depending on the application.

Many of the modulation strategies that exist for two-level inverters also exist for three-level inverters, though the additional voltage level complicates all of these methods to some degree. Many PWM techniques such as sinusoidal PWM, selective harmonic elimination PWM, and space vector modulation have been applied successfully to three-level inverters [60]. Three-level space vector modulation is developed in the following section. Furthermore, the three methods under investigation, each of which applies a different switching sequence, are explained.

### **3.2 Three-Level SVPWM**

The basic theory of three-level space vector PWM is very similar to two-level space vector PWM. Recall the three-level NPC inverter presented in Figure 3.1, which

has four IGBTs  $Q_{x1}$ ,  $Q_{x2}$ ,  $Q_{x3}$ , and  $Q_{x4}$  per phase leg  $x = \{a, b, c\}$ . Similar to the two-level case where the top and bottom switches in each phase leg are complementary, the two switches  $Q_{x1}$  and  $Q_{x3}$  are complementary, and the two switches  $Q_{x2}$  and  $Q_{x4}$  are complementary. With this arrangement, the phase output can be connected to the positive dc bus P when  $Q_{x1}$  and  $Q_{x2}$  are conducting, to the negative dc bus N when  $Q_{x3}$  and  $Q_{x4}$  are conducting, or to the neutral point of the dc bus O when  $Q_{x1}$  and  $Q_{x3}$  are open and  $Q_{x2}$  and  $Q_{x4}$  are conducting. These relationships are shown in Table 3.1.

	$Q_{x1}$	$Q_{x2}$	$Q_{x3}$	$Q_{x4}$
N	OFF	OFF	ON	ON
O	OFF	ON	ON	OFF
P	ON	ON	OFF	OFF

Table 3.1: Representation of switching states for a switching combination where  $x = \{a, b, c\}$ .

Due to the three possible connections to the dc bus for each of the three phases, the three-level inverter can produce a total of  $(3)^3 = 27$  switching states, as opposed to the eight switching states in the two-level inverter. The three-level switching states are represented based on the phase connections to the dc bus. The first letter in the state name corresponds to the phase A leg connection to the dc bus, the second letter corresponds to the phase B connection to the dc bus, and the third letter corresponds to the phase C connection to the dc bus. For example, the switching state (*PON*) represents the phase A leg connected to the positive dc bus, the phase B leg connected to the neutral point of the dc bus, and the phase C leg connected to the negative dc

bus. Line-to-line and line-to-neutral voltages corresponding to the different switching states may be found using a method identical to the method presented in the two-level space vector PWM development. The complete set of switching states and their corresponding line-to-line and line-to-neutral voltages are presented in Table 3.2.

The space vector transform previously presented in Equation 2.3 is used to create voltage vectors that compactly represent the output phase voltages for each switching state. By examining the magnitudes of the voltage space vectors for each switching state, it becomes apparent that the vectors may be grouped by length. The three zero vectors have zero length, the twelve small vectors have a length of  $\frac{1}{3}V_{bus}$ , the six medium vectors have a length of  $\frac{\sqrt{3}}{3}V_{bus}$ , and the six large vectors have a length of  $\frac{2}{3}V_{bus}$ . The complete set of switching states and their corresponding voltage vectors is shown in Table 3.3.

It is shown in [64] that when one or two phases are connected to the neutral point of the dc bus, a current flows between the neutral point of the bus and the neutral point connections of the three phases. This causes the bus capacitors to charge and discharge, creating an imbalance in the neutral point voltage. In the case of one phase connected to the neutral point, the neutral point current is in the same direction as the current in that phase. In the case of two phases connected to the neutral point, the neutral point current is in the opposite direction of the current in the third phase. Only in the cases of the small and medium vectors are one or two phases connected

to the neutral point of the dc bus. Thus only these vectors affect the neutral point balance. The effect of each switching state on the neutral point balance of the dc bus is shown in Table 3.3.

The small vectors may be further subdivided based on the direction in which they affect the neutral point balance. The small vectors that affect the neutral point balance in the same direction as the phase current are called positive small vectors, and the small vectors that affect the neutral point balance in the opposite direction of the phase current are called negative small vectors. For each positive small vector, there is a negative small vector of equal magnitude and angle. Thus all of the small vectors are redundant.

Switch State	$v_{AB}$	$v_{BC}$	$v_{CA}$	$v_{An}$	$v_{Bn}$	$v_{Cn}$
( <i>NNN</i> )	0	0	0	0	0	0
( <i>OOO</i> )	0	0	0	0	0	0
( <i>PPP</i> )	0	0	0	0	0	0
( <i>ONN</i> )	$\frac{1}{2}V_{bus}$	0	$-\frac{1}{2}V_{bus}$	$\frac{1}{3}V_{bus}$	$-\frac{1}{6}V_{bus}$	$-\frac{1}{6}V_{bus}$
( <i>PPO</i> )	0	$\frac{1}{2}V_{bus}$	$-\frac{1}{2}V_{bus}$	$\frac{1}{6}V_{bus}$	$\frac{1}{6}V_{bus}$	$-\frac{1}{3}V_{bus}$
( <i>NON</i> )	$-\frac{1}{2}V_{bus}$	$\frac{1}{2}V_{bus}$	0	$-\frac{1}{6}V_{bus}$	$\frac{1}{3}V_{bus}$	$-\frac{1}{6}V_{bus}$
( <i>OPP</i> )	$-\frac{1}{2}V_{bus}$	0	$\frac{1}{2}V_{bus}$	$-\frac{1}{3}V_{bus}$	$\frac{1}{6}V_{bus}$	$\frac{1}{6}V_{bus}$
( <i>NNO</i> )	0	$-\frac{1}{2}V_{bus}$	$\frac{1}{2}V_{bus}$	$-\frac{1}{6}V_{bus}$	$-\frac{1}{6}V_{bus}$	$\frac{1}{3}V_{bus}$
( <i>POP</i> )	$\frac{1}{2}V_{bus}$	$-\frac{1}{2}V_{bus}$	0	$\frac{1}{6}V_{bus}$	$-\frac{1}{3}V_{bus}$	$\frac{1}{6}V_{bus}$
( <i>POO</i> )	$\frac{1}{2}V_{bus}$	0	$-\frac{1}{2}V_{bus}$	$\frac{1}{3}V_{bus}$	$-\frac{1}{6}V_{bus}$	$-\frac{1}{6}V_{bus}$
( <i>OON</i> )	0	$\frac{1}{2}V_{bus}$	$-\frac{1}{2}V_{bus}$	$\frac{1}{6}V_{bus}$	$\frac{1}{6}V_{bus}$	$-\frac{1}{3}V_{bus}$
( <i>OPO</i> )	$-\frac{1}{2}V_{bus}$	$\frac{1}{2}V_{bus}$	0	$-\frac{1}{6}V_{bus}$	$\frac{1}{3}V_{bus}$	$-\frac{1}{6}V_{bus}$
( <i>NOO</i> )	$-\frac{1}{2}V_{bus}$	0	$\frac{1}{2}V_{bus}$	$-\frac{1}{3}V_{bus}$	$\frac{1}{6}V_{bus}$	$\frac{1}{6}V_{bus}$
( <i>OOP</i> )	0	$-\frac{1}{2}V_{bus}$	$\frac{1}{2}V_{bus}$	$-\frac{1}{6}V_{bus}$	$-\frac{1}{6}V_{bus}$	$\frac{1}{3}V_{bus}$
( <i>ONO</i> )	$\frac{1}{2}V_{bus}$	$-\frac{1}{2}V_{bus}$	0	$\frac{1}{6}V_{bus}$	$-\frac{1}{3}V_{bus}$	$\frac{1}{6}V_{bus}$
( <i>PON</i> )	$\frac{1}{2}V_{bus}$	$\frac{1}{2}V_{bus}$	$-V_{bus}$	$\frac{1}{2}V_{bus}$	0	$-\frac{1}{2}V_{bus}$
( <i>OPN</i> )	$-\frac{1}{2}V_{bus}$	$V_{bus}$	$-\frac{1}{2}V_{bus}$	0	$\frac{1}{2}V_{bus}$	$-\frac{1}{2}V_{bus}$
( <i>NPO</i> )	$-V_{bus}$	$\frac{1}{2}V_{bus}$	$\frac{1}{2}V_{bus}$	$-\frac{1}{2}V_{bus}$	$\frac{1}{2}V_{bus}$	0
( <i>NOP</i> )	$-\frac{1}{2}V_{bus}$	$-\frac{1}{2}V_{bus}$	$V_{bus}$	$-\frac{1}{2}V_{bus}$	0	$\frac{1}{2}V_{bus}$
( <i>ONP</i> )	$\frac{1}{2}V_{bus}$	$-V_{bus}$	$\frac{1}{2}V_{bus}$	0	$-\frac{1}{2}V_{bus}$	$\frac{1}{2}V_{bus}$
( <i>PNO</i> )	$V_{bus}$	$-\frac{1}{2}V_{bus}$	$-\frac{1}{2}V_{bus}$	$\frac{1}{2}V_{bus}$	$-\frac{1}{2}V_{bus}$	0
( <i>PNN</i> )	$V_{bus}$	0	$-V_{bus}$	$\frac{2}{3}V_{bus}$	$-\frac{1}{3}V_{bus}$	$-\frac{1}{3}V_{bus}$
( <i>PPN</i> )	0	$V_{bus}$	$-V_{bus}$	$\frac{1}{3}V_{bus}$	$\frac{1}{3}V_{bus}$	$-\frac{2}{3}V_{bus}$
( <i>NPN</i> )	$-V_{bus}$	$V_{bus}$	0	$-\frac{1}{3}V_{bus}$	$\frac{2}{3}V_{bus}$	$-\frac{1}{3}V_{bus}$
( <i>NPP</i> )	$-V_{bus}$	0	$V_{bus}$	$-\frac{2}{3}V_{bus}$	$\frac{1}{3}V_{bus}$	$\frac{1}{3}V_{bus}$
( <i>NNP</i> )	0	$-V_{bus}$	$V_{bus}$	$-\frac{1}{3}V_{bus}$	$-\frac{1}{3}V_{bus}$	$\frac{2}{3}V_{bus}$
( <i>PNP</i> )	$V_{bus}$	$-V_{bus}$	0	$\frac{1}{3}V_{bus}$	$-\frac{2}{3}V_{bus}$	$\frac{1}{3}V_{bus}$

Table 3.2: Line-to-line and line-to-neutral voltages in Volts corresponding to the 27 switching states.

Switching State	Type	Voltage Space Vector	$i_{NP}$
( <i>NNN</i> )	Zero	0	0
( <i>OOO</i> )	Zero	0	0
( <i>PPP</i> )	Zero	0	0
( <i>ONN</i> )	Small+	$\frac{1}{3}V_{bus}e^{j0}$	$i_a$
( <i>PPO</i> )	Small+	$\frac{1}{3}V_{bus}e^{j\pi/3}$	$i_c$
( <i>NON</i> )	Small+	$\frac{1}{3}V_{bus}e^{j2\pi/3}$	$i_b$
( <i>OPP</i> )	Small+	$\frac{1}{3}V_{bus}e^{j\pi}$	$i_a$
( <i>NNO</i> )	Small+	$\frac{1}{3}V_{bus}e^{j4\pi/3}$	$i_c$
( <i>POP</i> )	Small+	$\frac{1}{3}V_{bus}e^{j5\pi/3}$	$i_b$
( <i>POO</i> )	Small-	$\frac{1}{3}V_{bus}e^{j0}$	$-i_a$
( <i>OON</i> )	Small-	$\frac{1}{3}V_{bus}e^{j\pi/3}$	$-i_c$
( <i>OPO</i> )	Small-	$\frac{1}{3}V_{bus}e^{j2\pi/3}$	$-i_b$
( <i>NOO</i> )	Small-	$\frac{1}{3}V_{bus}e^{j\pi}$	$-i_a$
( <i>OOP</i> )	Small-	$\frac{1}{3}V_{bus}e^{j4\pi/3}$	$-i_c$
( <i>ONO</i> )	Small-	$\frac{1}{3}V_{bus}e^{j5\pi/3}$	$-i_b$
( <i>PON</i> )	Medium	$\frac{\sqrt{3}}{3}V_{bus}e^{j\pi/6}$	$i_b$
( <i>OPN</i> )	Medium	$\frac{\sqrt{3}}{3}V_{bus}e^{j\pi/2}$	$i_a$
( <i>NPO</i> )	Medium	$\frac{\sqrt{3}}{3}V_{bus}e^{j5\pi/6}$	$i_c$
( <i>NPO</i> )	Medium	$\frac{\sqrt{3}}{3}V_{bus}e^{j7\pi/6}$	$i_b$
( <i>ONP</i> )	Medium	$\frac{\sqrt{3}}{3}V_{bus}e^{j3\pi/2}$	$i_a$
( <i>PNO</i> )	Medium	$\frac{\sqrt{3}}{3}V_{bus}e^{j11\pi/6}$	$i_c$
( <i>PNN</i> )	Large	$\frac{2}{3}V_{bus}e^{j0}$	0
( <i>PPN</i> )	Large	$\frac{2}{3}V_{bus}e^{j\pi/3}$	0
( <i>NPN</i> )	Large	$\frac{2}{3}V_{bus}e^{j2\pi/3}$	0
( <i>NPP</i> )	Large	$\frac{2}{3}V_{bus}e^{j\pi}$	0
( <i>NNP</i> )	Large	$\frac{2}{3}V_{bus}e^{j4\pi/3}$	0
( <i>PNP</i> )	Large	$\frac{2}{3}V_{bus}e^{j5\pi/3}$	0

Table 3.3: Three-level switching voltages in space vector form.

By plotting the set of 27 voltage vectors in the  $(\alpha - \beta)$  plane as in Figure 3.4, the relationship between the voltage vectors may be established. The six positive small vectors and their corresponding negative small vectors form the vertices of a small inner hexagon. The six large vectors form the vertices of a large outer hexagon aligned with the inner hexagon. The medium vectors bisect the sides of the outer hexagon. By connecting the tips of the vectors closest to each other, a pattern of equilateral triangles within the hexagon is formed.

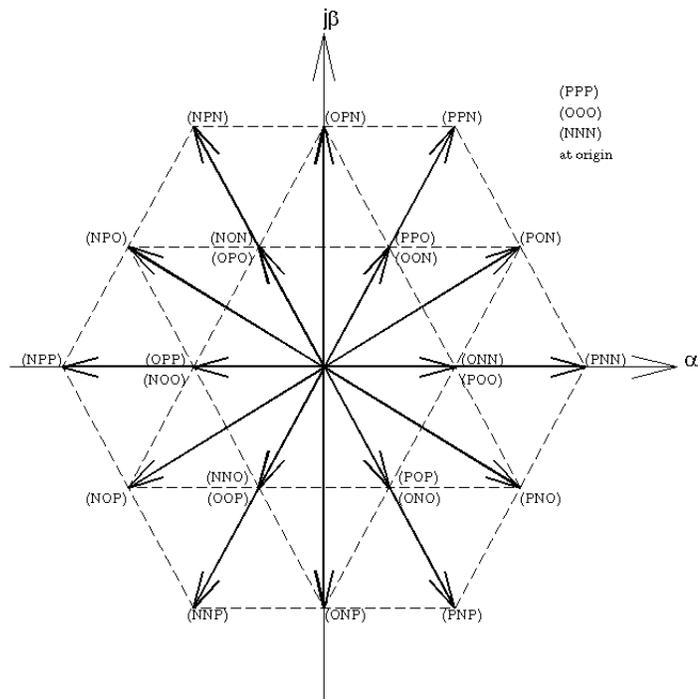


Figure 3.4: The three-level voltage vectors plotted in the  $(\alpha - \beta)$  plane.

The basic strategy of three-level space vector PWM is identical to that of two-level space vector PWM. A rotating reference vector formed from three sinusoidal sources is approximated over a sampling period  $T_s$  using linear combinations of voltage vectors. The reference vector is written in Equation 3.1. The magnitude of the reference vector  $V_{ref}$  represents the desired peak of the fundamental line-to-neutral output voltage. The angular position in e.rad of the reference vector in the  $(\alpha - \beta)$  plane is represented by  $\theta$ , and the desired output fundamental frequency in e.rad/s is represented by  $\omega_e$ . The term  $\phi$  represents the initial angular position of the reference vector in e.rad.

$$\bar{V}_{ref} = V_{ref}e^{j\theta}, \quad \text{where } \theta = \omega_e t + \phi \quad (3.1)$$

As in two-level space vector PWM, as long as the reference vector lies within the hexagon formed by the large voltage vectors, it may be exactly represented as its sampled value over a sampling period using a linear combination of voltage vectors. When the trajectory of the reference vector lies completely within the large hexagon over the fundamental period, the inverter is operating in the linear modulation region. For sinusoidal references, the trajectory of the reference vector is a circle in the  $(\alpha - \beta)$  plane. The radius of the largest circle that can be inscribed in the outer hexagon marks the upper limit of the linear modulation region. In the three-level case, this

corresponds to the magnitude of the medium vectors. Thus, the upper boundary of the linear modulation region for three-level space vector PWM is  $V_{ref,max} = \frac{\sqrt{3}}{3}V_{bus}$ , which is identical to the boundary of the linear modulation region in two-level space vector PWM.

If the trajectory of the reference vector extends beyond the hexagon in whole or in part, the reference vector cannot be represented exactly within a single sampling period, and the inverter enters the overmodulation region. The three-level overmodulation region is very similar to the two-level overmodulation region. However, a detailed description of overmodulation operation is beyond the scope of this thesis. For more information on overmodulation operation in multilevel inverters, references [34] and [35] should be consulted.

The primary challenge in the development of algorithms for multilevel space vector PWM is the selection of voltage vectors for each sampling period. The increased vector redundancy over two-level space vector PWM allows for much flexibility in the creation of a PWM method, but it also increases implementation complexity. Representing the reference vector using the three nearest voltage vectors has been shown to produce minimal distortion [22]. However, determining the three nearest voltage vectors can be computationally difficult. There are several algorithms in the literature [22], [24] for selecting the three nearest voltage vectors to the reference vector, but most of these algorithms are capable of producing the same switching

signals. One method of determining the three nearest voltage vectors and calculating the dwell times of the corresponding vectors is presented in [23] and [53], which is the method used in this thesis. In this method, the three-level space vector PWM problem is reduced to a two-level space vector PWM problem. This method may be extended to higher level inverters, but complexity increases as the number of levels increases.

To simplify the three-level space vector PWM logic, the three-level hexagon of voltage vectors is divided into six smaller hexagons. Three of these smaller hexagons are shown in Figure 3.5. Each of these smaller hexagons is centered at the tips of the small vectors and consists of six equilateral triangles corresponding to the six sectors of a two-level inverter. When the reference vector lies within a specific small hexagon, that hexagon may be controlled in the same manner as a two-level space vector PWM inverter. The small vectors are treated as the zero vectors of the small hexagons.

Since these hexagons overlap, an additional condition is needed to select the proper hexagon when constructing the reference vector. In particular, a smooth transition between hexagons that does not introduce excessive changes in switching states is necessary for reducing current distortion [25]. To achieve a smooth transition between hexagons, the three-level voltage vector hexagon may be divided along the medium vectors into six sectors [53]. These sectors are shown in Figure 3.6. The small hexagon whose center is located within a specific three-level sector is associated with



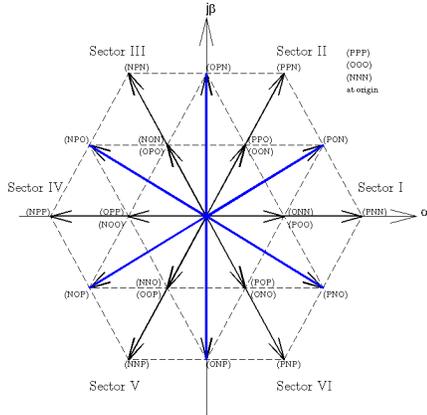


Figure 3.6: The division of the three-level hexagon into sectors.

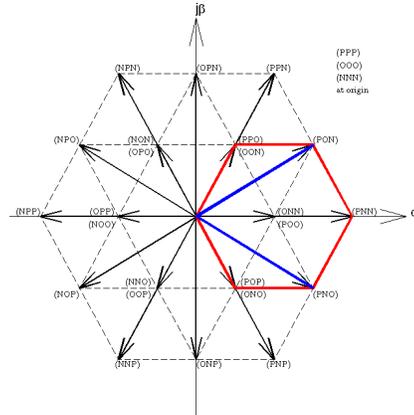


Figure 3.7: Sector I with its corresponding hexagon.

sector I of the three-level sector I.

Since each of the small hexagons may be controlled in the same manner as a two-level space vector modulated inverter, all of the equations introduced for two-level space vector PWM also apply here with some minor modifications. In particular, the basic form of the dwell time equations for the two-level sector  $u$  presented previously in Equation 2.26 and Equation 2.27 remains the same. The only differences lie in the scaling of the equations. As seen in Equation 3.2 and Equation 3.3, the dc bus voltage is divided by two. This is necessary because the origin is shifted when controlling a small hexagon as a two-level inverter. In relation to the shifted origin, all of the voltage vectors appear as though they have a length of  $\frac{1}{3}V_{bus}$  instead of  $\frac{2}{3}V_{bus}$  as in the true two-level case. The definition of  $T_0$  remains the same as shown in Equation 3.4, but instead of corresponding to the dwell time of the zero vector, it corresponds

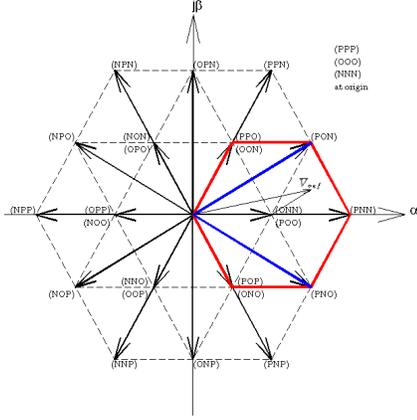


Figure 3.8: Mapping of the three-level voltage reference into the sector I two-level hexagon.

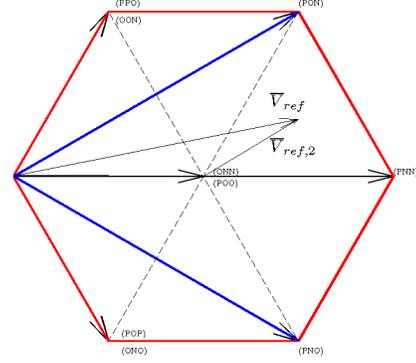


Figure 3.9: Mapping of the three-level voltage reference into the sector I two-level hexagon (enlarged).

to the dwell time of the redundant vector  $\bar{V}_{center}$  at the center of the hexagon.

$$T_u = \sqrt{3} \frac{2V_{ref,2}}{V_{bus}} T_s \sin \left( u \frac{\pi}{3} - \theta \right) \quad (3.2)$$

$$T_v = \sqrt{3} \frac{2V_{ref,2}}{V_{bus}} T_s \sin \left( (u+2) \frac{\pi}{3} - \theta \right) \quad (3.3)$$

$$T_0 = T_s - T_u - T_v \quad (3.4)$$

Once the dwell times for the three voltage vectors are found, the general expression for the three-level reference vector in a two-level sector  $u$  may be written as in Equation 3.5.

$$\bar{V}_{ref} = \frac{T_u}{T_s}\bar{V}_u + \frac{T_v}{T_s}\bar{V}_v + \frac{T_0}{T_s}\bar{V}_{center} \quad (3.5)$$

As in the two-level case, this equation provides no information on the order in which the three voltage vectors, and their corresponding switching states, should be applied. By applying the voltage vectors in different orders, different space vector PWM methods are created. The large number of redundant vectors allows for a wide variety of switching patterns and thus much flexibility in the creation of space vector PWM methods. However, the large number of possibilities for switching patterns also increases the complexity of algorithms. The three space vector PWM methods investigated in this thesis, each of which varies the order of applying the voltage vectors, are described in detail in the remainder of this chapter.

### 3.2.1 SVPWM Method 1

The first three-level space vector PWM switching sequence investigated in this thesis is found in [25]. This sequence is intended to minimize the total number of switching transitions within each sampling period as well as maintain low harmonic distortion in the output voltages. It is based on the basic (0 – 1 – 2 – 7) two-level switching sequence, where the first half of the sampling period in sector I has the switching sequence  $\bar{V}_0 \rightarrow \bar{V}_1 \rightarrow \bar{V}_2 \rightarrow \bar{V}_7$ . In the three-level case, each sampling period begins and ends in the redundant vector. The switching state sequence over the

first half of the switching period transitions around the sector so that no more than one pair of complementary switches changes state at one time. The reverse of the switching sequence is performed in the second half of the switching period. Two representative switching tables are shown in Figure 3.10 and Figure 3.11, while the complete set of 36 switching tables is included in the appendix. In the case of sector I, two-level sector I shown in Figure 3.10, the first half sampling period begins with the positive small vector ( $ONN$ ) and then transitions to the large vector ( $PNN$ ) followed by the medium vector ( $PON$ ) and the negative small vector ( $POO$ ). The second half of the sampling period applies that sequence in reverse: ( $POO$ )  $\rightarrow$  ( $PON$ )  $\rightarrow$  ( $PNN$ )  $\rightarrow$  ( $ONN$ ). The dwell time  $T_0$  is split evenly between the four instances of the small vectors in the sequence, the dwell time  $T_u$  is split evenly between the two instances of the large vector, and the dwell time  $T_v$  is split evenly between the two instances of the medium vector. Due to its relatively high quality waveforms and its simplicity, it is a commonly used sequence.

### 3.2.2 SVPWM Method 2

The second three-level space vector PWM switching sequence investigated in this thesis is proposed in [31]. This sequence is based on the (7 – 2 – 1 – 2) two-level switching sequence, where the first half of the sampling period in sector I has the switching sequence  $\bar{V}_7 \rightarrow \bar{V}_2 \rightarrow \bar{V}_1 \rightarrow \bar{V}_2$ . In this case, a vector other than the

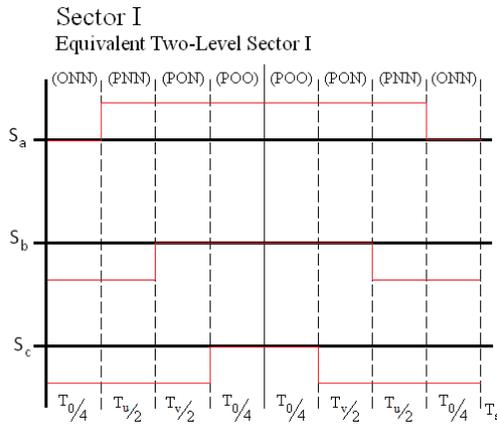


Figure 3.10: Method 1 switching pattern in Sector I, two-level sector I.

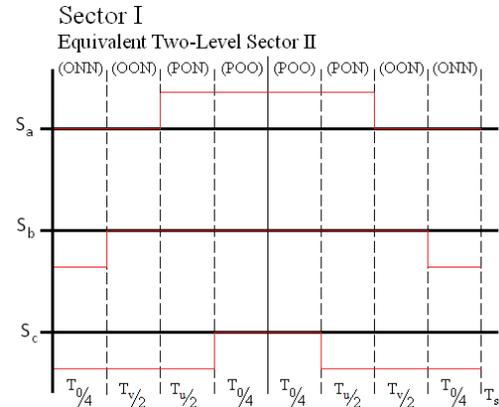


Figure 3.11: Method 1 switching pattern in Sector I, two-level sector II.

redundant vector is repeated within the half sampling period. This switching sequence was found to reduce the output current distortion for certain modulation indices in the case of an induction machine load. However, the reduced use of the redundant small vectors can lead to a larger dc bus neutral point imbalance. Two representative switching tables are shown in Figure 3.12 and Figure 3.13, while the complete set of 36 switching tables is included in the appendix. In the case of sector I, two-level sector I shown in Figure 3.12, the first half sampling period begins with the negative small vector ( $POO$ ) and then transitions to the medium vector ( $PON$ ) followed by the large vector ( $PNN$ ) and the medium vector ( $PON$ ). The second half of the sampling period applies that sequence in reverse: ( $PON$ )  $\rightarrow$  ( $PNN$ )  $\rightarrow$  ( $PON$ )  $\rightarrow$  ( $POO$ ). The dwell time  $T_0$  is split evenly between the two instances of the negative small vector in the sequence, the dwell time  $T_u$  is split evenly between the two instances of

the large vector, and the dwell time  $T_v$  is split evenly between the four instances of the medium vector. Since this method does not use balanced positive and negative small vectors within each sampling period, the neutral point imbalance is expected to be worse for Method 2 than for Method 1 or Method 3.

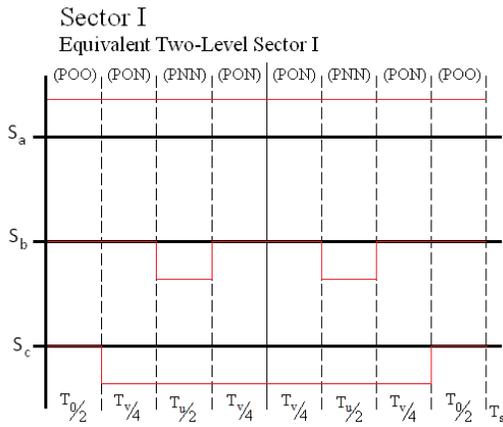


Figure 3.12: Method 2 switching pattern in Sector I, two-level sector I.

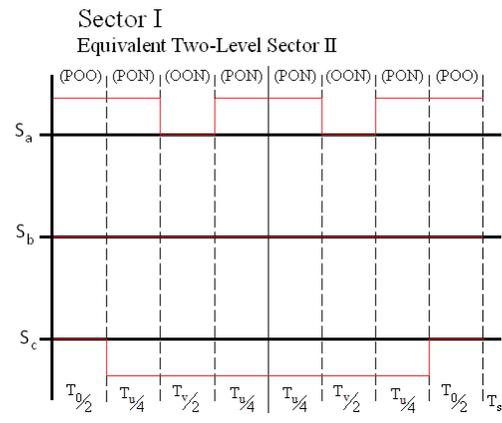


Figure 3.13: Method 2 switching pattern in Sector I, two-level sector II.

### 3.2.3 SVPWM Method 3

The final three-level space vector PWM switching sequence investigated in this thesis is found in [4]. In this method, the number of switching states per half sampling period increases as the magnitude of the reference vector decreases, allowing the inverter to take advantage of all available redundancies in the voltage vectors. This method is particularly useful in closed-loop applications that attempt to control the neutral point imbalance through the ratios of the dwell times of the positive and

negative small vectors due to its use of all available redundancies. However, the use of all redundant vectors also leads to higher switching losses for lower output voltages.

In this method, the three-level voltage vector hexagon may be seen as three layers of triangles: the innermost layer where the vertices of the triangle are two small vectors and the zero vector, the middle layer where the vertices of the triangle are two small vectors and a medium vector, and the outermost layer where the vertices of the triangle are a small vector, a medium vector, and a large vector. For the innermost triangles such as sector I, two-level sector III, the switching period always begins in the switching state  $(NNN)$ , and each half sampling period uses each of the seven available switching states corresponding to the three nearest voltage vectors. For the middle triangles such as sector I, two-level sector II, the switching period always begins in a positive small vector adjacent to  $(NNN)$ , and each half sampling period uses each of the five available switching states corresponding to the three nearest voltage vectors. The switching periods within the outermost triangles such as sector I, two-level sector I use the standard  $(0 - 1 - 2 - 7)$  switching sequence defined in Method 1, and each half sampling period uses each of the four available switching states corresponding to the three nearest voltage vectors. Two representative switching tables for an inner triangle and a middle triangle are shown in Figure 3.14 and Figure 3.15. The form of the switching table for the outer triangles is similar to that of Figure 3.10. For brevity, it is not shown here. The complete set of 36 switching tables is included in

the appendix.

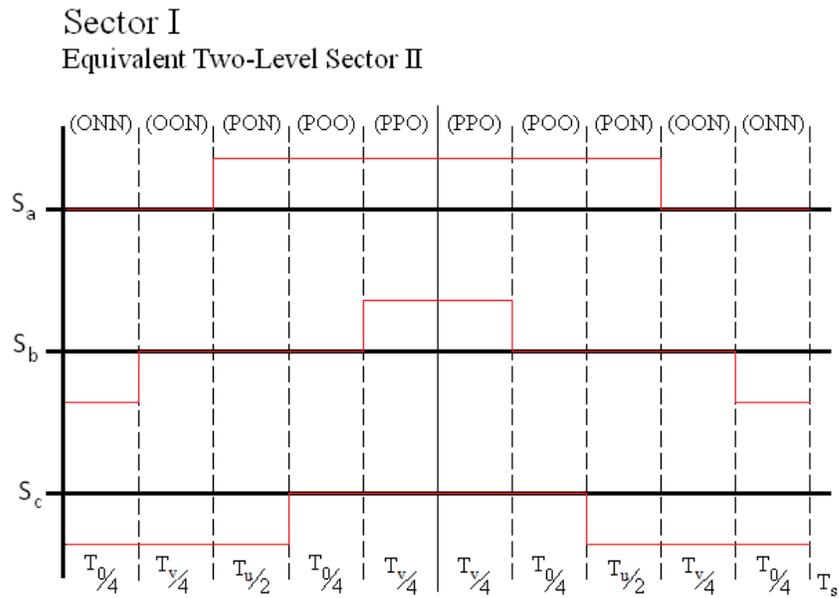


Figure 3.14: Method 3 switching pattern in Sector I, two-level sector II.

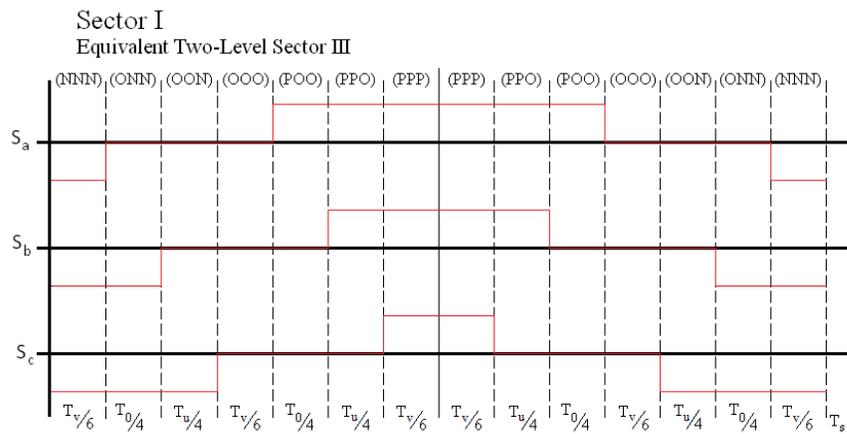


Figure 3.15: Method 3 switching pattern in Sector I, two-level sector III.

In Chapter 3, the three main three-level inverter topologies were introduced,

and three-level space vector PWM theory was presented in terms of two-level space vector PWM. The three space vector PWM switching sequences under investigation were also explained. The system model, including the IPM machine model, the three-level NPC inverter model, and the space vector PWM pulse generator, will be presented in Chapter 4.

## Chapter 4

### Development of System Models and Simulations

In this chapter, the simulation model developed for the three-level inverter system is presented. MATLAB Simulink was used in the simulation of this system because a wide variety of controls and expressions are easily implemented in the Simulink environment. The system model consists of three modules: the IPM machine load, the three-level NPC inverter, and the space vector PWM pulse generator. The state space model for a PM machine is presented in the first section, and the specific model for the IPM machine under investigation is developed in the following section. Since all three space vector PWM models apply the same logic and only differ in the generated switching patterns, the generic space vector PWM pulse generator is explained in Section 4.3. The differences between the pulse generator blocks for the three methods are also explained. The development of the three-level NPC inverter model and the overall system model is presented in the final section.

#### 4.1 Introduction to Machine State Space Models

The state space modeling technique is a method of reducing a  $k^{th}$  order differential equation to a set of  $k$  coupled first order differential equations. As applied to electric machines, state space models are a convenient way to compactly represent the defining differential equations of the machine. Several different forms of state space models for PM machines have been used over the years. In particular, the machine phase currents have been used as the state variables in some work, and the machine flux linkages have been used as the state variables in other studies. Likewise, two different frames of reference have been applied: the abc frame of reference in which the real phase values are the state variables, and the dqo frame of reference in which the state variables are transformed into the rotating dqo reference frame. An excellent development of the technique is presented in [65].

In this thesis, the abc current frame of reference will be considered because this model can include most of the characteristics of the machine. Since this is a lightly saturated machine, the effects of the space harmonics in the PM-induced emfs and the effects of the higher order harmonic components of the winding inductances may be included [66]. The basic state space representation of a PM machine in the abc current frame of reference is presented in [66] and is reproduced in Equation 4.1:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} r_a & 0 & 0 \\ 0 & r_b & 0 \\ 0 & 0 & r_c \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \frac{d}{dt} \left\{ \begin{bmatrix} L_{aa} & L_{ab} & L_{ac} \\ L_{ba} & L_{bb} & L_{bc} \\ L_{ca} & L_{cb} & L_{cc} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \right\} + \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \quad (4.1)$$

In this model,  $v_a$ ,  $v_b$ , and  $v_c$  represent the time domain terminal phase voltages of the machine, and  $i_a$ ,  $i_b$ , and  $i_c$  represent the time domain phase currents of the machine. Also,  $r_a$ ,  $r_b$ , and  $r_c$  represent the winding resistances, and  $e_a$ ,  $e_b$ , and  $e_c$  represent the PM-induced back emfs. The various terms of the form  $L_{xy}$ , where  $x = \{a, b, c\}$  and  $y = \{a, b, c\}$ , represent the time-varying self and mutual inductances of the phase windings. The terms for the inductances and back emfs can be calculated using Finite Element Analysis (FEA) [67].

## 4.2 The Machine to be Used in Simulation

### 4.2.1 Machine Specifications

The machine used in this investigation is an internal permanent magnet synchronous machine donated to Marquette University by A.O. Smith Corporation. The machine ratings are presented in Table 4.1. This machine was designed with a trapezoidal back emf, which is expected to have an interesting effect on the space vector PWM methods under investigation. Normally, a machine such as this one is not driven by a multilevel inverter. However, this machine was used in the investigation because

all of its design information was available. With this design information, an accurate circuit model could be created for this machine.

Rated Power	3.5 hp
Rated Speed	3450 r/min
Rated Torque	7.25 N·m
Rated Current	10 A
Rated Line-to-Line Voltage	240 V

Table 4.1: Ratings of the IPM machine under investigation.

Expressions for the back emf and the time-varying inductances were found previously using the Finite Element Analysis tool ANSYS Maxwell. The expressions for the back emfs of the machine are of the following form:

$$e_a(\sigma) = \omega_m \sum_{h=1}^{13} A_h \cos [h(\sigma) - \psi_h] \text{ V} \quad (4.2)$$

$$e_b(\sigma) = \omega_m \sum_{h=1}^{13} A_h \cos \left[ h \left( \sigma - \frac{2\pi}{3} \right) - \psi_h \right] \text{ V} \quad (4.3)$$

$$e_c(\sigma) = \omega_m \sum_{h=1}^{13} A_h \cos \left[ h \left( \sigma - \frac{4\pi}{3} \right) - \psi_h \right] \text{ V} \quad (4.4)$$

Here,  $\omega_m$  is the speed of the machine in m.rad/s,  $A_h$  represents the different magnitudes of the harmonic components in V/m.rad/s,  $\psi_h$  represents the phase angle of the different harmonics in e.rad, and  $\sigma$  is the position of the rotor in e.rad. In steady state,  $\sigma$  may be rewritten as follows:

$$\sigma = \omega_e t + \sigma_0 \quad (4.5)$$

where  $\omega_e$  is the electrical speed of the machine in e.rad/s,  $t$  is time in seconds, and  $\sigma_0$  is the initial position of the rotor in e.rad. The values of  $A_h$  and  $\psi_h$  for the first thirteen harmonics are given in Table 4.2.

Harmonic Order h	$A_h$ (V/m.rad/s)	$\psi_h$ (e.rad)
1	$4.464 \cdot 10^{-1}$	1.5702
3	$1.013 \cdot 10^{-1}$	1.5717
5	$1.889 \cdot 10^{-2}$	1.5854
7	$1.081 \cdot 10^{-2}$	-1.5765
9	$1.380 \cdot 10^{-2}$	-1.5583
11	$1.899 \cdot 10^{-2}$	1.5667
13	$8.873 \cdot 10^{-3}$	1.5787

Table 4.2: Harmonic components of the back emf for the IPM machine under investigation found using FEA.

The values of the winding resistances, the self inductances, and the mutual inductances were also found from FEA. These machine parameters are found in Table 4.3.

Parameter	Expression
$r_a = r_b = r_c$	$0.49\Omega$
$L_{aa}$	$6.008607 + 1.981518 \cos(2\sigma) + 0.274595 \cos(4\sigma)$ mH
$L_{bb}$	$6.008607 + 1.981518 \cos\left(2\sigma - \frac{4\pi}{3}\right) + 0.274595 \cos\left(4\sigma - \frac{2\pi}{3}\right)$ mH
$L_{cc}$	$6.008607 + 1.981518 \cos\left(2\sigma - \frac{2\pi}{3}\right) + 0.274595 \cos\left(4\sigma - \frac{4\pi}{3}\right)$ mH
$L_{ab} = L_{ba}$	$-1.940512 - 1.529431 \sin\left(2\sigma - \frac{\pi}{3}\right) - 0.08451 \sin\left(4\sigma - \frac{2\pi}{3}\right)$ mH
$L_{bc} = L_{cb}$	$-1.940512 - 1.529431 \sin\left(2\sigma - \frac{5\pi}{3}\right) - 0.08451 \sin\left(4\sigma - \frac{4\pi}{3}\right)$ mH
$L_{ca} = L_{ac}$	$-1.940512 - 1.529431 \sin(2\sigma - \pi) - 0.08451 \sin(4\sigma)$ mH

Table 4.3: Phase resistance and inductances of the IPM machine under investigation found using FEA.

The machine state space representation will be implemented in the following section using a circuit model based on the FEA-calculated back emfs, the self inductances, and the mutual inductances.

#### 4.2.2 Machine Model

Based on Equation 4.1, a circuit model that can be implemented using MATLAB Simulink can be created. By examining this equation, it is apparent that the terminal voltage of the machine consists of three voltage terms: the ohmic voltage drop, the inductive voltage drop, and the PM-induced back emf. The ohmic voltage drop can be modeled simply as a three-phase resistance as in Figure 4.1. The two remaining terms are slightly more complicated because they vary with rotor position (or, in the steady state case, time). Thus, these two terms are implemented using two controlled (or dependent) voltage sources. The back emf of the machine is simple to implement using a MATLAB function block, which allows the user to write a MATLAB script that couples with a Simulink model. In this case, the MATLAB function block calculates the values of  $e_a$ ,  $e_b$ , and  $e_c$  at each time step, which determine the values of the dependent voltage sources corresponding to the back emfs. Thus, Equation 4.2 through Equation 4.4 may be implemented directly. The inductive voltage drop is slightly more complicated to implement due to the derivative associated with the term. The product of the inductance matrix and the current vector is calculated at each time

step using another MATLAB function block. A derivative block is used to differentiate the elements of the resulting vector with respect to time, and the result is used to control the second set of dependent voltage sources. The inclusion of the derivative block can cause simulation non-convergence if the time step is not sufficiently small, or if the derivative changes too quickly. Thus, care must be taken in the selection of the simulation time step. In this investigation, a variable step discrete solver was used with a maximum time step of 1 microsecond, which provided satisfactory results.

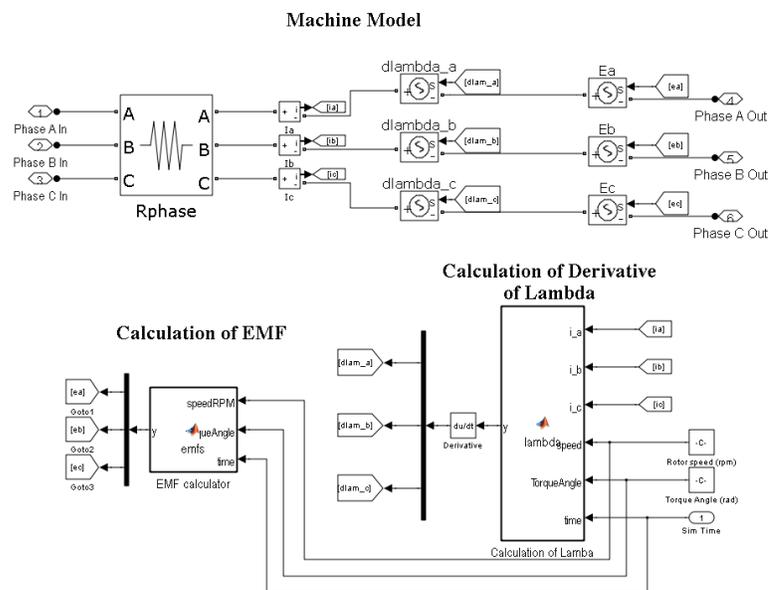


Figure 4.1: Circuit representation of the state space equations for the given IPM machine.

The simulation model was verified by running an open circuit simulation at rated speed and measuring the terminal voltages of the machine, the results of which are provided in Figure 4.2. These results agree with the results previously found using

an FEA model.

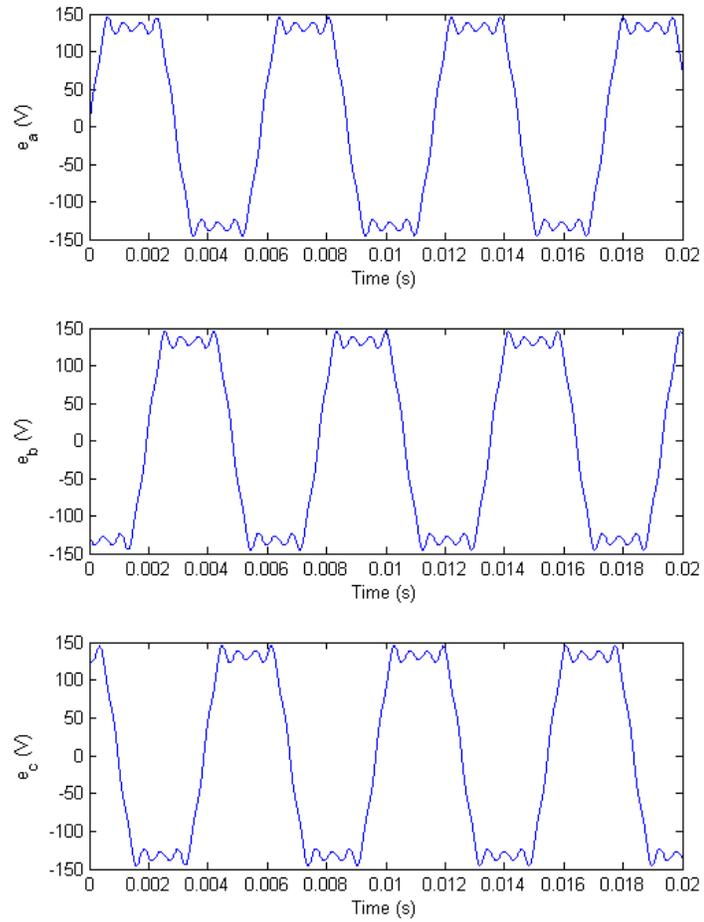


Figure 4.2: Simulated open circuit back emf of the IPM machine.

The circuit model of the IPM machine used in this investigation was developed in this section, and the model was verified using the results from an open circuit simulation at rated speed operation. The space vector PWM simulation models are

developed in the following section.

### 4.3 Space Vector PWM Simulation Models

The space vector PWM generator block is based on the theory developed in Chapter 2 and Chapter 3. The generic Simulink model that implements all three PWM methods under investigation is shown in Figure 4.3. The three sinusoidal reference generators are found at the far left of the model. These references are each sampled using a zero order hold operating at the sampling frequency. The sampled values of the reference are passed into a MATLAB function block (called the Alpha Beta Transform in the model) that transforms the three sampled sinusoids into the  $(\alpha - \beta)$  plane using the space vector transformation previously presented in Equation 2.3. Once the reference vector is found, the angle of the reference vector is calculated. The sector in which the reference vector is located can be found based solely on the angle of the reference vector using simple conditional statements. Once the three-level sector is determined, this information is used to find the magnitude and phase of the equivalent two-level reference vector  $\bar{V}_{ref,2}$ . The magnitude and phase of the equivalent two-level reference as well as the equivalent two-level sector are passed to the MATLAB function block “Calculate State Times” which calculates the values of the dwell times using Equation 3.2, Equation 3.3, and Equation 3.4. The dwell times are passed to the “State Implementation” block along with the three-level sector information and the

equivalent two-level sector information. In order to keep track of the beginning of a sampling period, the simulation time is sampled using a zero order hold and is then passed to the State Implementation block along with the current simulation time. The switching tables presented in Chapter 3 are then implemented using a combination of switch statements and conditionals within the State Implementation block. The only component that varies between the different space vector PWM methods under investigation is the State Implementation block since the switching tables, which are unique to each method, are implemented within this block. Once the desired switching state is found in the State Implementation block, this information is passed to the “Conversion to Switch States” block. The signals for the individual IGBTs within each phase leg are generated within this block.

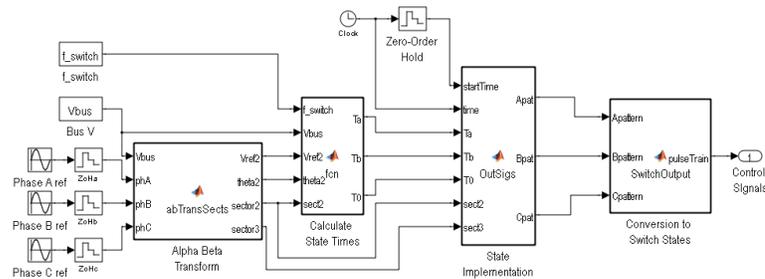


Figure 4.3: The generic space vector PWM pulse generator model.

The model for the generic space vector PWM pulse generator was presented in this section. The overall system model will be presented in the following section.

#### 4.4 Three-Level NPC Inverter System Model

The overall system model is built from a three-level NPC voltage source inverter consisting of standard Simulink components, the IPM machine model, and the space vector PWM pulse generator developed earlier in this chapter. The complete system model is shown in Figure 4.4. The standard three-level bridge found in the SimPowerSystems toolbox of Simulink is used to model the three-level NPC inverter. By using this block instead of creating a new block to model the inverter, simulation speed is increased, and the simulation convergence is somewhat improved. However, the three-level bridge model does not include the turn-on time nor the turn-off time of the IGBTs. For this thesis, these times do not need to be modeled since this investigation is focused on examining the inherent properties of the space vector PWM methods. The additional non-ideality of the inverter is not necessary in this case. The dc bus consists of two series-connected capacitors, a small source resistance to meet simulation logic requirements, and two dc sources in series with a ground connection between them. The ground connection at this location improves simulation stability without influencing the inverter operation. The dc bus voltage is selected to be  $V_{bus} = 360V$ . This value was chosen because at the rated operation of the IPM machine, the output voltage is relatively close to its maximum value but does not exceed it. For the majority of the simulations, the total bus capacitance is fixed at

$C_{bus} = 4$  mF. The IPM machine model and the space vector PWM generator model are connected to the inverter as shown in Figure 4.4.

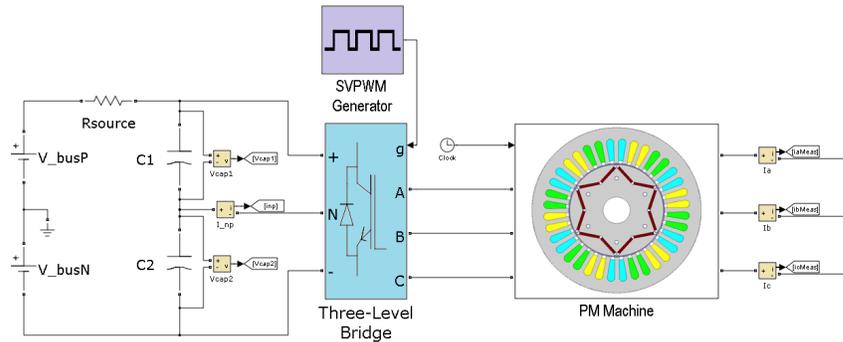


Figure 4.4: System model including inverter, space vector PWM generator, and PM machine.

Two machine loading conditions were simulated: rated speed, rated load and half rated speed, rated load. These two operating conditions were chosen so that the output current would remain constant between the simulations while forcing the inverter into two different modes of operation. At rated speed, the inverter operates in three-level mode, while at half speed, the inverter operates in two-level mode. This difference is due to the different magnitudes of the desired output voltages in each case. The number of sampling periods per fundamental cycle is fixed at 36 samples for both machine operating conditions. This implies that the sampling period varies with the output frequency, and thus varies with the motor speed. By maintaining a constant 36 samples per cycle, the relative sampling of the reference signals is not changed from one operating point to another operating point. As stated previously, a

variable step discrete solver with a maximum time step of 1 microsecond is used for the simulation.

The simulation models for the drive system were presented in Chapter 4. In particular, a circuit model for the IPM machine based on its state space representation, the generic form of the space vector PWM pulse generator, and the overall system model were presented. The results of the simulations for each of the three PWM methods are presented in Chapter 5, and the three methods are compared based on these results.

## **Chapter 5**

### **Simulation Results and Analysis**

In this chapter, the simulation results for each of the three space vector PWM methods with the IPM machine load are presented. First, the tools used in the analysis of the PWM methods are explained. Then the results for Method 1, Method 2, and Method 3, each operating at rated speed, rated load and operating at half rated speed, rated load, are discussed in Section 5.2, Section 5.3, and Section 5.4. Finally, the three methods are compared based on several aspects of the results.

#### **5.1 Space Vector PWM Analysis Tools**

Each three-level space vector PWM method under investigation is evaluated using several analysis tools. In this investigation four signals of interest are considered: the line-to-neutral voltage, the line-to-line voltage, the phase current, and the neutral point current. The first analysis tool is the time domain plots of these signals. Although a time domain plot cannot be used to make conclusions on its own, a good overall understanding about the nature of the signal can be gained from it. If severe distortion

is present in a signal, it is often visible in the time domain plot. Thus time domain plots are useful as an initial check for signal correctness and quality. The root mean square (rms) value of the neutral point current is also included to help create a more meaningful comparison between the different methods. For a generic discrete signal  $x = \{x_1, x_2, \dots, x_k\}$  with  $k$  samples, the rms value of the signal is defined as follows:

$$x_{rms} = \sqrt{\frac{1}{k} \sum_{i=1}^k x_i^2} \quad (5.1)$$

The second analysis tool is the space vector transform of the line-to-neutral voltages and the phase currents, which reflects the trajectory of the quantity within the  $(\alpha - \beta)$  plane. In the case of a balanced purely sinusoidal phase current, the current space vector would trace a circle centered at the origin of the  $(\alpha - \beta)$  plane. Thus, any deviations of the current space vector from the path of a circle correspond to distortion in the output phase currents. In contrast, the switching pattern of the inverter is traced by the line-to-neutral voltage space vector. Thus, the corners formed by the voltage space vector should align with the active vectors in the  $(\alpha - \beta)$  plane. Differences between the voltage space vector corners and the corresponding active vectors can be used to quantify imbalances in the dc bus neutral point caused by the space vector PWM method. In this thesis, the 2-norm of the difference between the output voltage space vector and the corresponding active vector is used for comparing

neutral point imbalance between space vector PWM methods. For a generic vector  $\bar{V} = x + jy$  in the  $(\alpha - \beta)$  plane, the 2-norm is defined as in Equation 5.2.

$$\|\bar{V}\| = \sqrt{x^2 + y^2} \quad (5.2)$$

The final analysis tool is the application of the Fast Fourier Transform (FFT) to the line-to-neutral voltage, the line-to-line voltage, and the phase current to obtain the harmonic spectra of these signals. The harmonic spectrum of a signal provides insight into the frequency components present in that signal. In this investigation, a Bohman window is applied to the data instead of the common rectangular window. Although it is beyond the scope of this thesis to provide a detailed explanation on applying windows to data before applying the FFT, it is sufficient to note that the Bohman window has a faster sidelobe fall off than the rectangular window [68]. This prevents smaller harmonic components from being hidden by nearby larger harmonic components. The total harmonic distortion (THD) of each of these signals is also calculated. The definition of the THD of a voltage including all harmonics up to the  $n^{th}$  harmonic is given in Equation 5.3. The current total harmonic distortion is defined similarly.

$$V_{THD} = \frac{\sqrt{\sum_{h=2}^n V_h^2}}{V_1} \quad (5.3)$$

Several other analysis tools for PWM strategies exist beyond those presented here [53]. The analysis in this thesis is limited to these three tools to allow for a wider investigation of space vector PWM methods as well as inverter operating conditions.

## 5.2 Results and Analysis for Method 1

### 5.2.1 Rated Speed, Rated Load Results and Analysis

In this section, the results from Method 1 with the machine operating at rated speed and rated load are examined. The time domain plots of the line-to-neutral voltages  $v_{An}$ ,  $v_{Bn}$ , and  $v_{Cn}$  as well as their corresponding harmonic spectra in per unit (p.u.) are shown in Figure 5.1 through Figure 5.6. It is clear from the time domain plots that the line-to-neutral voltages are heavily distorted by the back emf of the machine. By examining the frequency plots, it can be seen that this distortion is caused by a significant third harmonic, which is over 40% of the fundamental, and a smaller ninth harmonic. The remainder of the harmonic content is visible in the side bands around harmonics of the sampling frequency  $f_s = 6210$  Hz.

The time domain plots of the line-to-line voltages  $v_{AB}$ ,  $v_{BC}$ , and  $v_{CA}$  as well as their corresponding harmonic spectra are shown in Figure 5.7 through Figure 5.12. As opposed to the line-to-neutral voltages, the line-to-line voltages have the typical three-level output voltage shape. When inspecting the frequency plots, it can be seen that the large third harmonic components and the ninth harmonic components

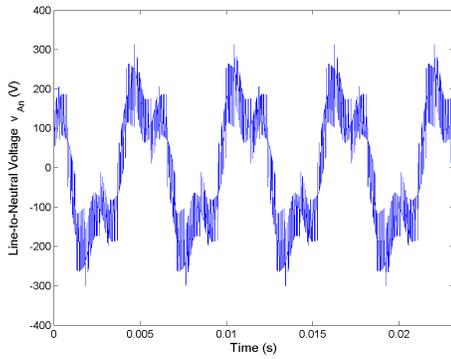


Figure 5.1: Line-to-neutral voltage  $v_{An}$  for Method 1 rated speed, rated load.

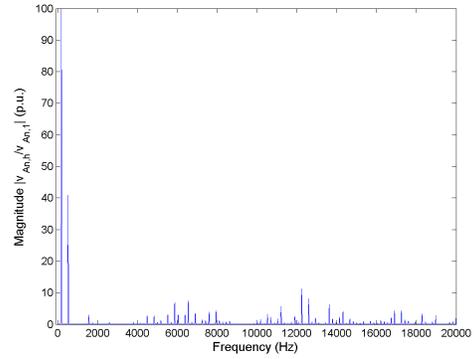


Figure 5.2: FFT of line-to-neutral voltage  $v_{An}$  for Method 1 rated speed, rated load.

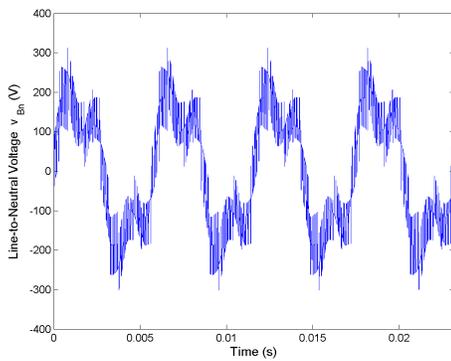


Figure 5.3: Line-to-neutral voltage  $v_{Bn}$  for Method 1 rated speed, rated load.

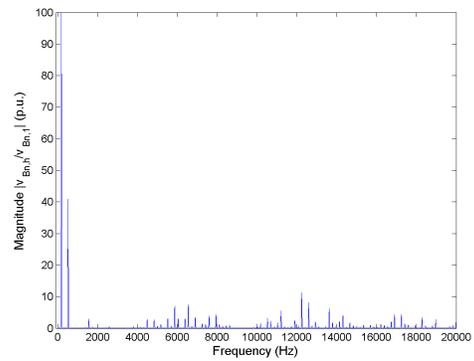


Figure 5.4: FFT of line-to-neutral voltage  $v_{Bn}$  for Method 1 rated speed, rated load.

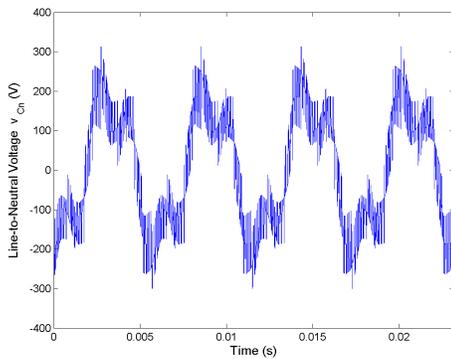


Figure 5.5: Line-to-neutral voltage  $v_{Cn}$  for Method 1 rated speed, rated load.

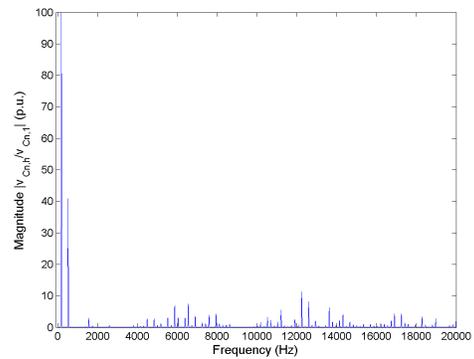


Figure 5.6: FFT of line-to-neutral voltage  $v_{Cn}$  for Method 1 rated speed, rated load.

from the line-to-neutral voltages were eliminated from the line-to-line voltages. The remainder of the harmonic content is caused by the PWM switching pattern and is present in the side bands of the harmonics of the sampling frequency.

The time domain plots of the phase currents  $i_A$ ,  $i_B$ , and  $i_C$  as well as their corresponding harmonic spectra are shown in Figure 5.13 through Figure 5.18. From the time domain plots, the currents appear to be nearly sinusoidal. This is confirmed in the frequency plots of the currents, which are scaled in decibels (dB) as opposed to per unit because the harmonic components are very small in relation to the fundamental. For reference, 0.1% of the fundamental corresponds to -60 dB, so it is reasonable to assume all harmonics below -60 dB are simply artifacts of the FFT. As in the case of the voltage, much of the harmonic content is located in the side bands of the harmonics of the sampling frequency. However, a relatively significant fifth harmonic, seventh harmonic, and eleventh harmonic also exist. As a percentage of the fundamental, the fifth harmonic component is approximately 1.73%, the seventh harmonic is approximately 0.35%, and the eleventh harmonic component is approximately 0.55%. These additional harmonics are most likely caused by the back emf of the IPM machine, which also contains these harmonics.

The space vector plot of the line-to-neutral voltages is presented in Figure 5.19. For this PWM method, the voltage space vector appears hexagonal with equilateral triangles lining the edge. The line segments connecting the vertices of the triangles are

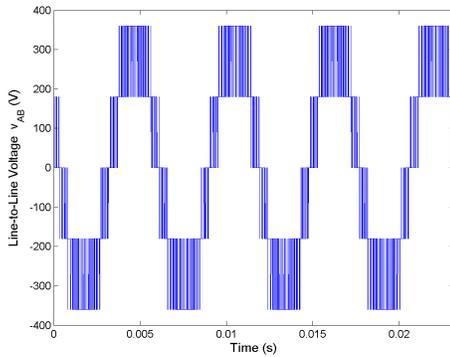


Figure 5.7: Line-to-line voltage  $v_{AB}$  for Method 1 rated speed, rated load.

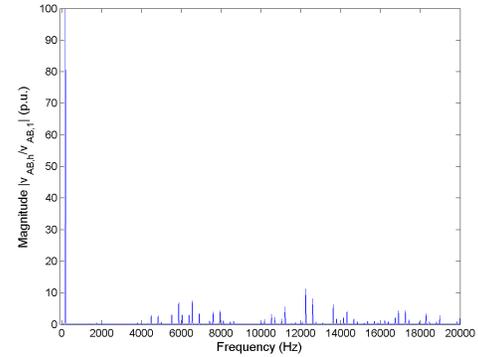


Figure 5.8: FFT of line-to-line voltage  $v_{AB}$  for Method 1 rated speed, rated load.

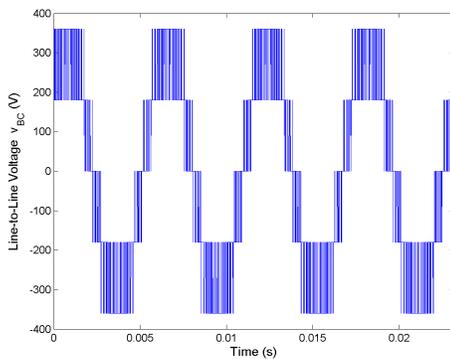


Figure 5.9: Line-to-line voltage  $v_{BC}$  for Method 1 rated speed, rated load.

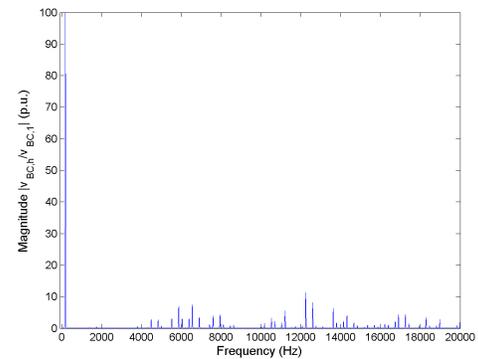


Figure 5.10: FFT of line-to-line voltage  $v_{BC}$  for Method 1 rated speed, rated load.

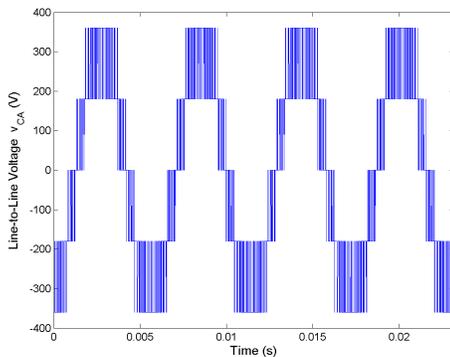


Figure 5.11: Line-to-line voltage  $v_{CA}$  for Method 1 rated speed, rated load.

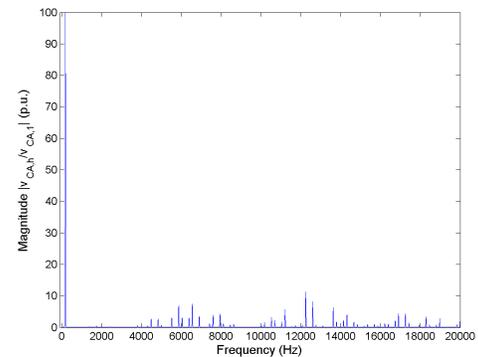


Figure 5.12: FFT of line-to-line voltage  $v_{CA}$  for Method 1 rated speed, rated load.

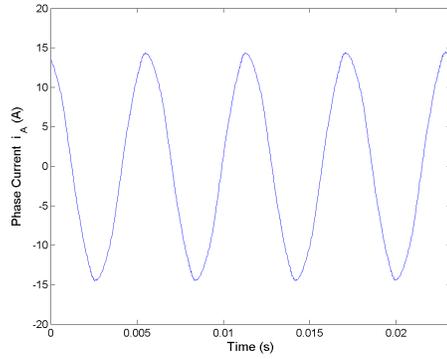


Figure 5.13: Phase current  $i_A$  for Method 1 rated speed, rated load.

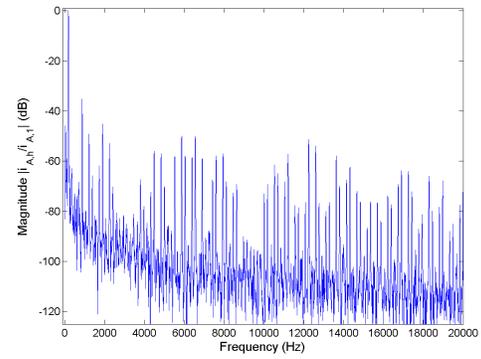


Figure 5.14: FFT of phase current  $i_A$  for Method 1 rated speed, rated load.

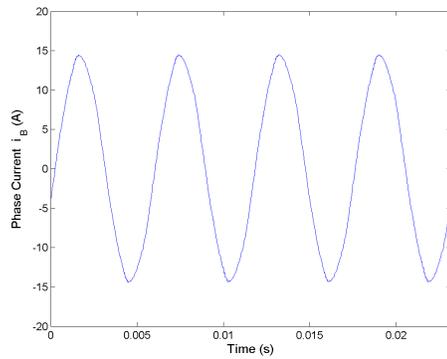


Figure 5.15: Phase current  $i_B$  for Method 1 rated speed, rated load.

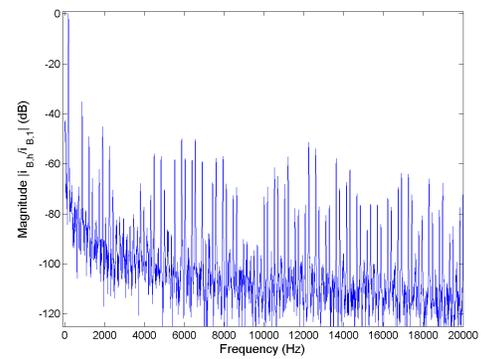


Figure 5.16: FFT of phase current  $i_B$  for Method 1 rated speed, rated load.

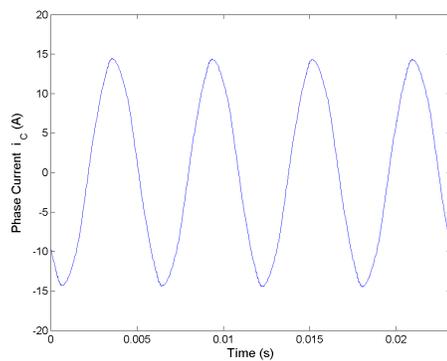


Figure 5.17: Phase current  $i_C$  for Method 1 rated speed, rated load.

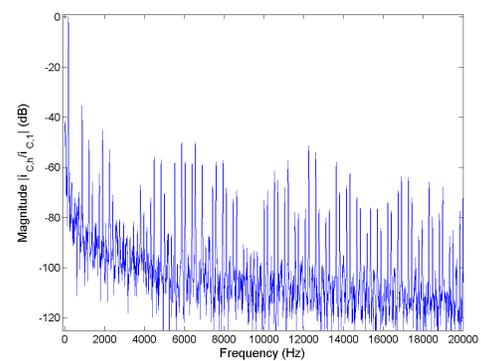


Figure 5.18: FFT of phase current  $i_C$  for Method 1 rated speed, rated load.

added by MATLAB and give an indirect indication of the switching pattern. When two vertices are connected by a line segment, then the PWM method consecutively switches between those two voltage vectors at some point during the fundamental cycle. Since triangles are formed by the switching pattern in this space vector plot, this PWM method is shown to cycle completely through the three nearest voltage vectors during each sampling period. Vertices appear every  $60^\circ e$ . beginning at  $0^\circ e$ . in the cases of the small vectors and the large vectors. Vertices appear every  $60^\circ e$ . beginning at  $30^\circ e$ . in the case of the medium vectors. The vertices appear to align fairly well with these angles, so the imbalance in the neutral point of the dc bus is not significant. The calculated values of the 2-norm of the differences between the vertices and the corresponding voltage vectors are presented in Section 5.5.1.

The space vector plot of the phase currents and the time domain plot of the neutral point current are presented in Figure 5.20 and Figure 5.21. The current space vector is circular in general, but it has six flattened sides approximately every  $60^\circ e$ . This is most likely an effect of the fifth harmonic, the seventh harmonic, and the eleventh harmonic previously seen in the frequency plots of the current. The slightly jagged deviations in the trajectory are due to the sampling frequency of the PWM method. In Figure 5.21, the neutral point current is plotted in the time domain. The jagged appearance of the waveform is due to the sampling frequency of the inverter. The most important aspect about this figure is that the neutral point current seems

to be split fairly evenly between the positive half of the cycle and the negative half of the cycle. When the neutral point current is balanced in this way, it has a lesser effect on the neutral point voltage balance.

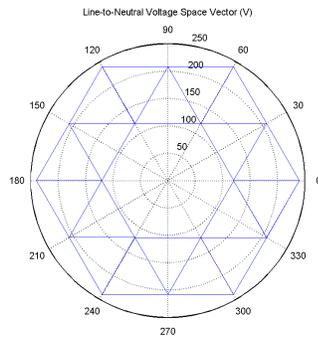


Figure 5.19: Space vector of line-to-neutral voltages for Method 1 rated speed, rated load.

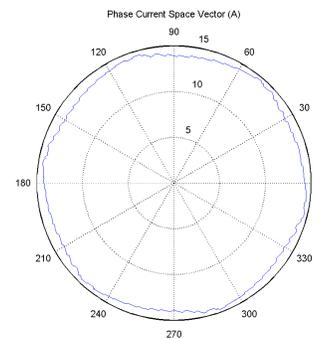


Figure 5.20: Space vector of phase currents for Method 1 rated speed, rated load.

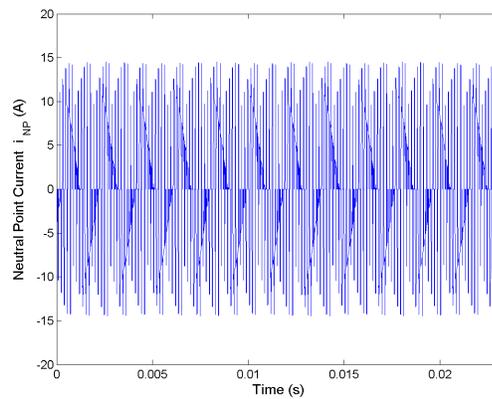


Figure 5.21: Neutral point current  $i_{NP}$  for Method 1 rated speed, rated load.

### 5.2.2 Half Rated Speed, Rated Load Results and Analysis

In this section, the results from Method 1 with the machine operating at half speed and rated load are examined. The time domain plots of the line-to-neutral voltages  $v_{An}$ ,  $v_{Bn}$ , and  $v_{Cn}$  as well as their corresponding harmonic spectra in per unit are shown in Figure 5.22 through Figure 5.27. It is clear from the time domain plots that the line-to-neutral voltages are heavily distorted by the back emf of the machine. By examining the frequency plots, it can be seen that these line-to-neutral voltages have a significant third harmonic slightly less than 40% of the fundamental and a smaller ninth harmonic just as in the rated speed case. The remainder of the harmonic content is visible in the side bands around harmonics of the sampling frequency  $f_s = 3105$  Hz, though in this case, the harmonics in the side bands of  $(2f_s)$  are more significant than those in the side bands of  $f_s$ .

The time domain plots of the line-to-line voltages  $v_{AB}$ ,  $v_{BC}$ , and  $v_{CA}$  as well as their corresponding harmonic spectra are shown in Figure 5.28 through Figure 5.33. From the time domain plots, it is clear that the inverter is operating in two-level mode as expected for the half rated speed case. Again, the large third harmonic components and the ninth harmonic components from the line-to-neutral voltages were eliminated from the line-to-line voltages due to the Y-connection of the machine winding. The remainder of the harmonic content is caused by the PWM switching pattern and is present in the side bands of the harmonics of the sampling frequency, particularly

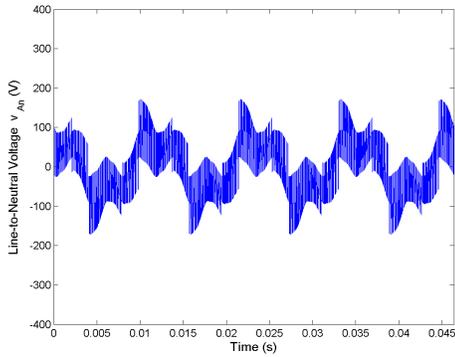


Figure 5.22: Line-to-neutral voltage  $v_{An}$  for Method 1 half rated speed, rated load.

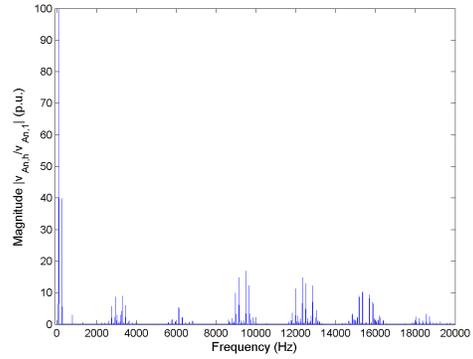


Figure 5.23: FFT of line-to-neutral voltage  $v_{An}$  for Method 1 half rated speed, rated load.

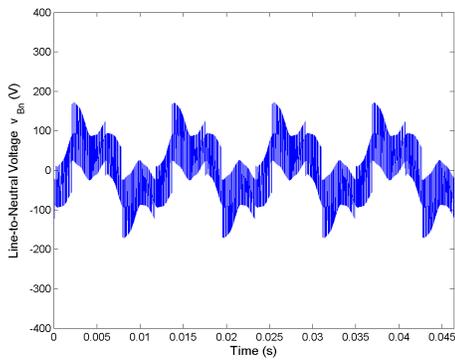


Figure 5.24: Line-to-neutral voltage  $v_{Bn}$  for Method 1 half rated speed, rated load.

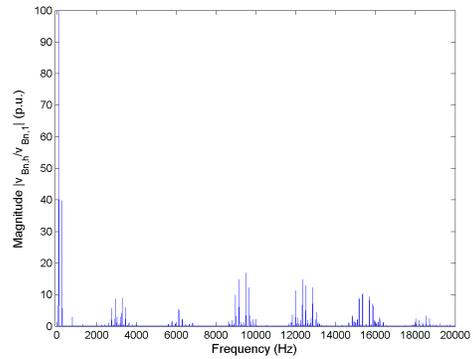


Figure 5.25: FFT of line-to-neutral voltage  $v_{Bn}$  for Method 1 half rated speed, rated load.

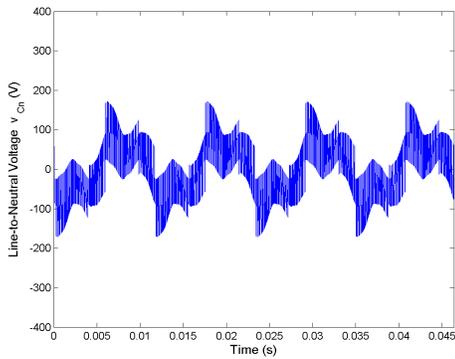


Figure 5.26: Line-to-neutral voltage  $v_{Cn}$  for Method 1 half rated speed, rated load.

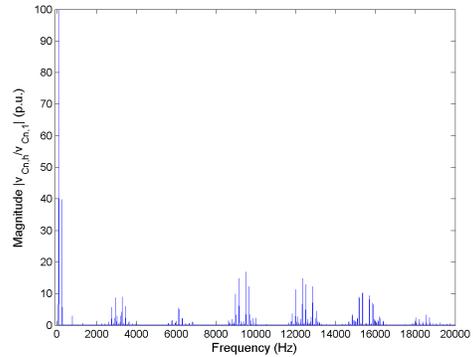


Figure 5.27: FFT of line-to-neutral voltage  $v_{Cn}$  for Method 1 half rated speed, rated load.

$(2f_s)$ .

The time domain plots of the phase currents  $i_A$ ,  $i_B$ , and  $i_C$  as well as their corresponding harmonic spectra are shown in Figure 5.34 through Figure 5.39. From the time domain plots, the currents appear to be nearly sinusoidal. This is confirmed in the frequency plots of the currents, which are scaled in decibels once again as opposed to per unit because the harmonic components are very small in relation to the fundamental. Again, all frequency content below -60 dB is taken to be artifacts of the FFT. Similar to the voltage, much of the harmonic content is located in the side bands of the second harmonic of the sampling frequency. However, a relatively significant fifth harmonic, seventh harmonic, and eleventh harmonic also exist. As a percentage of the fundamental, the fifth harmonic component is approximately 1.65%, the seventh harmonic is approximately 0.35%, and the eleventh harmonic component is approximately 0.55%. The fifth harmonic decreases slightly at half rated speed, but the seventh and eleventh harmonics remain constant.

The space vector plot of the line-to-neutral voltages is presented in Figure 5.40. For this PWM method with the machine operating at half speed, full load, the voltage space vector has the appearance of the hexagon that is normally associated with a two-level inverter. The line segments connecting the vertices of the triangles within the hexagon are added by MATLAB and give an indirect indication of the switching pattern. From this space vector plot, it becomes apparent that only zero vectors

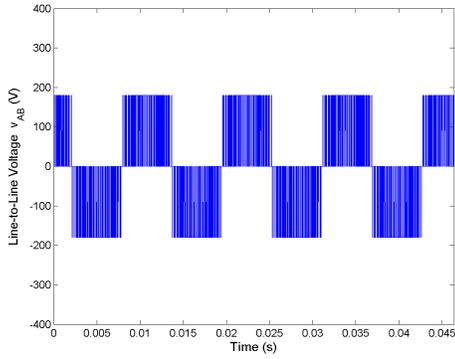


Figure 5.28: Line-to-line voltage  $v_{AB}$  for Method 1 half rated speed, rated load.

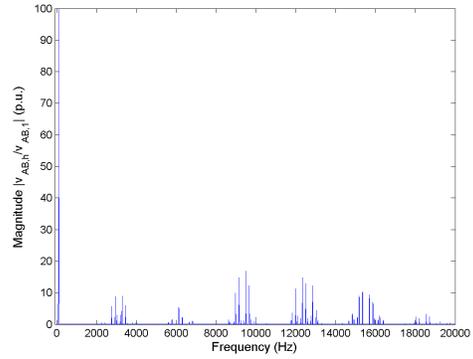


Figure 5.29: FFT of line-to-line voltage  $v_{AB}$  for Method 1 half rated speed, rated load.

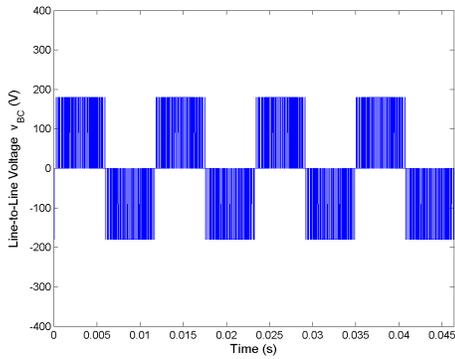


Figure 5.30: Line-to-line voltage  $v_{BC}$  for Method 1 half rated speed, rated load.

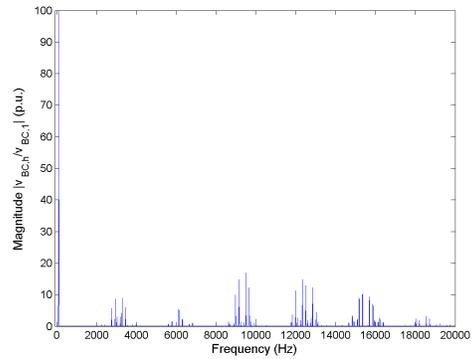


Figure 5.31: FFT of line-to-line voltage  $v_{BC}$  for Method 1 half rated speed, rated load.

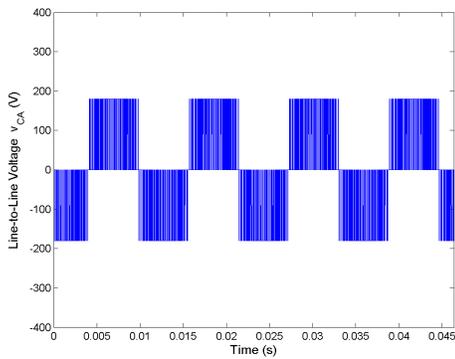


Figure 5.32: Line-to-line voltage  $v_{CA}$  for Method 1 half rated speed, rated load.

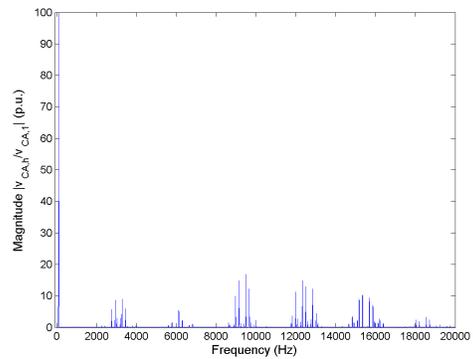


Figure 5.33: FFT of line-to-line voltage  $v_{CA}$  for Method 1 half rated speed, rated load.

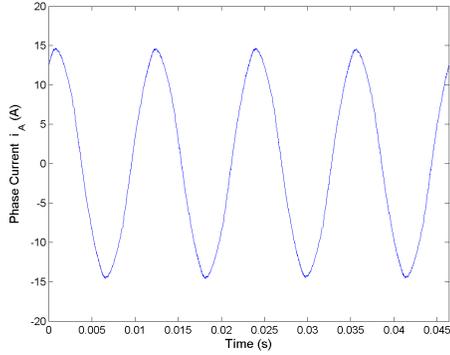


Figure 5.34: Phase current  $i_A$  for Method 1 half rated speed, rated load.

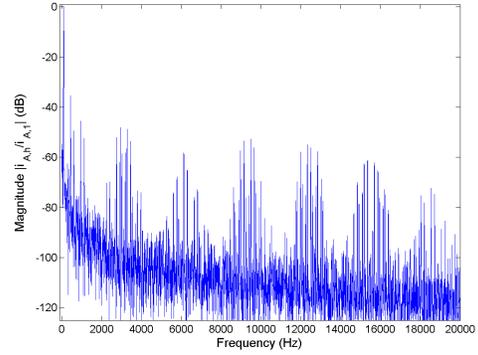


Figure 5.35: FFT of phase current  $i_A$  for Method 1 half rated speed, rated load.

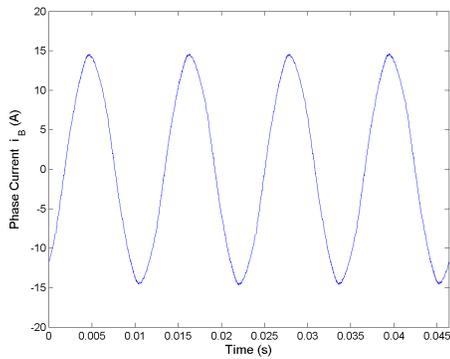


Figure 5.36: Phase current  $i_B$  for Method 1 half rated speed, rated load.

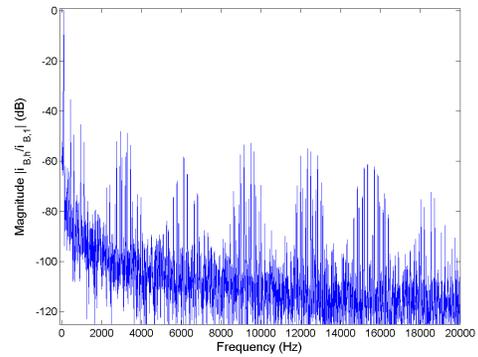


Figure 5.37: FFT of phase current  $i_B$  for Method 1 half rated speed, rated load.

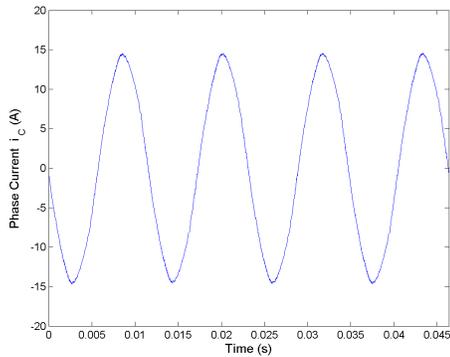


Figure 5.38: Phase current  $i_C$  for Method 1 half rated speed, rated load.

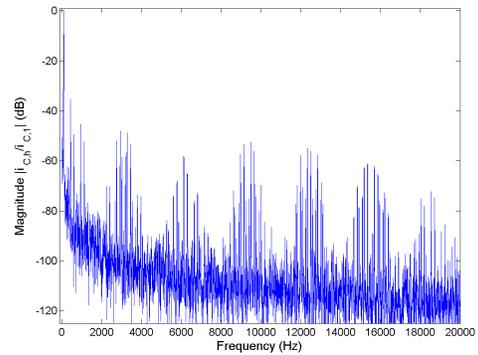


Figure 5.39: FFT of phase current  $i_C$  for Method 1 half rated speed, rated load.

and small vectors are used at this operating point, hence its operation as a two-level inverter. Since triangles are formed by the switching pattern, this PWM method is shown to cycle completely through the three nearest voltage vectors each sampling period as in its operation at full speed. The vertices of the triangles appear to align fairly well with the locations of the small vectors, which indicates the imbalance in the neutral point of the dc bus is not significant. The calculated values of the 2-norm of the differences between the vertices and the corresponding voltage vectors are presented in Section 5.5.2.

The space vector plot of the phase currents and the time domain plot of the neutral point current are presented in Figure 5.41 and Figure 5.42. The current space vector is circular in general, but it has six flattened sides as in the case of full speed operation. This is most likely an effect of the fifth harmonic, the seventh harmonic, and the eleventh harmonic previously seen in the frequency plots of the current. The slightly jagged deviations in the trajectory are due to the sampling frequency of the PWM method. In Figure 5.42, the neutral point current is plotted in the time domain. The high frequency component of the waveform is due to the sampling frequency of the inverter. Once again, the neutral point current seems to be split fairly evenly between the positive half of the cycle and the negative half of the cycle, indicating that it has a lesser effect on the neutral point voltage balance.

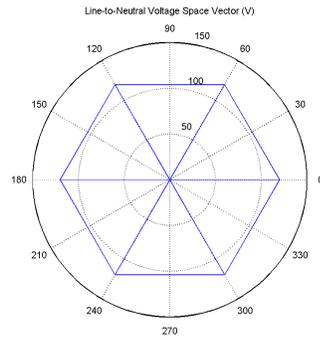


Figure 5.40: Space vector of line-to-neutral voltages for Method 1 half rated speed, rated load.

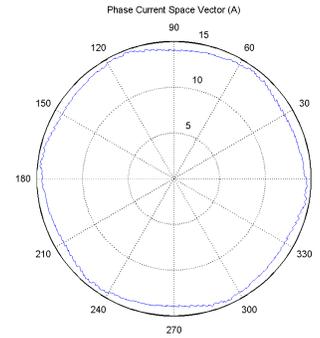


Figure 5.41: Space vector of phase currents for Method 1 half rated speed, rated load.

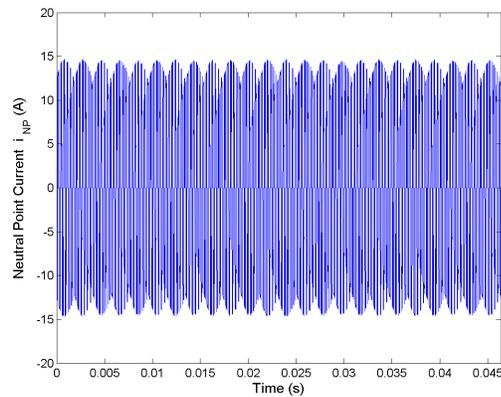


Figure 5.42: Neutral point current  $i_{NP}$  for Method 1 half rated speed, rated load.

### 5.3 Results and Analysis for Method 2

#### 5.3.1 Rated Speed, Rated Load Results and Analysis

In this section, the results from Method 2 with the machine operating at rated speed and rated load are examined. The time domain plots of the line-to-neutral voltages  $v_{An}$ ,  $v_{Bn}$ , and  $v_{Cn}$  as well as their corresponding harmonic spectra in per unit are shown in Figure 5.43 through Figure 5.48. In this case, the time domain plots appear to be relatively similar to those of PWM Method 1 in the case of operation at rated speed and rated load. However, by examining the frequency plots, it is clear that these line-to-neutral voltages are significantly more distorted than those of Method 1. In addition to the harmonics caused by the sampling frequency  $f_s = 6210$  Hz, the second harmonic through the ninth harmonic are present as well. The presence of the even harmonics explains the lack of symmetry between the positive and negative halves of the voltages. These additional harmonics are caused by a severe dc bus neutral point imbalance that will be demonstrated in the voltage space vector.

The time domain plots of the line-to-line voltages  $v_{AB}$ ,  $v_{BC}$ , and  $v_{CA}$  as well as their corresponding harmonic spectra are shown in Figure 5.49 through Figure 5.54. Unlike the Method 1 line-to-line voltages, the Method 2 line-to-line voltages are visibly distorted in the time domain plots. When comparing the frequency plots to those of the line-to-neutral voltages, many of the same harmonics appear. In particular, the

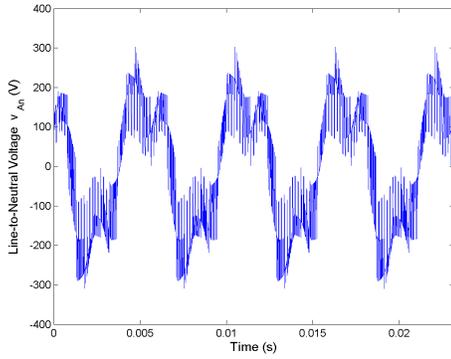


Figure 5.43: Line-to-neutral voltage  $v_{An}$  for Method 2 rated speed, rated load.

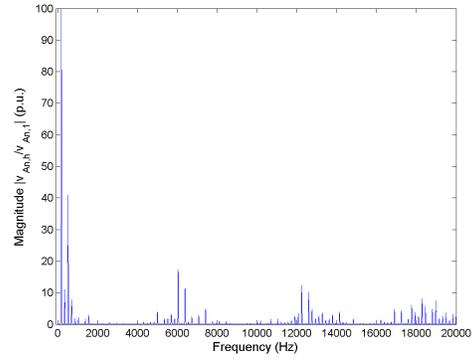


Figure 5.44: FFT of line-to-neutral voltage  $v_{An}$  for Method 2 rated speed, rated load.

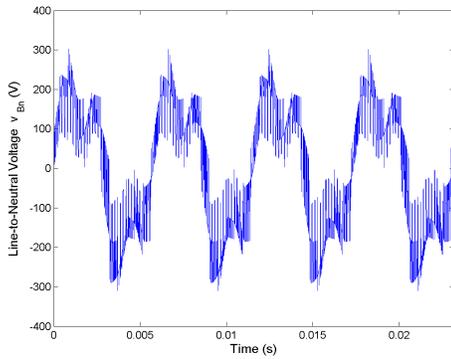


Figure 5.45: Line-to-neutral voltage  $v_{Bn}$  for Method 2 rated speed, rated load.

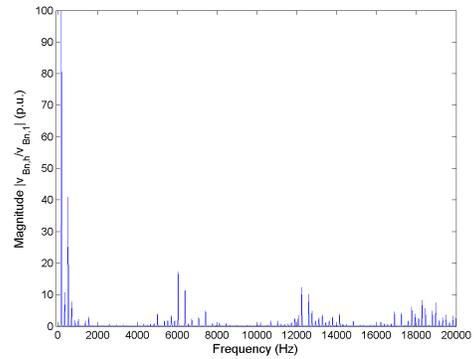


Figure 5.46: FFT of line-to-neutral voltage  $v_{Bn}$  for Method 2 rated speed, rated load.

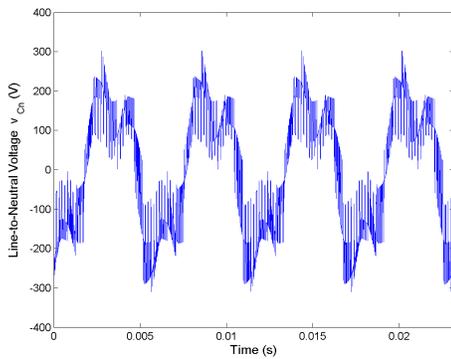


Figure 5.47: Line-to-neutral voltage  $v_{Cn}$  for Method 2 rated speed, rated load.

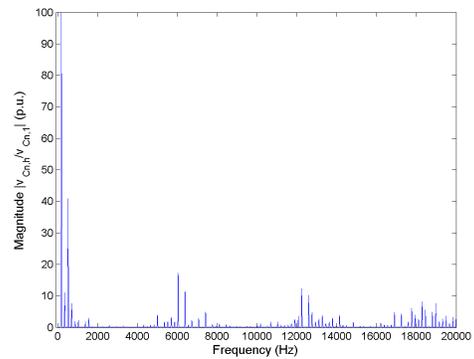


Figure 5.48: FFT of line-to-neutral voltage  $v_{Cn}$  for Method 2 rated speed, rated load.

second harmonic, the fourth harmonic, the fifth harmonic, and the eighth harmonic are present in the line-to-line voltages. The third harmonic, the sixth harmonic, and the ninth harmonic that were also in the line-to-neutral voltages are not present in the line-to-line voltages. This is another indicator that a significant imbalance in the neutral point of the dc bus exists for this method.

The time domain plots of the phase currents  $i_A$ ,  $i_B$ , and  $i_C$  as well as their corresponding harmonic spectra are shown in Figure 5.55 through Figure 5.60. In the time domain plots, the currents appear reasonably sinusoidal, but they are slightly pointed near the peaks. This is confirmed in the frequency plots of the currents. Unlike the currents found using PWM Method 1, the Method 2 currents contain a second harmonic (8.37% of the fundamental), a fourth harmonic (2.41% of the fundamental), a fifth harmonic (1.15% of the fundamental), a seventh harmonic (0.37% of the fundamental), an eighth harmonic (0.36% of the fundamental), an eleventh harmonic (0.55% of the fundamental), and a thirteenth harmonic (0.20% of the fundamental). These additional harmonics are caused by the additional distortion in the voltages.

The space vector plot of the line-to-neutral voltages is presented in Figure 5.61. In this case, the voltage space vector takes the form of two concentric hexagons with line segments radiating out from the vertices of the inner hexagon to the outer hexagon. This is an excellent example of the imbalance in the neutral point caused by the switching pattern of Method 2. The vertices corresponding to the large vectors

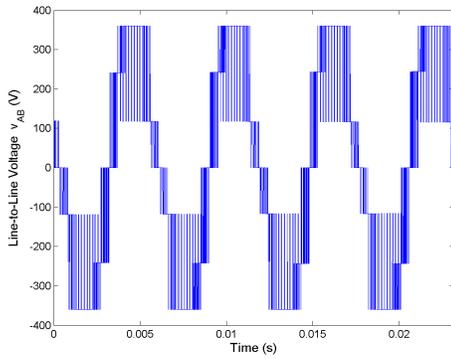


Figure 5.49: Line-to-line voltage  $v_{AB}$  for Method 2 rated speed, rated load.

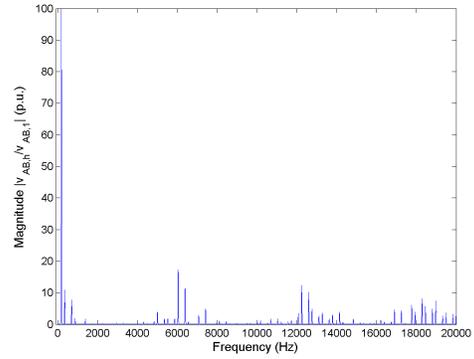


Figure 5.50: FFT of line-to-line voltage  $v_{AB}$  for Method 2 rated speed, rated load.

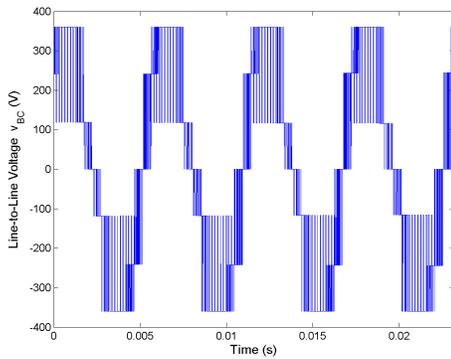


Figure 5.51: Line-to-line voltage  $v_{BC}$  for Method 2 rated speed, rated load.

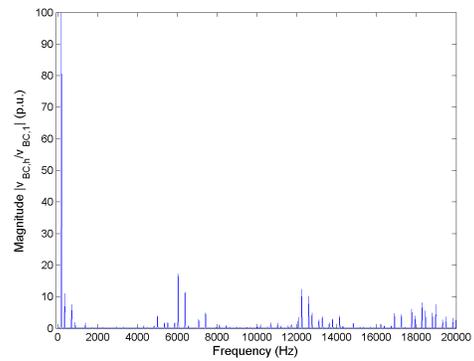


Figure 5.52: FFT of line-to-line voltage  $v_{BC}$  for Method 2 rated speed, rated load.

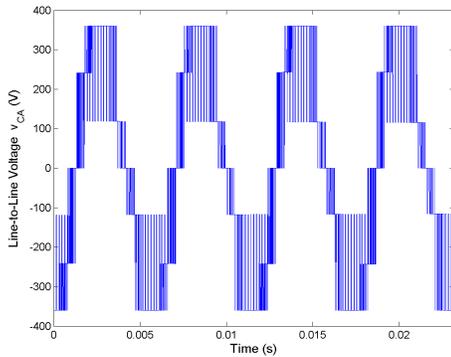


Figure 5.53: Line-to-line voltage  $v_{CA}$  for Method 2 rated speed, rated load.

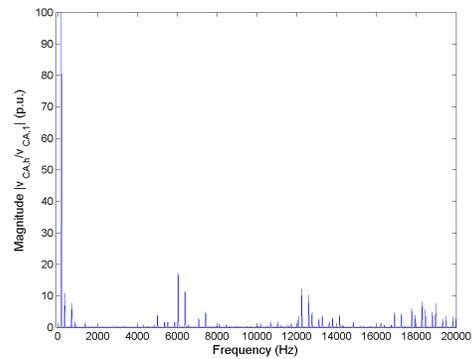


Figure 5.54: FFT of line-to-line voltage  $v_{CA}$  for Method 2 rated speed, rated load.

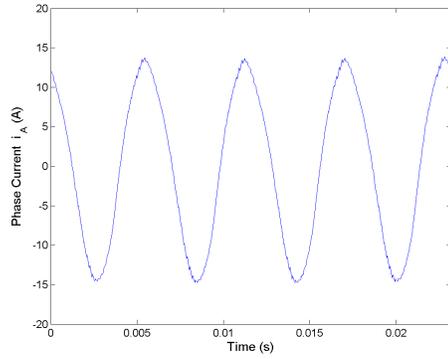


Figure 5.55: Phase current  $i_A$  for Method 2 rated speed, rated load.

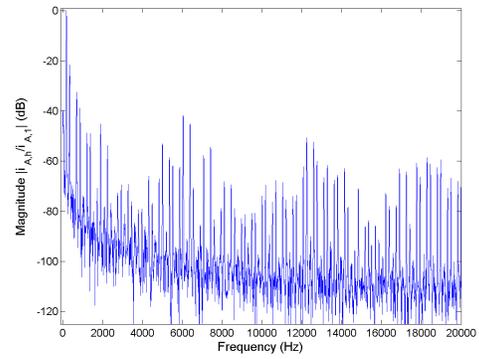


Figure 5.56: FFT of phase current  $i_A$  for Method 2 rated speed, rated load.

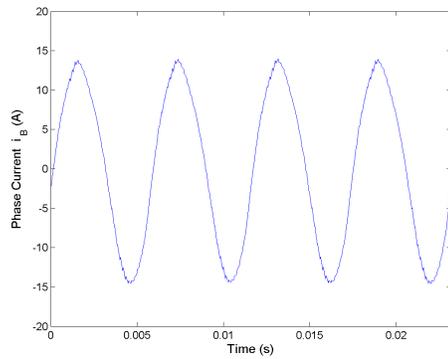


Figure 5.57: Phase current  $i_B$  for Method 2 rated speed, rated load.

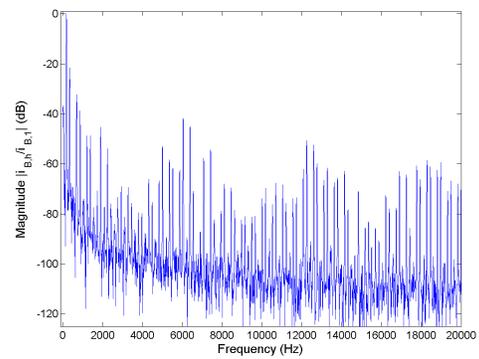


Figure 5.58: FFT of phase current  $i_B$  for Method 2 rated speed, rated load.

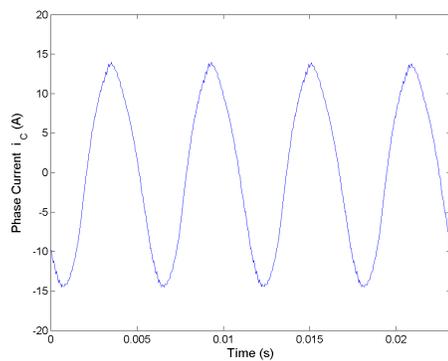


Figure 5.59: Phase current  $i_C$  for Method 2 rated speed, rated load.

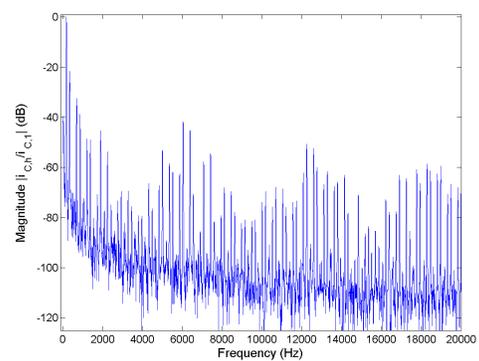


Figure 5.60: FFT of phase current  $i_C$  for Method 2 rated speed, rated load.

are correct because those vectors do not affect, and so are not affected by, the neutral point imbalance. However, the medium vectors have shifted, and both their length and angle have changed. The small vectors have changed solely in length. The calculated values of the 2-norm of the differences between the vertices and the corresponding voltage vectors are presented in Section 5.5.1.

The space vector plot of the phase currents and the time domain plot of the neutral point current are presented in Figure 5.62 and Figure 5.63. Although the currents had appeared reasonably sinusoidal in the time domain, the current space vector is more triangular with rounded corners. This distortion of the trajectory of the current space vector indicates that the neutral point voltage imbalance also degrades the output current quality. This is a particular concern for inverters driving a motor because distorted phase current can produce significant developed torque pulsations. In Figure 5.63, the neutral point current is plotted in the time domain. For the switching pattern of Method 2, the negative portion of the waveform is much more pronounced than the positive portion as a result of using only a positive small vector or only a negative small vector within each sampling period. This weight associated with one half of the neutral point current waveform has a much more significant effect on the neutral point balance than the neutral point current of Method 1.

As expected, the switching pattern of Method 2 severely affected the balance of the neutral point of the dc bus. In an attempt to evaluate Method 2 when functioning

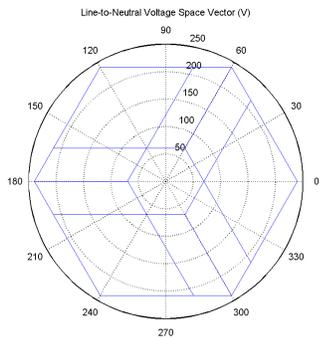


Figure 5.61: Space vector of line-to-neutral voltages for Method 2 rated speed, rated load.

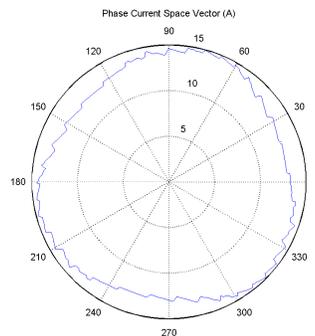


Figure 5.62: Space vector of phase currents for Method 2 rated speed, rated load.

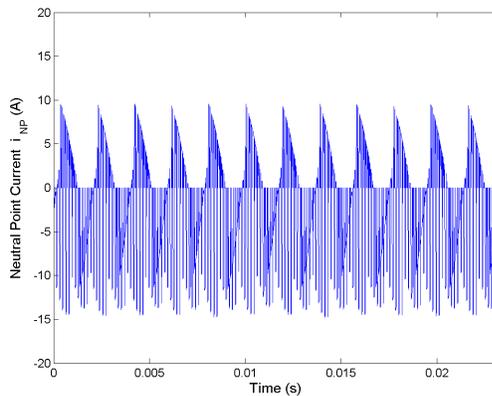


Figure 5.63: Neutral point current  $i_{NP}$  for Method 2 rated speed, rated load.

as intended, the bus capacitance in the simulation was increased from 4 mF to 400 mF. The increase in bus capacitance makes the dc bus stiffer and more resilient to neutral point imbalance. Although this bus capacitance is very unrealistic for an inverter, this change will provide more insight into the qualities of this switching pattern.

The time domain plots of the line-to-neutral voltages  $v_{An}$ ,  $v_{Bn}$ , and  $v_{Cn}$  for

Method 2 with increased bus capacitance as well as their corresponding harmonic spectra in per unit are shown in Figure 5.64 through Figure 5.69. The time domain plots of these voltages are much more similar to the line-to-neutral voltages of Method 1 at rated speed, rated load than those produced by the smaller bus capacitance. However, differences can be seen in the frequency plots of the line-to-neutral voltages between Method 1 and Method 2 with increased bus capacitance. In Method 1, the sampling frequency side bands were balanced, while in this case the lower side band harmonics are slightly more prominent than the upper side band harmonics. Regardless, it seems that the increase in bus capacitance improved the line-to-neutral voltages produced by the switching pattern of Method 2.

The time domain plots of the line-to-line voltages  $v_{AB}$ ,  $v_{BC}$ , and  $v_{CA}$  for Method 2 with increased bus capacitance as well as their corresponding harmonic spectra are shown in Figure 5.70 through Figure 5.75. As opposed to the line-to-neutral voltages, the line-to-line voltages have the typical three-level output voltage shape. When inspecting the frequency plots, it can be seen that the large third harmonic components present in the line-to-neutral voltages were eliminated from the line-to-line voltages as expected. The remaining harmonic content is caused by the PWM switching pattern and mostly appears in the side bands of higher harmonics of the sampling frequency.

The time domain plots of the phase currents  $i_A$ ,  $i_B$ , and  $i_C$  for Method 2 with

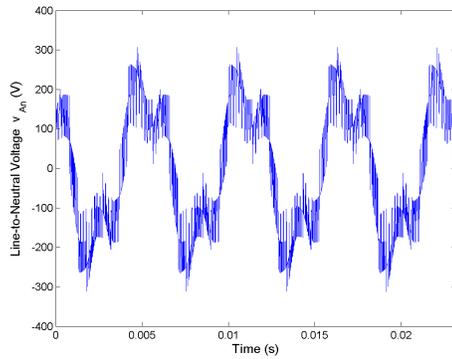


Figure 5.64: Line-to-neutral voltage  $v_{An}$  for Method 2 rated speed, rated load and  $C_{bus} = 400mF$ .

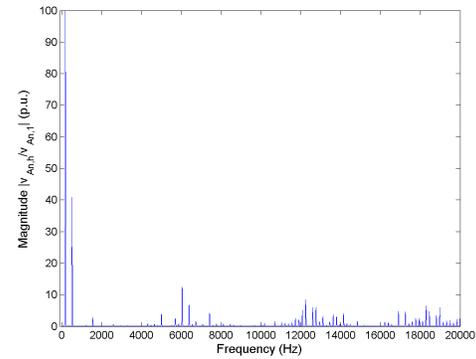


Figure 5.65: FFT of line-to-neutral voltage  $v_{An}$  for Method 2 rated speed, rated load and  $C_{bus} = 400mF$ .

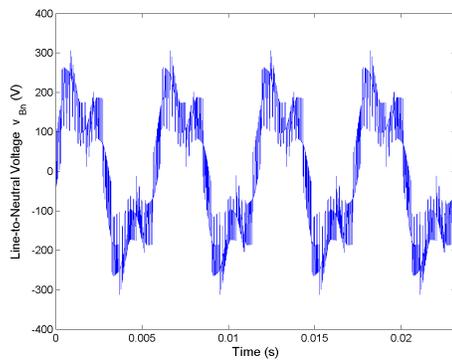


Figure 5.66: Line-to-neutral voltage  $v_{Bn}$  for Method 2 rated speed, rated load and  $C_{bus} = 400mF$ .

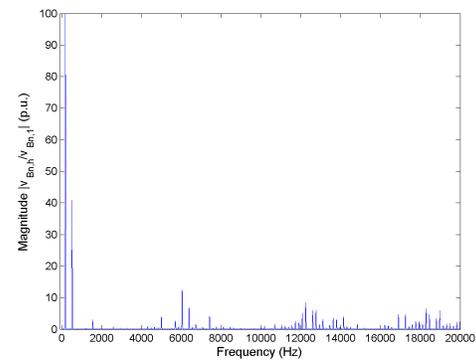


Figure 5.67: FFT of line-to-neutral voltage  $v_{Bn}$  for Method 2 rated speed, rated load and  $C_{bus} = 400mF$ .

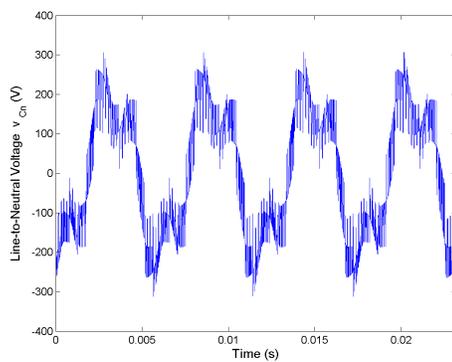


Figure 5.68: Line-to-neutral voltage  $v_{Cn}$  for Method 2 rated speed, rated load and  $C_{bus} = 400mF$ .

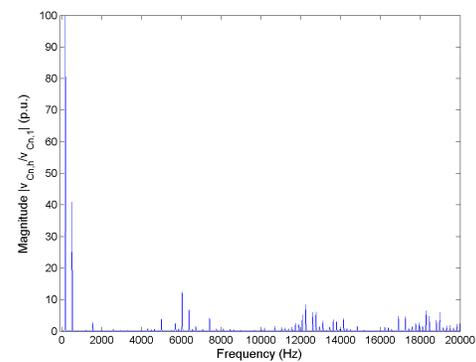


Figure 5.69: FFT of line-to-neutral voltage  $v_{Cn}$  for Method 2 rated speed, rated load and  $C_{bus} = 400mF$ .

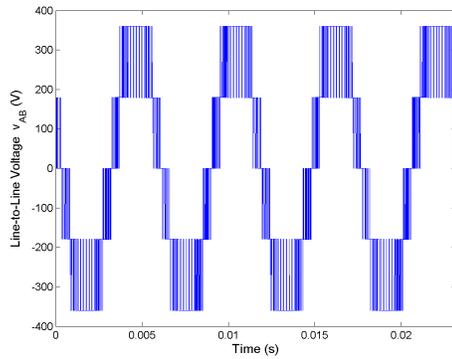


Figure 5.70: Line-to-line voltage  $v_{AB}$  for Method 2 rated speed, rated load and  $C_{bus} = 400mF$ .

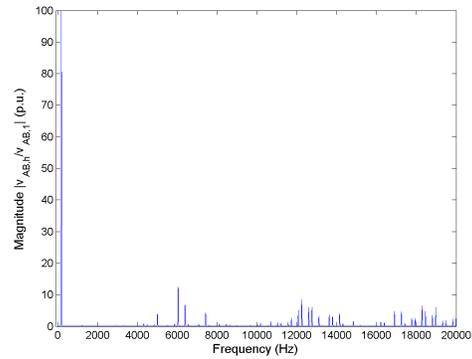


Figure 5.71: FFT of line-to-line voltage  $v_{AB}$  for Method 2 rated speed, rated load and  $C_{bus} = 400mF$ .

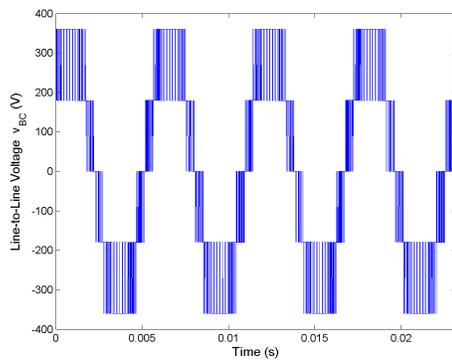


Figure 5.72: Line-to-line voltage  $v_{BC}$  for Method 2 rated speed, rated load and  $C_{bus} = 400mF$ .

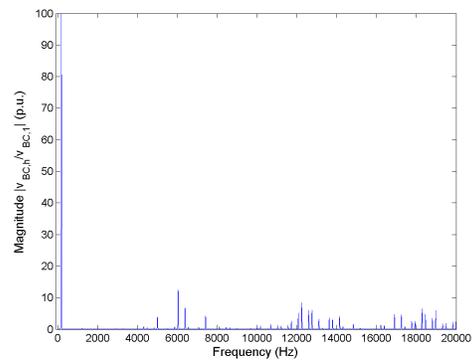


Figure 5.73: FFT of line-to-line voltage  $v_{BC}$  for Method 2 rated speed, rated load and  $C_{bus} = 400mF$ .

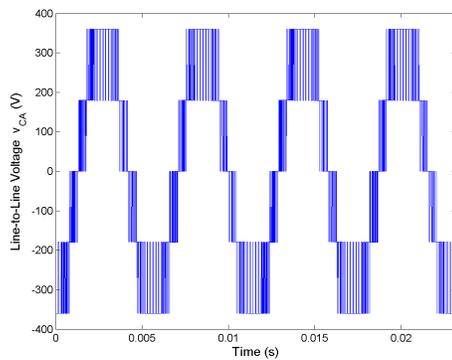


Figure 5.74: Line-to-line voltage  $v_{CA}$  for Method 2 rated speed, rated load and  $C_{bus} = 400mF$ .

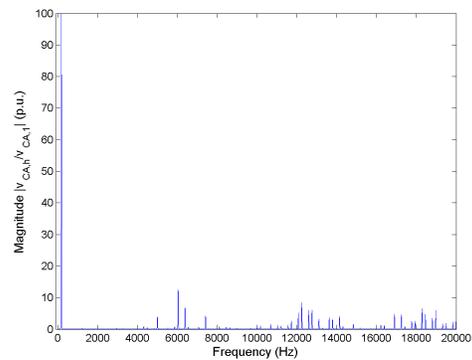


Figure 5.75: FFT of line-to-line voltage  $v_{CA}$  for Method 2 rated speed, rated load and  $C_{bus} = 400mF$ .

increased bus capacitance as well as their corresponding harmonic spectra are shown in Figure 5.76 through Figure 5.81. From the time domain plots, the currents appear to be nearly sinusoidal. This is confirmed in the frequency plots of the currents, which are scaled in decibels. As in the currents produced by Method 1, much of the harmonic content is located in the side bands of the harmonics of the sampling frequency. The fifth harmonic (1.73% of the fundamental), the seventh harmonic (0.37% of the fundamental), and the eleventh harmonic (0.55% of the fundamental) are also relatively significant. Overall, these results are similar to the results from Method 1 operating at rated speed.

The space vector plot of the line-to-neutral voltages for Method 2 with increased bus capacitance is presented in Figure 5.82. For this PWM method, the voltage space vector appears hexagonal with rhombi lining the edges. Since rhombi are formed by this switching pattern as opposed to the triangles formed in the space vector plot from Method 1, the switching pattern of Method 2 is shown to use three out of the four available switching states when applying the three nearest voltage vectors during each sampling period. Unlike the previous case, the voltage vectors of Method 2 with increased bus capacitance seem to have little drift, indicating that the imbalance in the neutral point of the dc bus is not significant. The calculated values of the 2-norm of the differences between the vertices and the corresponding voltage vectors are presented in Section 5.5.1.

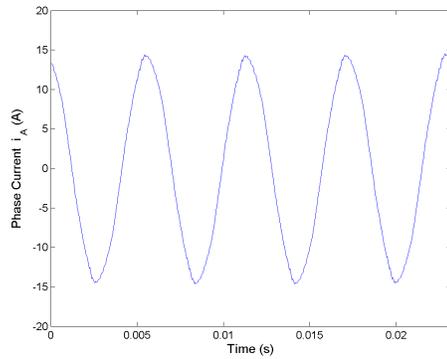


Figure 5.76: Phase current  $i_A$  for Method 2 rated speed, rated load and  $C_{bus} = 400mF$ .

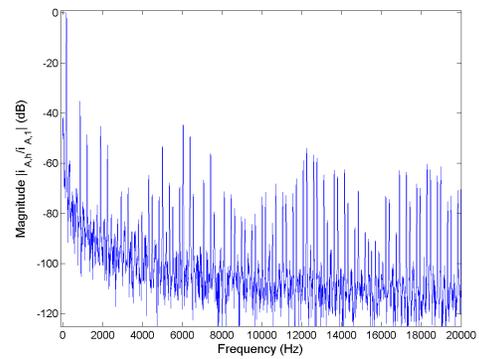


Figure 5.77: FFT of phase current  $i_A$  for Method 2 rated speed, rated load and  $C_{bus} = 400mF$ .

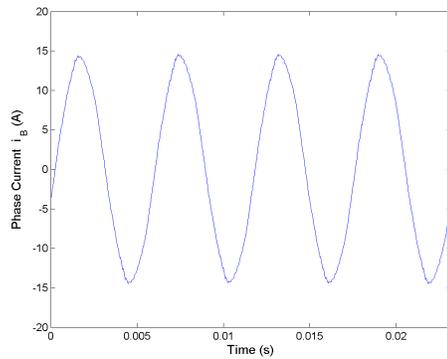


Figure 5.78: Phase current  $i_B$  for Method 2 rated speed, rated load and  $C_{bus} = 400mF$ .

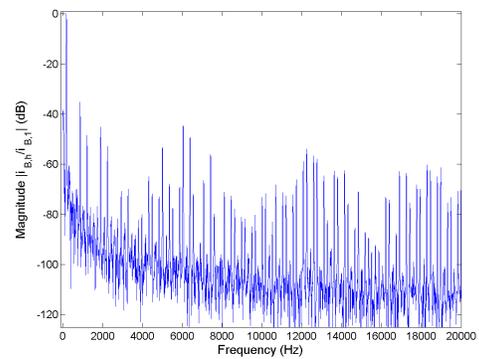


Figure 5.79: FFT of phase current  $i_B$  for Method 2 rated speed, rated load and  $C_{bus} = 400mF$ .

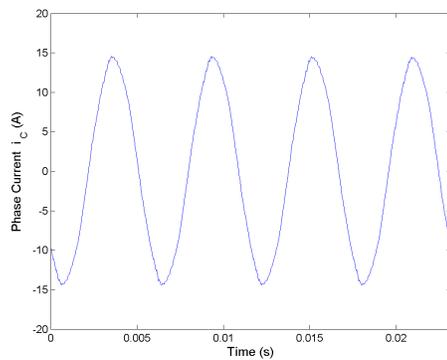


Figure 5.80: Phase current  $i_C$  for Method 2 rated speed, rated load and  $C_{bus} = 400mF$ .

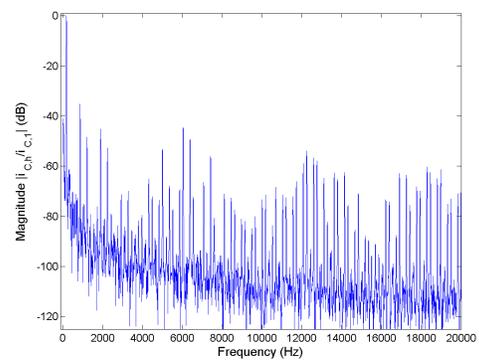


Figure 5.81: FFT of phase current  $i_C$  for Method 2 rated speed, rated load and  $C_{bus} = 400mF$ .

The space vector plot of the phase currents and the time domain plot of the neutral point current for Method 2 with increased bus capacitance are presented in Figure 5.83 and Figure 5.84. The current space vector is mostly circular, and the six flattened sides are not as prominent as in the current vector from Method 1. In Figure 5.21, the neutral point current is plotted in the time domain. Although the neutral point of the dc bus does not vary as much with the larger bus capacitance, the shape of the neutral point current did not change, which implies that the same unbalanced current flows through the neutral point. The only reason the balance of the dc bus voltage does not change significantly is because the larger capacitance increases the bus stiffness, preventing drastic voltage swings despite the presence of the same neutral point current.

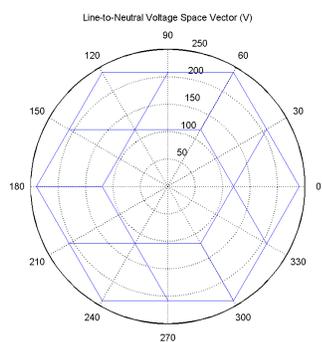


Figure 5.82: Space vector of line-to-neutral voltages for Method 2 rated speed, rated load and  $C_{bus} = 400mF$ .

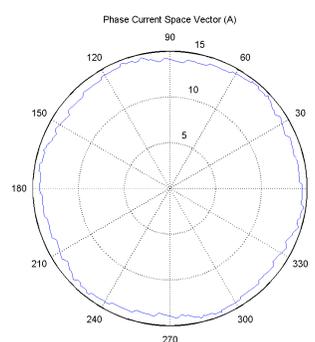


Figure 5.83: Space vector of phase currents for Method 2 rated speed, rated load and  $C_{bus} = 400mF$ .

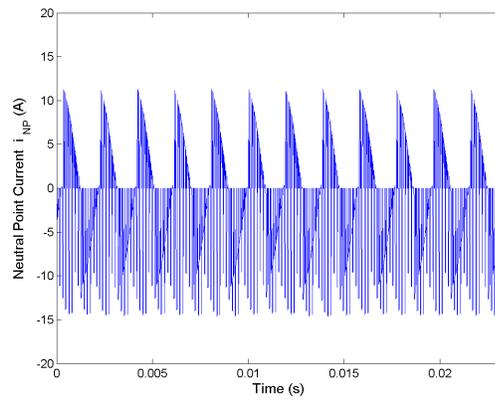


Figure 5.84: Neutral point current  $i_{NP}$  for Method 2 rated speed, rated load and  $C_{bus} = 400mF$ .

### 5.3.2 Half Rated Speed, Rated Load Results and Analysis

In this section, the results from Method 2 with the machine operating at half speed and rated load are examined. First, the results using a bus capacitance of 4 mF, which was used in the Method 1 simulation and the Method 3 simulation, are presented. Then, the results using a bus capacitance of 400 mF are presented.

The time domain plots of the line-to-neutral voltages  $v_{An}$ ,  $v_{Bn}$ , and  $v_{Cn}$  for Method 2 with a bus capacitance of 4 mF as well as their corresponding harmonic spectra in per unit are shown in Figure 5.85 through Figure 5.90. It is clear from the time domain plots that the neutral point imbalance is so severe in this case that only the third harmonic component of the voltage is recognizable. The frequency plots also indicate the severe distortion of the line-to-neutral voltages. Clearly, this method is not feasible at lower output voltages unless the dc bus capacitance is increased.

The time domain plots of the line-to-line voltages  $v_{AB}$ ,  $v_{BC}$ , and  $v_{CA}$  for Method 2 with a bus capacitance of 4 mF as well as their corresponding harmonic spectra are shown in Figure 5.91 through Figure 5.96. From the time domain plots, part of the expected two-level operation waveform is visible, but the magnitude of the pulses is generally much lower than expected. Likewise, some pulses appear that are much larger than expected. The frequency plots also indicate this severe distortion of the line-to-line voltages. As stated previously, the quality of these waveforms indicate that this method would not be practical at this operating point unless the dc bus

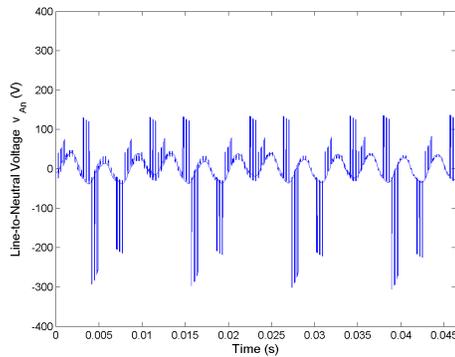


Figure 5.85: Line-to-neutral voltage  $v_{An}$  for Method 2 half rated speed, rated load.

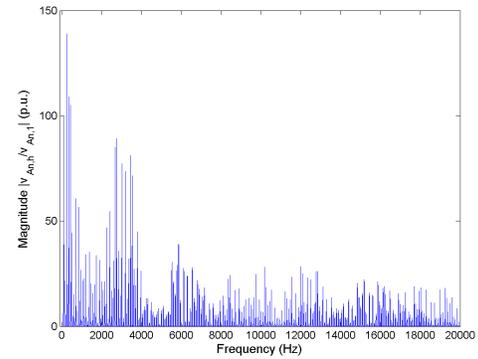


Figure 5.86: FFT of line-to-neutral voltage  $v_{An}$  for Method 2 half rated speed, rated load.

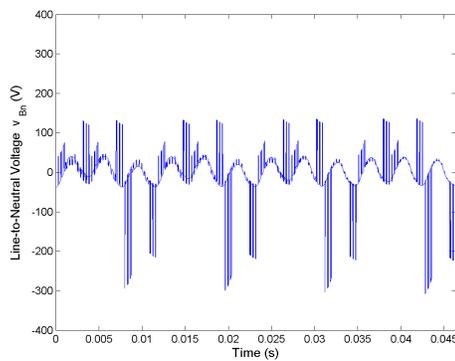


Figure 5.87: Line-to-neutral voltage  $v_{Bn}$  for Method 2 half rated speed, rated load.

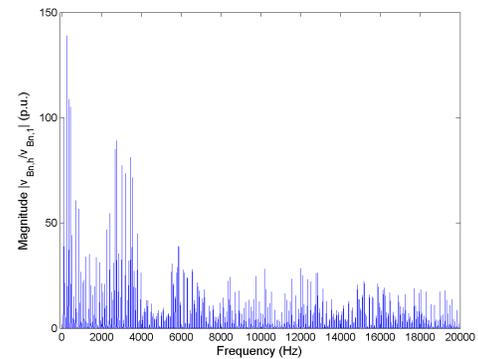


Figure 5.88: FFT of line-to-neutral voltage  $v_{Bn}$  for Method 2 half rated speed, rated load.

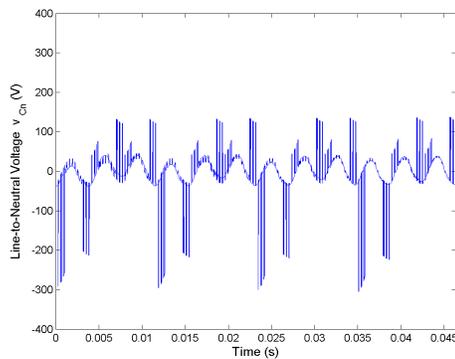


Figure 5.89: Line-to-neutral voltage  $v_{Cn}$  for Method 2 half rated speed, rated load.

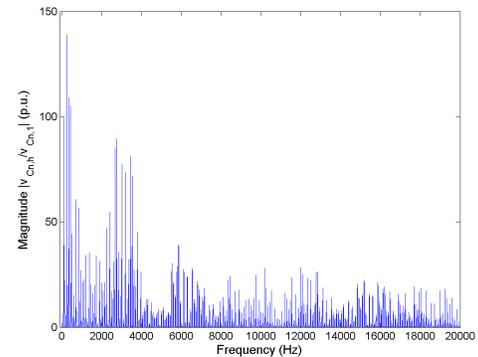


Figure 5.90: FFT of line-to-neutral voltage  $v_{Cn}$  for Method 2 half rated speed, rated load.

capacitance is increased.

The time domain plots of the phase currents  $i_A$ ,  $i_B$ , and  $i_C$  for Method 2 with a bus capacitance of 4 mF as well as their corresponding harmonic spectra are shown in Figure 5.97 through Figure 5.102. From the time domain plots, it is apparent that the phase currents are heavily distorted though some aspects of the fundamental sinusoid are still visible. This is confirmed in the frequency plots of the currents. The harmonic content of the currents is much larger than the harmonic content of the currents from Method 1, but these harmonics are still relatively small. The largest harmonic above the fundamental is the fourth harmonic, which is 8.45% of the fundamental.

The space vector plot of the line-to-neutral voltages for Method 2 with a bus capacitance of 4 mF is presented in Figure 5.103. This voltage space vector clearly demonstrates the severity of the neutral point imbalance. The small voltage vectors are badly distorted and have a magnitude significantly larger than the expected  $\frac{1}{3}V_{bus} = 120V$ . The calculated values of the 2-norm of the differences between the vertices and the corresponding voltage vectors are presented in Section 5.5.2.

The space vector plot of the phase currents and the time domain plot of the neutral point current for Method 2 with a bus capacitance of 4 mF are presented in Figure 5.104 and Figure 5.105. The trace of the current space vector is a highly distorted circle with severe deviations between  $30^\circ e.$  and  $60^\circ e.$ , between  $150^\circ e.$  and  $180^\circ e.$ , and between  $270^\circ e.$  and  $300^\circ e.$  Between these periods of severe distortion,

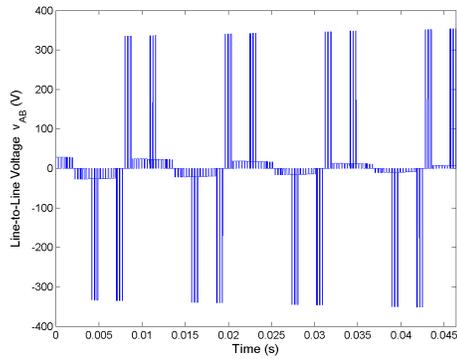


Figure 5.91: Line-to-line voltage  $v_{AB}$  for Method 2 half rated speed, rated load.

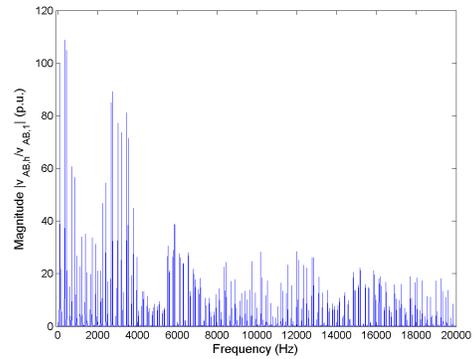


Figure 5.92: FFT of line-to-line voltage  $v_{AB}$  for Method 2 half rated speed, rated load.

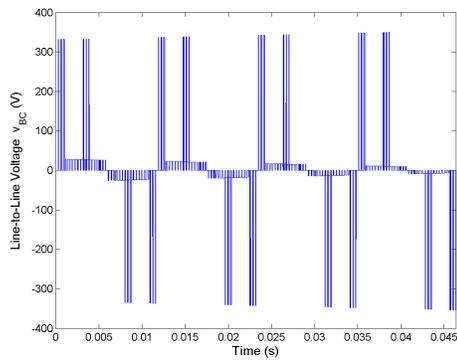


Figure 5.93: Line-to-line voltage  $v_{BC}$  for Method 2 half rated speed, rated load.

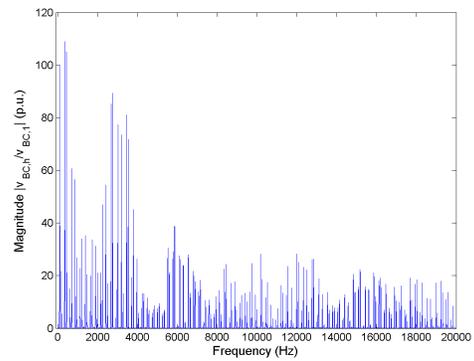


Figure 5.94: FFT of line-to-line voltage  $v_{BC}$  for Method 2 half rated speed, rated load.

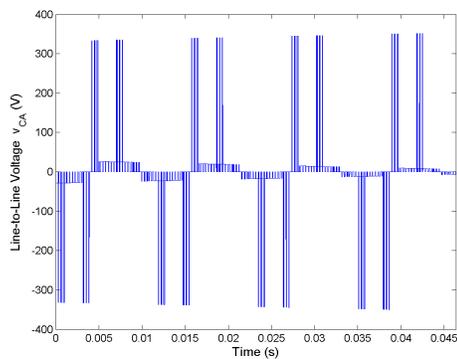


Figure 5.95: Line-to-line voltage  $v_{CA}$  for Method 2 half rated speed, rated load.

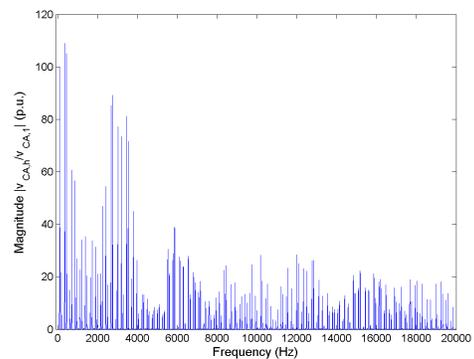


Figure 5.96: FFT of line-to-line voltage  $v_{CA}$  for Method 2 half rated speed, rated load.

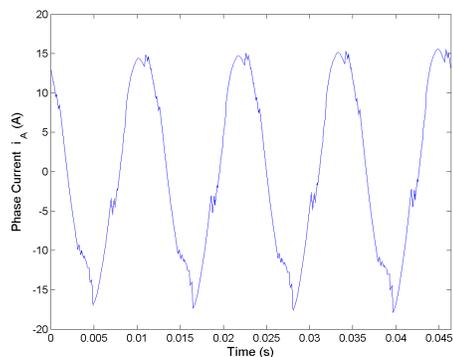


Figure 5.97: Phase current  $i_A$  for Method 2 half rated speed, rated load.

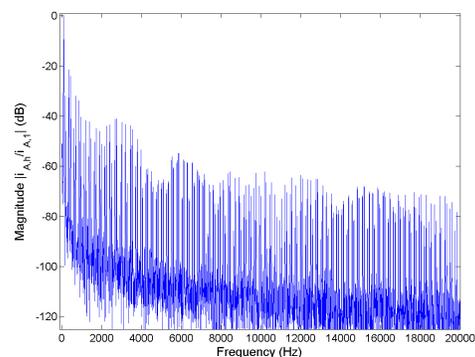


Figure 5.98: FFT of phase current  $i_A$  for Method 2 half rated speed, rated load.

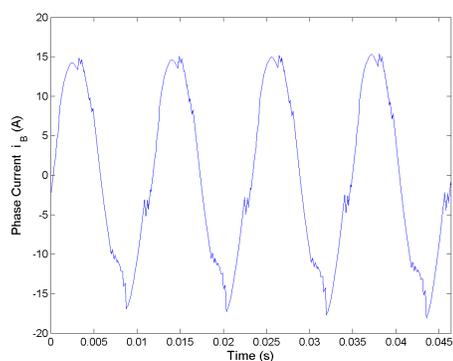


Figure 5.99: Phase current  $i_B$  for Method 2 half rated speed, rated load.

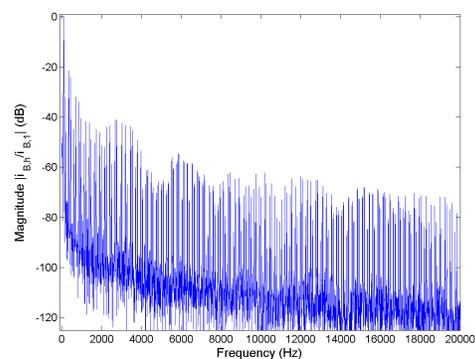


Figure 5.100: FFT of phase current  $i_B$  for Method 2 half rated speed, rated load.

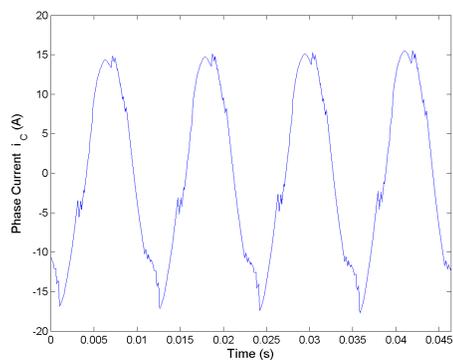


Figure 5.101: Phase current  $i_C$  for Method 2 half rated speed, rated load.

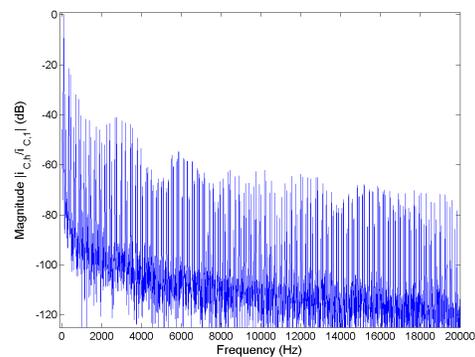


Figure 5.102: FFT of phase current  $i_C$  for Method 2 half rated speed, rated load.

the trajectory of the current space vector seems to follow an arc with a smoothly decreasing radius. Since the machine winding is highly inductive, this may be seen as the decay of the currents in an inductive circuit when the voltage source (in this case, the active voltage vector) is removed. Likewise, when the active voltage vectors are applied at  $60^\circ e.$ ,  $180^\circ e.$ , and  $300^\circ e.$ , the magnitude of the current space vector increases. In Figure 5.105, the neutral point current is plotted in the time domain. Similar to the neutral point current from the rated speed case, the negative portion of the waveform is more pronounced than the positive portion. Thus, the neutral point has a significant effect on the neutral point balance.

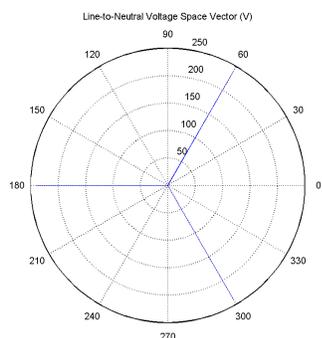


Figure 5.103: Space vector of line-to-neutral voltages for Method 2 half rated speed, rated load.

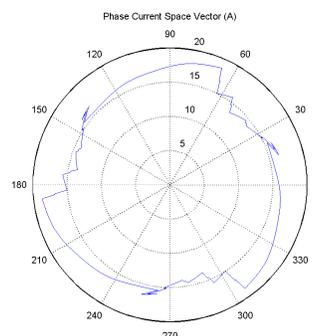


Figure 5.104: Space vector of phase currents for Method 2 half rated speed, rated load.

Again, it was shown that the switching pattern of Method 2 severely affected the balance of the neutral point of the dc bus. The simulation of the inverter with PWM Method 2 was repeated with an increased bus capacitance of 400 mF, and the

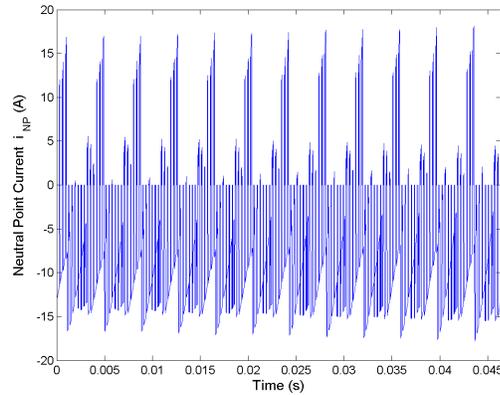


Figure 5.105: Neutral point current  $i_{NP}$  for Method 2 half rated speed, rated load.

results are provided in the remainder of this section.

The time domain plots of the line-to-neutral voltages  $v_{An}$ ,  $v_{Bn}$ , and  $v_{Cn}$  as well as their corresponding harmonic spectra in per unit are shown in Figure 5.106 through Figure 5.111. It is clear from the time domain plots that the line-to-neutral voltages are heavily distorted by the back emf of the machine. However, these results are similar to those of Method 1 operating at half speed, rated load. By examining the frequency plots, it can be seen that these line-to-neutral voltages have a significant third harmonic slightly less than 40% of the fundamental. The main portion of the harmonics caused by the switching of the IGBTs appear in the side bands of the sampling frequency  $f_s = 3105$  Hz. Overall, the increase in bus capacitance, though impractical, greatly improves the quality of the waveforms over half speed operation with lower bus capacitance.

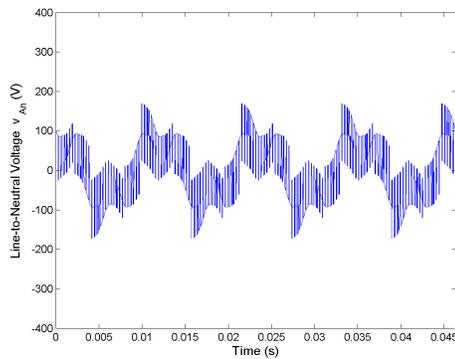


Figure 5.106: Line-to-neutral voltage  $v_{An}$  for Method 2 half rated speed, rated load and  $C_{bus} = 400mF$ .

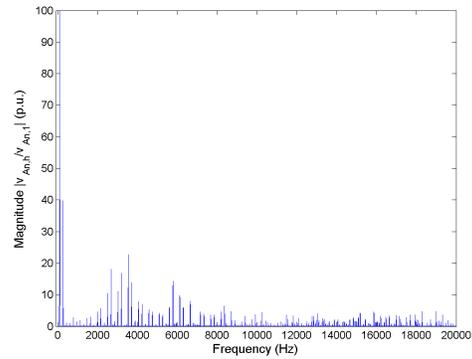


Figure 5.107: FFT of line-to-neutral voltage  $v_{An}$  for Method 2 half rated speed, rated load and  $C_{bus} = 400mF$ .

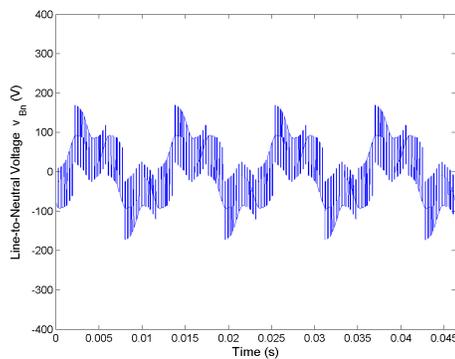


Figure 5.108: Line-to-neutral voltage  $v_{Bn}$  for Method 2 half rated speed, rated load and  $C_{bus} = 400mF$ .

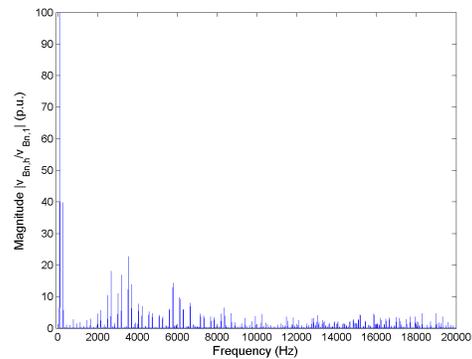


Figure 5.109: FFT of line-to-neutral voltage  $v_{Bn}$  for Method 2 half rated speed, rated load and  $C_{bus} = 400mF$ .

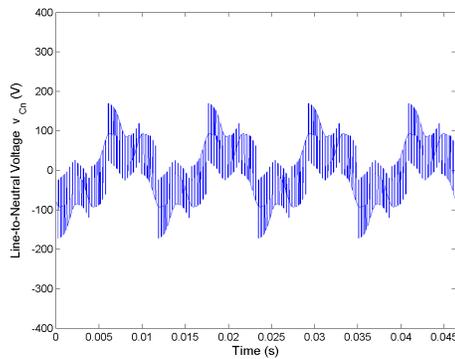


Figure 5.110: Line-to-neutral voltage  $v_{Cn}$  for Method 2 half rated speed, rated load and  $C_{bus} = 400mF$ .

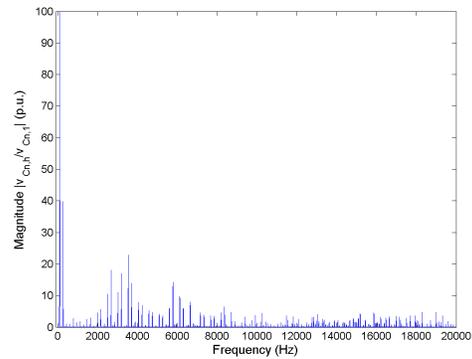


Figure 5.111: FFT of line-to-neutral voltage  $v_{Cn}$  for Method 2 half rated speed, rated load and  $C_{bus} = 400mF$ .

The time domain plots of the line-to-line voltages  $v_{AB}$ ,  $v_{BC}$ , and  $v_{CA}$  for Method 2 with a bus capacitance of 400 mF as well as their corresponding harmonic spectra are shown in Figure 5.112 through Figure 5.117. From the time domain plots, it is clear that the inverter is operating in two-level mode as expected for the half rated speed case. By examining the frequency plots, it is seen that the harmonic content is spread throughout the entire spectrum, though the largest harmonics appear in the side bands of the sampling frequency.

The time domain plots of the phase currents  $i_A$ ,  $i_B$ , and  $i_C$  and their corresponding harmonic spectra for Method 2 with a bus capacitance of 400 mF are shown in Figure 5.118 through Figure 5.123. From the time domain plots, the currents appear to be nearly sinusoidal, though a small ripple is seen in the current that is caused by the switching of the IGBTs. This is confirmed in the frequency plots of the currents. Much of the harmonic content is located in the side bands of the first harmonic of the sampling frequency. However, a relatively significant fifth harmonic (1.40% of the fundamental), seventh harmonic (0.43% of the fundamental), and eleventh harmonic (0.60% of the fundamental) also exist. It is clear that the increase in the bus capacitance greatly improved the output quality of the phase currents, though the result does not show improvement over Method 1.

The space vector plot of the line-to-neutral voltages for Method 2 with a bus capacitance of 400 mF is presented in Figure 5.124. As expected, the plot of the

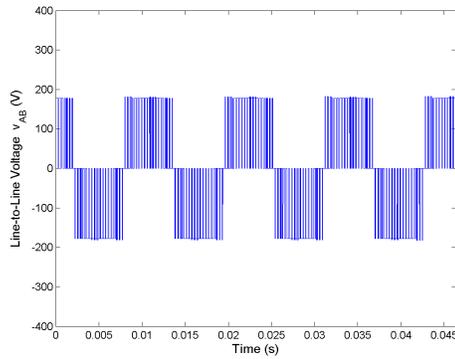


Figure 5.112: Line-to-line voltage  $v_{AB}$  for Method 2 half rated speed, rated load and  $C_{bus} = 400mF$ .

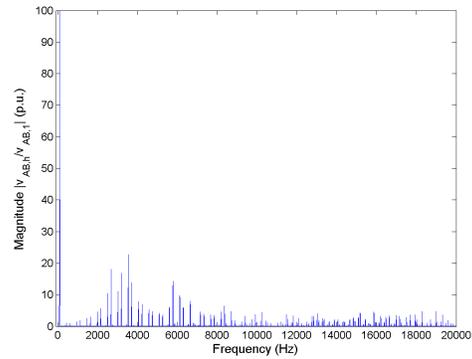


Figure 5.113: FFT of line-to-line voltage  $v_{AB}$  for Method 2 half rated speed, rated load and  $C_{bus} = 400mF$ .

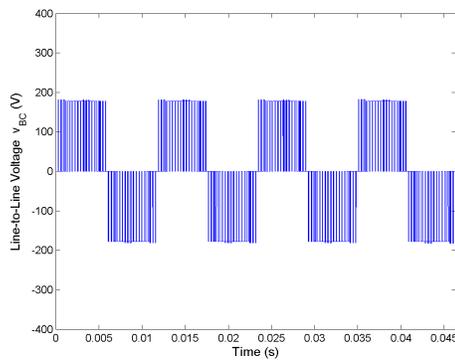


Figure 5.114: Line-to-line voltage  $v_{BC}$  for Method 2 half rated speed, rated load and  $C_{bus} = 400mF$ .

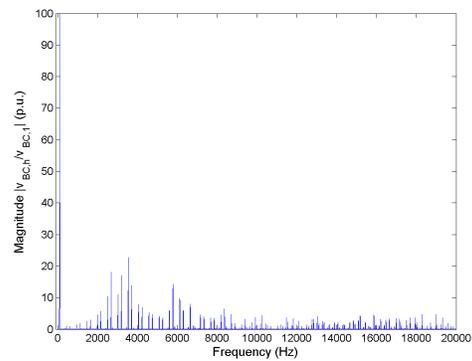


Figure 5.115: FFT of line-to-line voltage  $v_{BC}$  for Method 2 half rated speed, rated load and  $C_{bus} = 400mF$ .

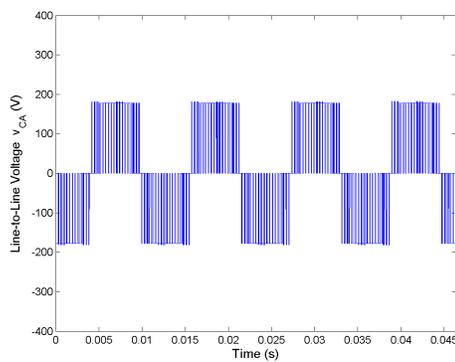


Figure 5.116: Line-to-line voltage  $v_{CA}$  for Method 2 half rated speed, rated load and  $C_{bus} = 400mF$ .

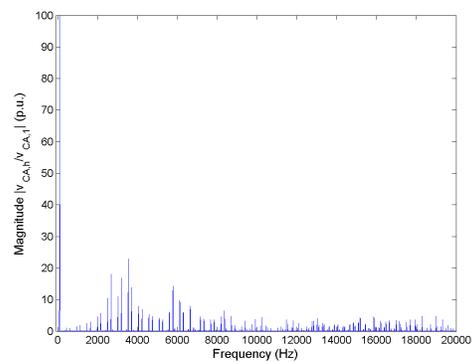


Figure 5.117: FFT of line-to-line voltage  $v_{CA}$  for Method 2 half rated speed, rated load and  $C_{bus} = 400mF$ .

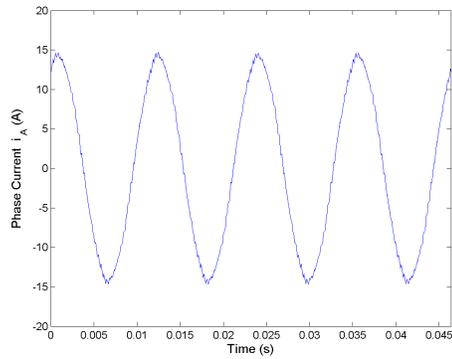


Figure 5.118: Phase current  $i_A$  for Method 2 half rated speed, rated load and  $C_{bus} = 400mF$ .

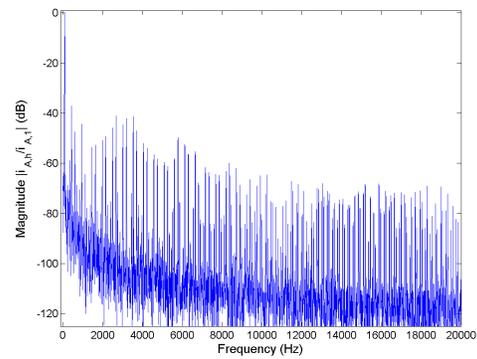


Figure 5.119: FFT of phase current  $i_A$  for Method 2 half rated speed, rated load and  $C_{bus} = 400mF$ .

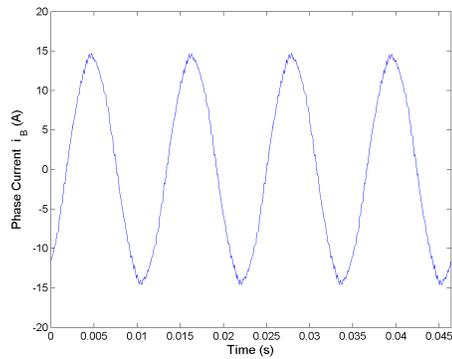


Figure 5.120: Phase current  $i_B$  for Method 2 half rated speed, rated load and  $C_{bus} = 400mF$ .

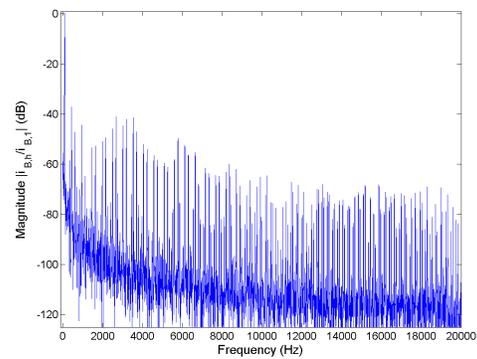


Figure 5.121: FFT of phase current  $i_B$  for Method 2 half rated speed, rated load and  $C_{bus} = 400mF$ .

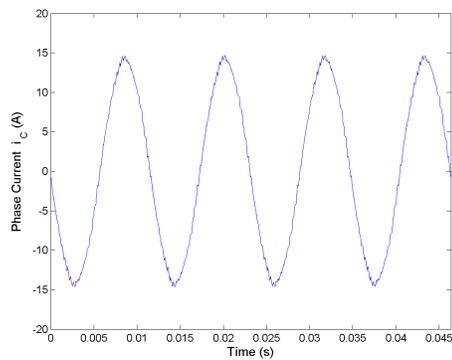


Figure 5.122: Phase current  $i_C$  for Method 2 half rated speed, rated load and  $C_{bus} = 400mF$ .

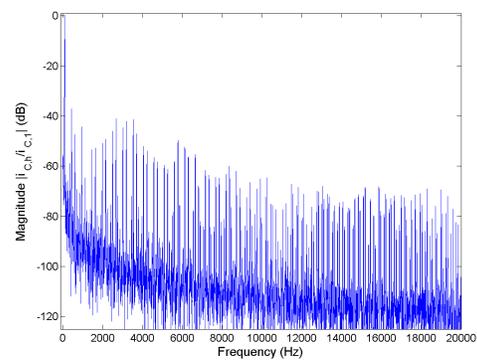


Figure 5.123: FFT of phase current  $i_C$  for Method 2 half rated speed, rated load and  $C_{bus} = 400mF$ .

space vector is similar to the hexagon that is normally associated with a two-level inverter. From this space vector plot, it becomes apparent that only zero vectors and small vectors are used at this operating point. The vertices of the triangles appear to align fairly well with the locations of the small vectors, which indicates the imbalance in the neutral point of the dc bus is not significant. The calculated values of the 2-norm of the differences between the vertices and the corresponding voltage vectors are presented in Section 5.5.2.

The space vector plot of the phase currents and the time domain plot of the neutral point current for Method 2 with a bus capacitance of 400 mF are presented in Figure 5.125 and Figure 5.126. The current space vector is nearly circular but has six slightly flattened sides as in the case of full speed operation. However, the flattening of the trajectory is not as severe as in some of the previous results. The slightly jagged deviations in the trajectory are due to the sampling frequency of the PWM method and seem to be slightly larger than those of the current trajectory from Method 1. In Figure 5.126, the neutral point current is plotted in the time domain. At this operating speed, the negative half of the time domain signal is significantly more prominent than the positive half. Again, this is an indication that this method inherently affects the balance of the dc bus neutral point more than the switching pattern of Method 1.

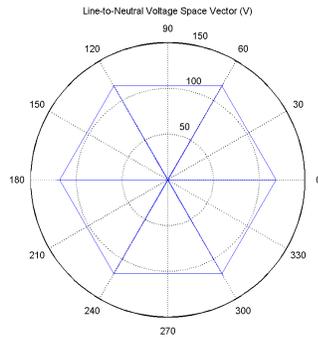


Figure 5.124: Space vector of line-to-neutral voltages for Method 2 half rated speed, rated load and  $C_{bus} = 400mF$ .

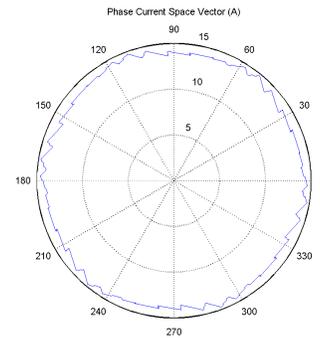


Figure 5.125: Space vector of phase currents for Method 2 half rated speed, rated load and  $C_{bus} = 400mF$ .

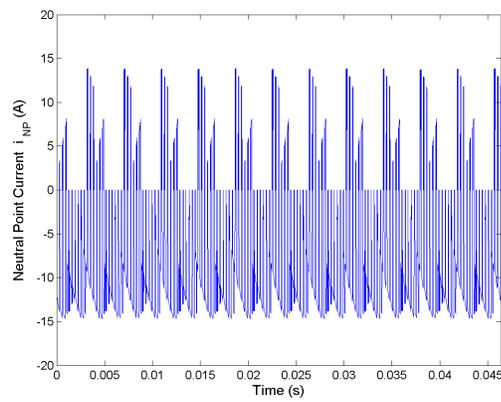


Figure 5.126: Neutral point current  $i_{NP}$  for Method 2 half rated speed, rated load and  $C_{bus} = 400mF$ .

## 5.4 Results and Analysis for Method 3

### 5.4.1 Rated Speed, Rated Load Results and Analysis

In this section, the results from Method 3 with the machine operating at rated speed and rated load are examined. Only a bus capacitance of 4 mF is considered for this switching pattern because the imbalance in the neutral point voltage is not severe in this case.

The time domain plots of the line-to-neutral voltages  $v_{An}$ ,  $v_{Bn}$ , and  $v_{Cn}$  as well as their corresponding harmonic spectra in per unit are shown in Figure 5.127 through Figure 5.132. As with the two previous PWM methods, it is clear from the time domain plots that the line-to-neutral voltages are heavily distorted by the back emf of the machine. By examining the frequency plots, it can be seen that this distortion is caused by a significant third harmonic, which is about 40% of the fundamental. A smaller ninth harmonic also exists, but with a magnitude of about 2.9% of the fundamental, its effect is relatively small. The remainder of the harmonic content is visible in the side bands around harmonics of the sampling frequency  $f_s = 6210$  Hz. Overall, these results are very similar to the line-to-neutral voltages of Method 1.

The time domain plots of the line-to-line voltages  $v_{AB}$ ,  $v_{BC}$ , and  $v_{CA}$  as well as their corresponding harmonic spectra are shown in Figure 5.133 through Figure 5.138. As opposed to the line-to-neutral voltages, the line-to-line voltages have the

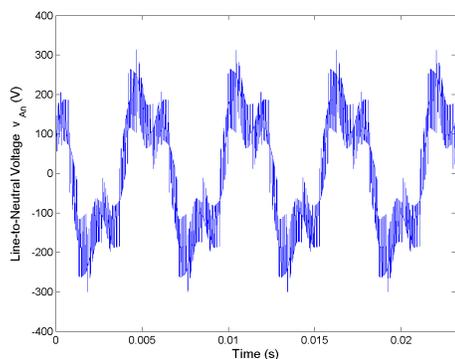


Figure 5.127: Line-to-neutral voltage  $v_{An}$  for Method 3 rated speed, rated load.

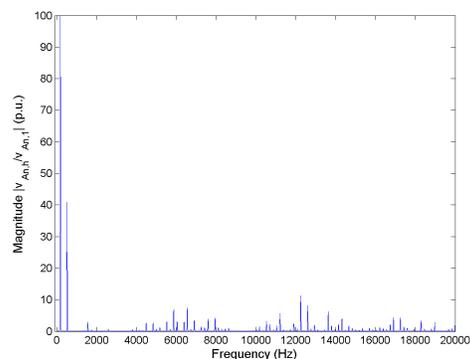


Figure 5.128: FFT of line-to-neutral voltage  $v_{An}$  for Method 3 rated speed, rated load.

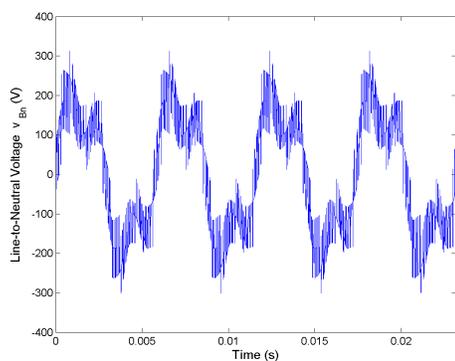


Figure 5.129: Line-to-neutral voltage  $v_{Bn}$  for Method 3 rated speed, rated load.

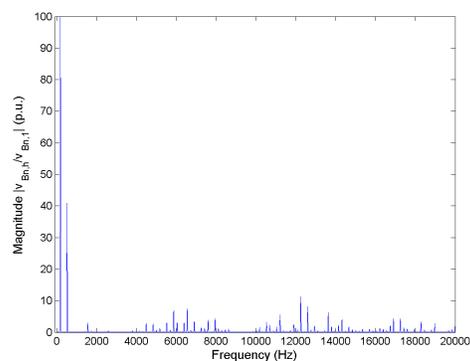


Figure 5.130: FFT of line-to-neutral voltage  $v_{Bn}$  for Method 3 rated speed, rated load.

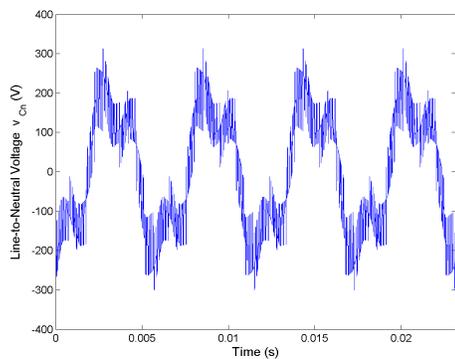


Figure 5.131: Line-to-neutral voltage  $v_{Cn}$  for Method 3 rated speed, rated load.

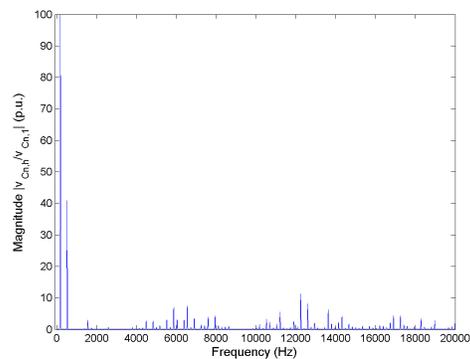


Figure 5.132: FFT of line-to-neutral voltage  $v_{Cn}$  for Method 3 rated speed, rated load.

typical three-level output voltage shape. When inspecting the frequency plots, it can be seen that the third harmonic components and the ninth harmonic components from the line-to-neutral voltages were eliminated from the line-to-line voltages as expected. The remainder of the harmonic content is found in the side bands of the harmonics of the sampling frequency. Again, these results are very similar to the line-to-line voltages produced by Method 1.

The time domain plots of the phase currents  $i_A$ ,  $i_B$ , and  $i_C$  as well as their corresponding harmonic spectra are shown in Figure 5.139 through Figure 5.144. From the time domain plots, the currents appear to be nearly sinusoidal. This is again confirmed in the frequency plots of the currents. The majority of the harmonic content is located in the side bands of the harmonics of the sampling frequency. However, a relatively significant fifth harmonic (1.73% of the fundamental), seventh harmonic (0.35% of the fundamental), and eleventh harmonic (0.55% of the fundamental) also exist. Again, the phase currents produced by Method 3 under rated speed, rated load are very similar to the phase currents produced by Method 1.

The space vector plot of the line-to-neutral voltages is presented in Figure 5.145. For this PWM method, the voltage space vector appears hexagonal with equilateral triangles lining the edges, which is very similar to the voltage space vector plot from Method 1. The main difference between the two plots is the slightly larger number of transitions between voltage vectors in Method 3. This difference is not

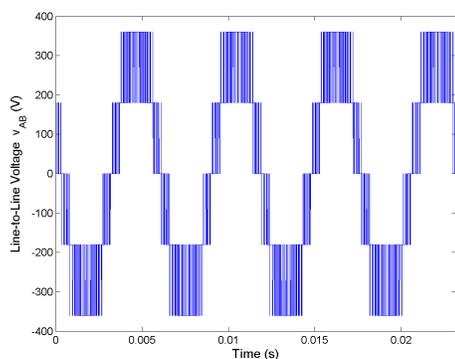


Figure 5.133: Line-to-line voltage  $v_{AB}$  for Method 3 rated speed, rated load.

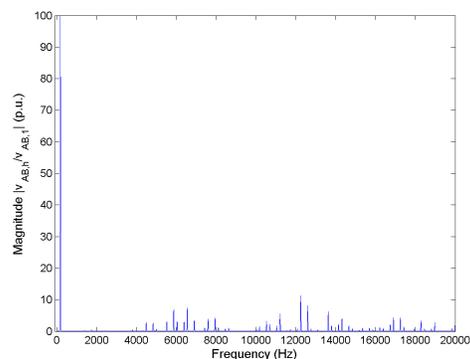


Figure 5.134: FFT of line-to-line voltage  $v_{AB}$  for Method 3 rated speed, rated load.

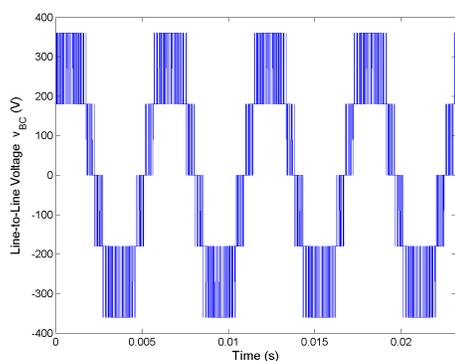


Figure 5.135: Line-to-line voltage  $v_{BC}$  for Method 3 rated speed, rated load.

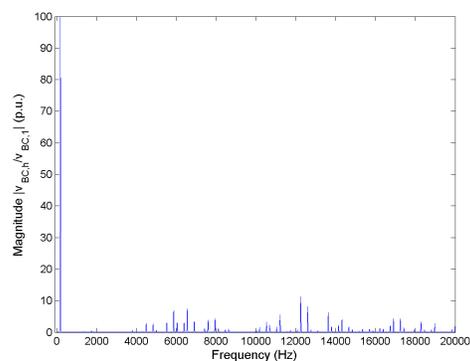


Figure 5.136: FFT of line-to-line voltage  $v_{BC}$  for Method 3 rated speed, rated load.

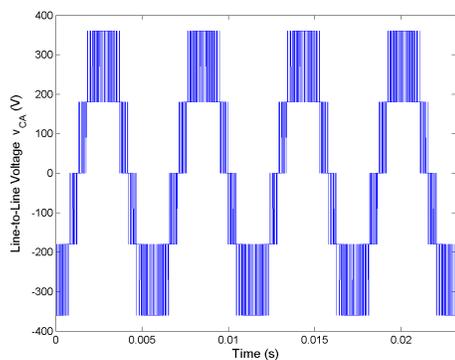


Figure 5.137: Line-to-line voltage  $v_{CA}$  for Method 3 rated speed, rated load.

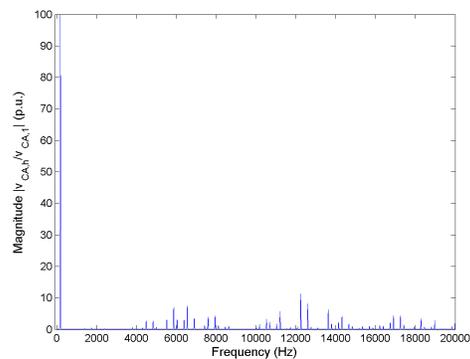


Figure 5.138: FFT of line-to-line voltage  $v_{CA}$  for Method 3 rated speed, rated load.

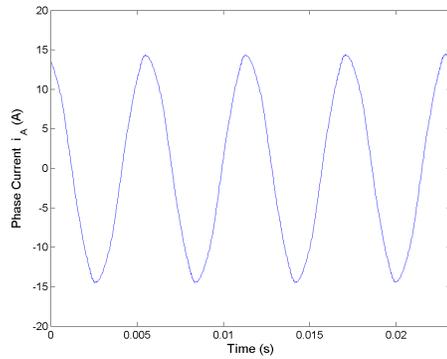


Figure 5.139: Phase current  $i_A$  for Method 3 rated speed, rated load.

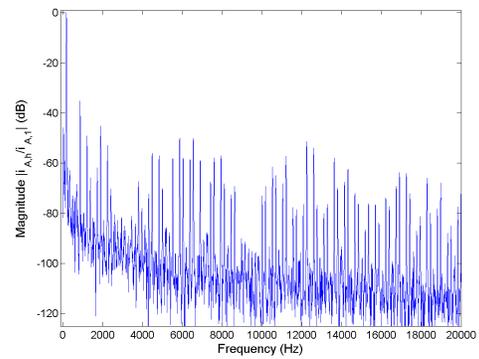


Figure 5.140: FFT of phase current  $i_A$  for Method 3 rated speed, rated load.

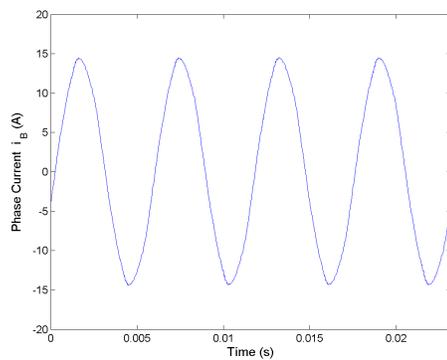


Figure 5.141: Phase current  $i_B$  for Method 3 rated speed, rated load.

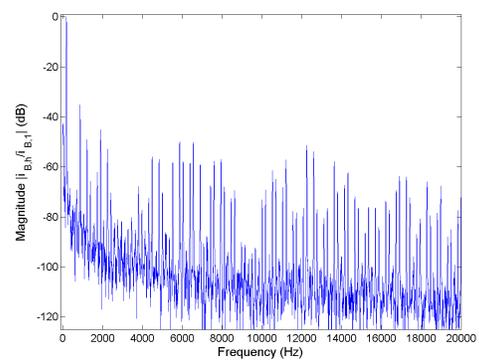


Figure 5.142: FFT of phase current  $i_B$  for Method 3 rated speed, rated load.

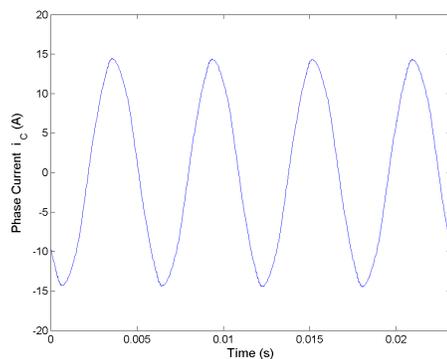


Figure 5.143: Phase current  $i_C$  for Method 3 rated speed, rated load.

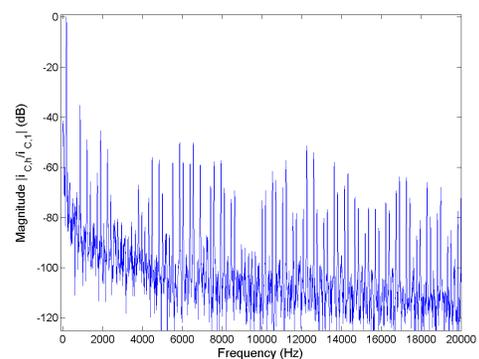


Figure 5.144: FFT of phase current  $i_C$  for Method 3 rated speed, rated load.

easily seen without plotting the voltage space vector as it changes over time. Based on visual inspection, the vertices of the triangles appear to align fairly well with the voltage vectors, implying that the imbalance in the neutral point of the dc bus is small. The calculated values of the 2-norm of the differences between the vertices and the corresponding voltage vectors are presented in Section 5.5.1.

The space vector plot of the phase currents and the time domain plot of the neutral point current are presented in Figure 5.146 and Figure 5.147. The current space vector is almost circular, but it has six flattened sides similar to those of the current space vector produced by Method 1 operating under rated speed and rated load. In Figure 5.147, the neutral point current is plotted in the time domain. Similar to the neutral point current generated by Method 1 operating under rated speed and rated load, the neutral point current is split fairly evenly between the positive half of the cycle and the negative half of the cycle. This is because in this method, both the positive small vectors and the negative small vectors are applied.

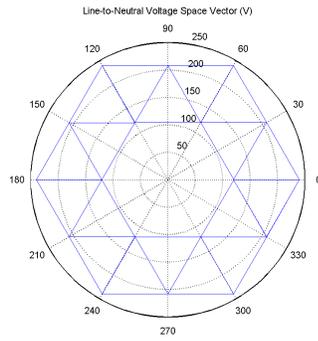


Figure 5.145: Space vector of line-to-neutral voltages for Method 3 rated speed, rated load.

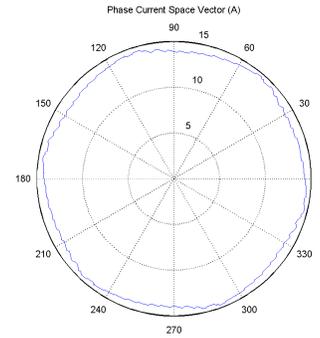


Figure 5.146: Space vector of phase currents for Method 3 rated speed, rated load.

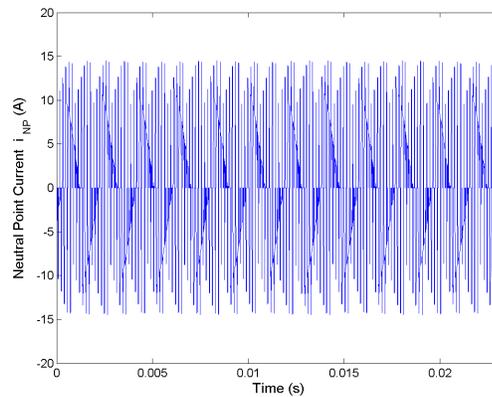


Figure 5.147: Neutral point current  $i_{NP}$  for Method 3 rated speed, rated load.

### 5.4.2 Half Rated Speed, Rated Load Results and Analysis

In this section, the results from Method 3 with the machine operating at half speed and rated load are examined. The time domain plots of the line-to-neutral voltages  $v_{An}$ ,  $v_{Bn}$ , and  $v_{Cn}$  as well as their corresponding harmonic spectra in per unit are shown in Figure 5.148 through Figure 5.153. It is clear from the time domain plots that the line-to-neutral voltages are distorted by the back emf of the machine. It is also clear that the switching frequency of the output has increased although the sampling frequency remained at  $f_s = 3105$  Hz. This is due to the increase in the number of switching state transitions within each sampling period for lower output voltage magnitudes. By examining the frequency plots, it can be seen that these line-to-neutral voltages have a significant third harmonic slightly less than 40% of the fundamental and a smaller ninth harmonic just as in the rated speed case. The remainder of the harmonic content is visible in the side bands around the harmonics of the sampling frequency.

The time domain plots of the line-to-line voltages  $v_{AB}$ ,  $v_{BC}$ , and  $v_{CA}$  as well as their corresponding harmonic spectra are shown in Figure 5.154 through Figure 5.159. From the time domain plots, it is clear that the inverter is operating in two-level mode for the half speed case as expected. As in the line-to-neutral voltages, the switching frequency of the line-to-line voltages has increased compared to the line-to-line voltages when operating at rated speed. From the frequency plots, the large third harmonic

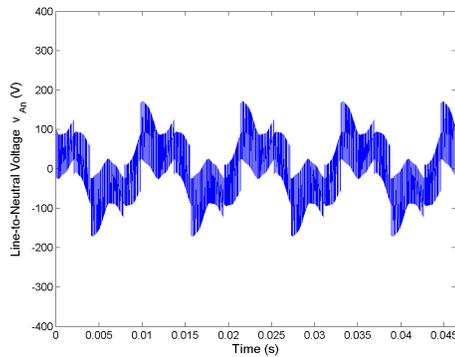


Figure 5.148: Line-to-neutral voltage  $v_{An}$  for Method 3 half rated speed, rated load.

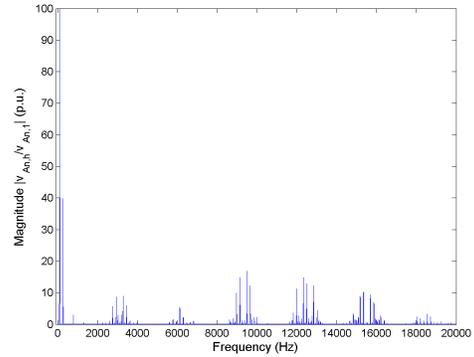


Figure 5.149: FFT of line-to-neutral voltage  $v_{An}$  for Method 3 half rated speed, rated load.

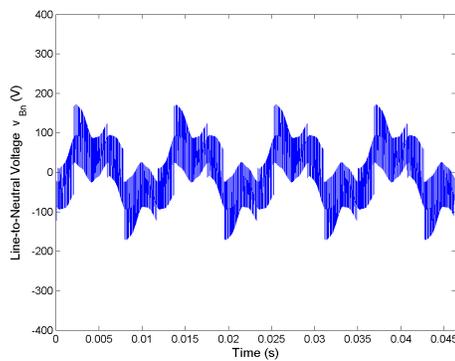


Figure 5.150: Line-to-neutral voltage  $v_{Bn}$  for Method 3 half rated speed, rated load.

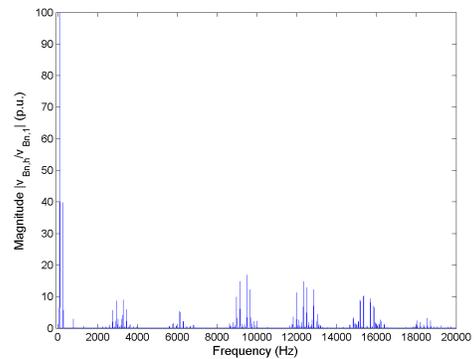


Figure 5.151: FFT of line-to-neutral voltage  $v_{Bn}$  for Method 3 half rated speed, rated load.

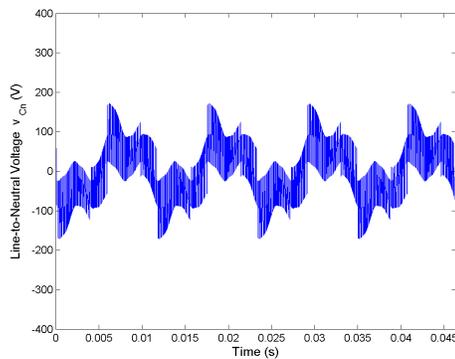


Figure 5.152: Line-to-neutral voltage  $v_{Cn}$  for Method 3 half rated speed, rated load.

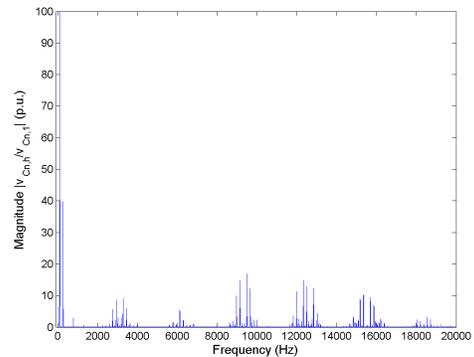


Figure 5.153: FFT of line-to-neutral voltage  $v_{Cn}$  for Method 3 half rated speed, rated load.

components and the ninth harmonic components from the line-to-neutral voltages were eliminated from the line-to-line voltages. The remainder of the harmonic content is present in the side bands of the harmonics of the sampling frequency, particularly  $(3f_s)$ ,  $(4f_s)$ , and  $(5f_s)$ .

The time domain plots of the phase currents  $i_A$ ,  $i_B$ , and  $i_C$  as well as their corresponding harmonic spectra are shown in Figure 5.160 through Figure 5.165. From the time domain plots, the currents appear to be nearly sinusoidal. This is confirmed in the frequency plots of the currents. Much of the harmonic content is located in the side bands of the harmonics of the sampling frequency, though more side bands appear in this case than in the phase currents of Method 1 operating at half speed, rated load. As in the other methods, a relatively significant fifth harmonic (1.71% of the fundamental), seventh harmonic (0.34% of the fundamental), and eleventh harmonic (0.53% of the fundamental) also exist.

The space vector plot of the line-to-neutral voltages is presented in Figure 5.166. As was the case with the previous two methods operating correctly at half speed, rated load, the voltage space vector has the appearance of the hexagon that is normally associated with a two-level inverter. Once again, the primary difference between this space vector plot and those of the previous methods is in the number of switching state transitions within each sampling period. Based on visual inspection, the vertices of the triangles appear to align fairly well with the locations of the small

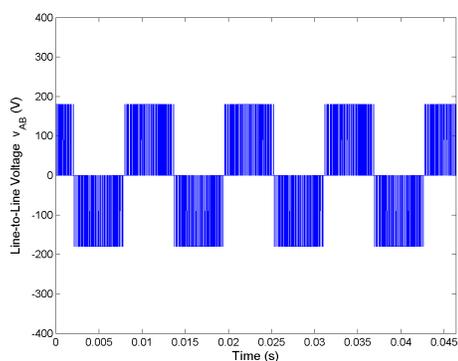


Figure 5.154: Line-to-line voltage  $v_{AB}$  for Method 3 half rated speed, rated load.

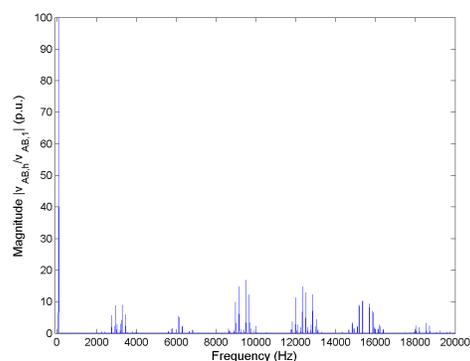


Figure 5.155: FFT of line-to-line voltage  $v_{AB}$  for Method 3 half rated speed, rated load.

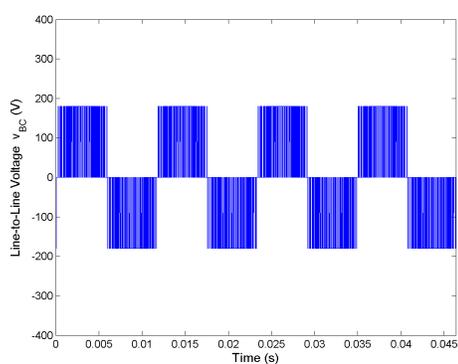


Figure 5.156: Line-to-line voltage  $v_{BC}$  for Method 3 half rated speed, rated load.

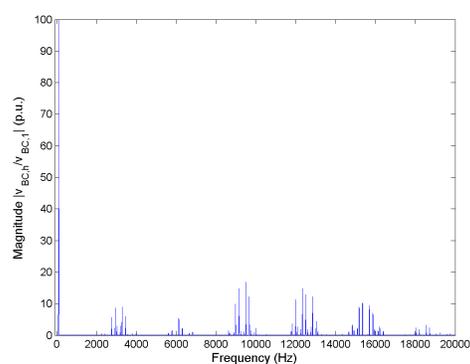


Figure 5.157: FFT of line-to-line voltage  $v_{BC}$  for Method 3 half rated speed, rated load.

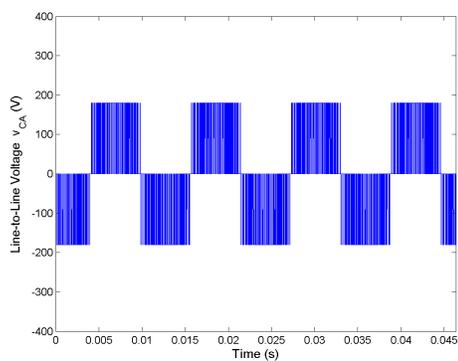


Figure 5.158: Line-to-line voltage  $v_{CA}$  for Method 3 half rated speed, rated load.

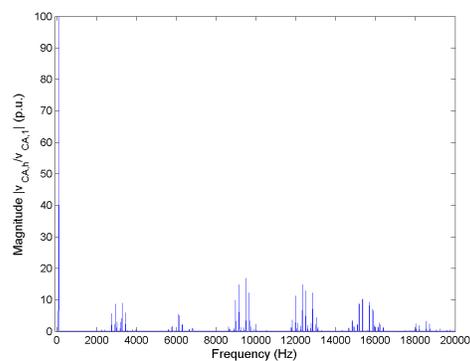


Figure 5.159: FFT of line-to-line voltage  $v_{CA}$  for Method 3 half rated speed, rated load.

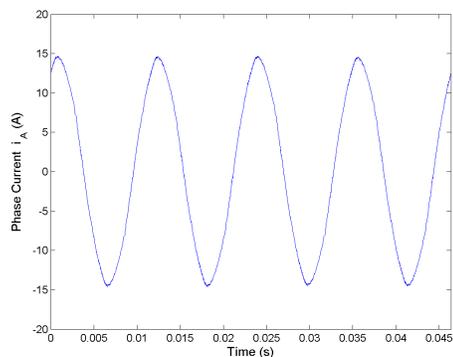


Figure 5.160: Phase current  $i_A$  for Method 3 half rated speed, rated load.

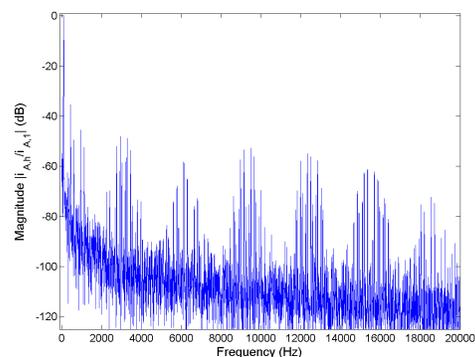


Figure 5.161: FFT of phase current  $i_A$  for Method 3 half rated speed, rated load.

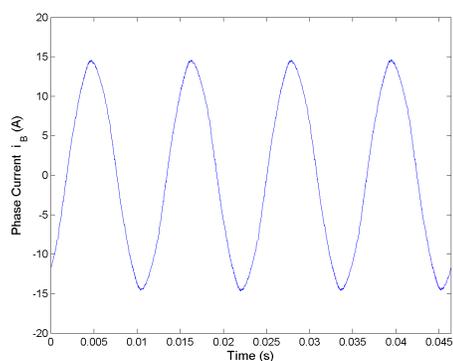


Figure 5.162: Phase current  $i_B$  for Method 3 half rated speed, rated load.

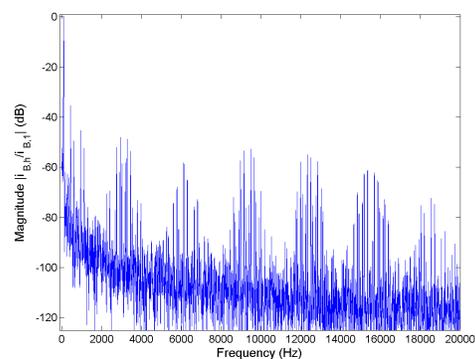


Figure 5.163: FFT of phase current  $i_B$  for Method 3 half rated speed, rated load.

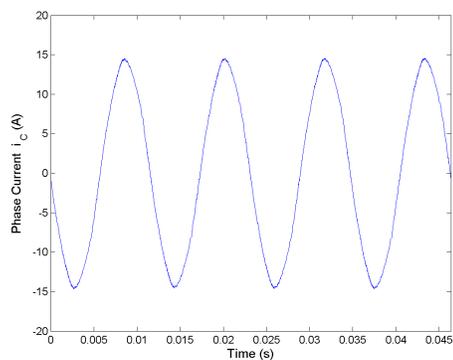


Figure 5.164: Phase current  $i_C$  for Method 3 half rated speed, rated load.

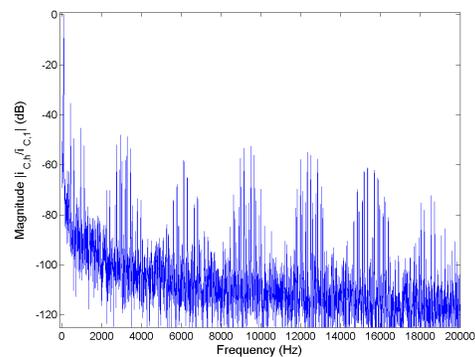


Figure 5.165: FFT of phase current  $i_C$  for Method 3 half rated speed, rated load.

vectors, indicating that neutral point imbalance is not significant. The calculated values of the 2-norm of the differences between the vertices and the corresponding voltage vectors are presented in Section 5.5.2.

The space vector plot of the phase currents and the time domain plot of the neutral point current are presented in Figure 5.167 and Figure 5.168. The current space vector is mostly circular, but it has six flattened sides as in the case of rated speed operation. The jagged deviations from the trajectory that are due to the switching of the IGBTs seem to be smaller in this case than in previous cases. This is due to the higher switching frequency of the IGBTs. In Figure 5.168, the neutral point current is plotted in the time domain. The neutral point current seems to be split fairly evenly between the positive half of the cycle and the negative half of the cycle, indicating its effect on the neutral point balance is relatively small. The switching frequency seen in the neutral point current also increased in this case.

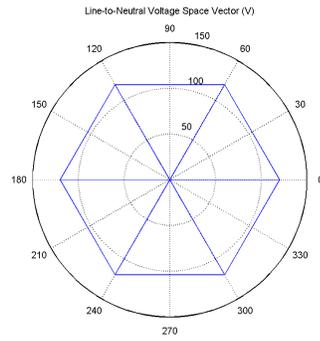


Figure 5.166: Space vector of line-to-neutral voltages for Method 3 half rated speed, rated load.

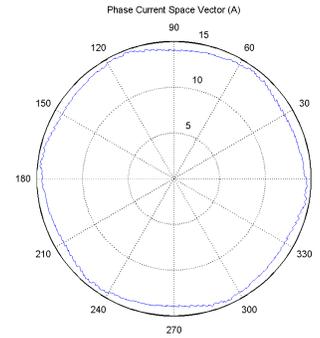


Figure 5.167: Space vector of phase currents for Method 3 half rated speed, rated load.

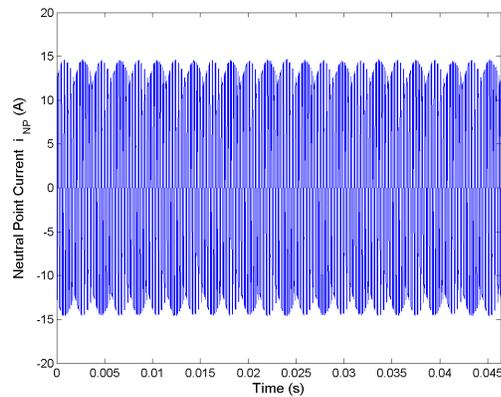


Figure 5.168: Neutral point current  $i_{NP}$  for Method 3 half rated speed, rated load.

## 5.5 Comparison of the Three Methods

### 5.5.1 Operation at Rated Speed, Rated Load

In this section, the three space vector PWM methods are compared when each is operating at rated speed and rated load. This comparison is based on the change in the small and medium voltage vectors during operation, the neutral point rms and mean values, and the total harmonic distortion of the line-to-neutral voltages, the line-to-line voltages, and the phase currents.

The total harmonic distortion of each of the line-to-neutral voltages for space vector PWM Method 1, Method 2, Method 3, and Method 2 with increased bus capacitance is presented in Table 5.1. The line-to-neutral voltage THD is nearly identical for both Method 1 and Method 3. The line-to-neutral voltage THD for Method 2 is significantly higher for the base case of  $C_{bus} = 4$  mF and slightly higher for the second case of  $C_{bus} = 400$  mF.

Rated Speed	Method 1	Method 2	Method 3	Method 2 ( $C_{bus}$ of 400mF)
$v_{An}$ THD	50.89%	57.97%	50.89%	51.00%
$v_{Bn}$ THD	50.90%	57.94%	50.90%	51.00%
$v_{Cn}$ THD	50.90%	57.96%	50.90%	51.00%
Average THD	50.90%	57.96%	50.90%	51.00%

Table 5.1: Summary of line-to-neutral voltage THD for all three methods at rated speed, rated load.

The total harmonic distortion of each of the line-to-line voltages for space

vector PWM Method 1, Method 2, Method 3, and Method 2 with increased bus capacitance is presented in Table 5.2. The line-to-line voltage THD is nearly identical for both Method 1 and Method 3. The line-to-line voltage THD for Method 2 is significantly higher for the base case of  $C_{bus} = 4$  mF and approximately the same for the second case of  $C_{bus} = 400$  mF.

Rated Speed	Method 1	Method 2	Method 3	Method 2 ( $C_{bus}$ of 400mF)
$v_{AB}$ THD	29.62%	40.30%	29.62%	29.82%
$v_{BC}$ THD	29.64%	40.34%	29.64%	29.84%
$v_{CA}$ THD	29.60%	40.33%	29.60%	29.84%
Average THD	29.62%	40.32%	29.62%	29.83%

Table 5.2: Summary of line-to-line voltage THD for all three methods at rated speed, rated load.

The total harmonic distortion of each of the phase currents for space vector PWM Method 1, Method 2, Method 3, and Method 2 with increased bus capacitance is presented in Table 5.3. The phase current THD is nearly identical for both Method 1 and Method 3. The phase current THD for Method 2 is approximately four and a half times higher for the base case of  $C_{bus} = 4$  mF, though it is nearly the same compared to Method 1 and Method 3 for the second case of  $C_{bus} = 400$  mF. The mean neutral point current is also very close to zero in both Method 1 and Method 3, indicating a small net current flowing through the bus neutral. Since there is little net current through the neutral point of the dc bus, the bus capacitors are not significantly charged or discharged. This indicates that both of these switching patterns have little

effect on the neutral point voltage balance. The sign of the mean neutral point current simply indicates the direction of net current flow through the neutral point, which indicates which of the bus capacitors is charging and which is discharging. In the case of Method 2, the absolute value of the mean neutral point current is much larger. Thus, the net neutral point current is larger, and the bus capacitors become overly charged or discharged, creating an imbalance in the neutral point voltage.

Rated Speed	Method 1	Method 2	Method 3	Method 2 ( $C_{bus}$ of 400mF)
$i_A$ THD	1.67%	7.76%	1.67%	1.72%
$i_B$ THD	1.68%	7.68%	1.68%	1.73%
$i_C$ THD	1.68%	7.67%	1.68%	1.72%
Average THD	1.68%	7.71%	1.68%	1.72%
$I_{NP,rms}$ ( $A_{rms}$ )	7.248	6.883	7.248	7.235
$mean(i_{NP})$ (A)	$-6.710E - 3$	-2.414	$-6.712E - 3$	-2.426

Table 5.3: Summary of phase current THD and RMS value of neutral point current for all three methods at rated speed, rated load.

The values of the 2-norm of the change in the small and medium voltage vectors during operation of the inverter for space vector PWM Method 1, Method 2, Method 3, and Method 2 with increased bus capacitance are presented in Table 5.4. In most cases, Method 1 and Method 3 both have relatively little drift in the small voltage vectors and the medium voltage vectors. For Method 2, in the base case of  $C_{bus} = 4$  mF, the deviation of the small and medium vectors from their correct values is very large, thus indicating significant neutral point voltage imbalance. When the bus capacitance is increased to  $C_{bus} = 400$  mF, however, the deviation of the small

and medium vectors is greatly reduced. The drift in the small vectors tends to be slightly smaller than the drift in the medium vectors for Method 1 and Method 3 since the small vectors are always applied in redundant pairs in these two switching patterns. In contrast, the drift is relatively constant between the small and medium vectors in Method 2 because only one of the redundant small vectors is applied within a sampling period.

Rated Speed	Method 1	Method 2	Method 3	Method 2 ( $C_{bus}$ of 400mF)
sm. vector 1 deviation (V)	0.0081	50.41	0.0081	0.5559
sm. vector 2 deviation (V)	0.0320	50.01	0.0319	0.5558
sm. vector 3 deviation (V)	0.0078	50.02	0.0078	0.5519
sm. vector 4 deviation (V)	0.0329	50.17	0.0328	0.5530
sm. vector 5 deviation (V)	0.0076	50.22	0.0077	0.5536
sm. vector 6 deviation (V)	0.0314	50.36	0.0314	0.5551
med. vector 1 deviation (V)	0.1105	49.96	0.1103	0.5086
med. vector 2 deviation (V)	0.0997	49.96	0.0996	0.4851
med. vector 3 deviation (V)	0.1099	50.03	0.1097	0.5106
med. vector 4 deviation (V)	0.1005	50.15	0.1005	0.4872
med. vector 5 deviation (V)	0.1119	50.22	0.1118	0.5121
med. vector 6 deviation (V)	0.1004	50.34	0.1002	0.4892

Table 5.4: Summary of the 2-norm of the drift of the voltage vectors for all three methods at rated speed, rated load.

Overall, both Method 1 and Method 3 seem to produce similar results when operating at rated speed and rated load. This is because when operating at rated speed and rated load, the reference vector rotating in the  $(\alpha - \beta)$  plane is near its maximum value. In this case, the reference vector only briefly passes through the middle ring of triangles and does not pass through the inner ring of triangles described

previously in the development of Method 3. Thus, for the majority of the fundamental cycle, the switching pattern for Method 3 is identical to that of Method 1.

Method 2 did not perform as well as Method 1 or Method 3, but for the most part, the waveforms were reasonable at this speed even when operating in the base case of  $C_{bus} = 4$  mF despite the significant neutral point voltage imbalance. This is again related to the magnitude of the reference vector in the  $(\alpha - \beta)$  plane. As stated previously, the majority of the fundamental cycle is spent within the outer ring of triangles. Within the outer triangles, most of the dwell time of the active vectors is assigned to the large vectors, and the medium vectors and small vectors are applied for a shorter portion of the sampling period. Since only the medium and small vectors affect the neutral point balance, there is a significant imbalance in the neutral point voltage, but it is not large enough that the inverter operation fails. Although increasing the bus capacitance greatly improved the results from Method 2, this is generally not practical since cost increases significantly as capacitance increases.

### 5.5.2 Operation at Half Speed, Rated Load

In this section, the three space vector PWM methods are compared when each is operating at half speed, rated load. This comparison is based on the changes in the small voltage vectors during operation, the neutral point rms and mean values, and the total harmonic distortion of the line-to-neutral voltages, the line-to-line voltages,

and the phase currents.

The total harmonic distortion of each of the line-to-neutral voltages for space vector PWM Method 1, Method 2, Method 3, and Method 2 with increased bus capacitance is presented in Table 5.5. For this operating condition, the line-to-neutral voltage THD of Method 3 is slightly less than that of Method 1. Likewise, the increase in the bus capacitance improved the voltage THD of Method 2, which is comparable to that of Method 3. However, the voltage THD is very high for the base case of  $C_{bus} = 4$  mF for Method 2. This is because the neutral point voltage imbalance was large enough that the inverter performed extremely poorly.

Half Speed	Method 1	Method 2	Method 3	Method 2 ( $C_{bus}$ of 400mF)
$v_{An}$ THD	71.41%	382.76%	69.35%	69.74%
$v_{Bn}$ THD	71.41%	382.52%	69.34%	69.73%
$v_{Cn}$ THD	71.41%	383.14%	69.32%	69.75%
Average THD	71.41%	382.80%	69.34%	69.74%

Table 5.5: Summary of line-to-neutral voltage THD for all three methods at half speed, rated load.

The total harmonic distortion of each of the line-to-line voltages for space vector PWM Method 1, Method 2, Method 3, and Method 2 with increased bus capacitance is presented in Table 5.6. For this operating condition, the line-to-line voltage THD of Method 3 is less than that of Method 1. Likewise, the increase in the bus capacitance improved the voltage THD of Method 2, which is comparable to that of Method 3. However, the voltage THD of Method 2 is once again very high for the

base case of  $C_{bus} = 4$  mF. Again, this is because the neutral point voltage imbalance was large enough that the inverter performed extremely poorly.

Half Speed	Method 1	Method 2	Method 3	Method 2 ( $C_{bus}$ of 400mF)
$v_{AB}$ THD	58.59%	341.82%	56.02%	56.51%
$v_{BC}$ THD	58.60%	342.25%	56.00%	56.54%
$v_{CA}$ THD	58.60%	342.31%	56.01%	56.54%
Average THD	58.60%	342.13%	56.01%	56.53%

Table 5.6: Summary of line-to-line voltage THD for all three methods at half speed, rated load.

The total harmonic distortion of each of the phase currents for space vector PWM Method 1, Method 2, Method 3, and Method 2 with increased bus capacitance is presented in Table 5.7. The phase current THD is slightly lower in the case of Method 3 than in the case of Method 1. The phase current THD of Method 2 is nearly six times higher for the base case of  $C_{bus} = 4$  mF and slightly higher for the second case of  $C_{bus} = 400$  mF. The mean neutral point current is also very close to zero in both Method 1 and Method 3. Thus, even at lower output voltages, the switching patterns of Method 1 and Method 3 have relatively little effect on the neutral point voltage balance. In the base case of Method 2, the mean neutral point current is also very small. However, this is not caused by an improvement of the neutral point balance. This is a result of the neutral point becoming so imbalanced that the inverter essentially fails. When the bus capacitance is increased for Method 2, the absolute value of the mean neutral point current is very large, creating an imbalance in the

neutral point voltage.

Half Speed	Method 1	Method 2	Method 3	Method 2 ( $C_{bus}$ of 400mF)
$i_A$ THD	1.78%	10.63%	1.70%	2.23%
$i_B$ THD	1.78%	10.63%	1.70%	2.23%
$i_C$ THD	1.78%	10.63%	1.71%	2.23%
Average THD	1.78%	10.63%	1.70%	2.23%
$I_{NP,rms}$ ( $A_{rms}$ )	11.585	7.577	11.592	11.556
$mean(i_{NP})$ (A)	$-1.430E - 2$	$2.441E - 4$	$-1.126E - 2$	$-8.294$

Table 5.7: Summary of phase current THD and RMS value of neutral point current for all three methods at half speed, rated load.

The values of the 2-norm of the change in the small voltage vectors during operation of the inverter for space vector PWM Method 1, Method 2, Method 3, and Method 2 with increased bus capacitance are presented in Table 5.8. Only small vectors are included because at half speed operation, no medium vectors are applied. In most cases, both Method 1 and Method 3 have relatively little drift in the small vectors. For Method 2, in the base case of  $C_{bus} = 4$  mF, the deviation of the small vectors from their correct values is very large, thus indicating significant neutral point voltage imbalance. When the bus capacitance is increased to  $C_{bus} = 400$  mF, however, the deviation of the small vectors is greatly reduced. Even after applying the larger bus capacitance, the deviation in the small vectors of Method 2 is still very large.

When operating at half speed, Method 3 seems to produce slightly improved results over Method 1. However, switching losses are larger at low speed operation in Method 3 due to the increase in the IGBT switching frequency associated with

Half Speed	Method 1	Method 2	Method 3	Method 2 ( $C_{bus}$ of 400mF)
sm. vector 1 deviation (V)	0.1121	119.9	0.1428	1.734
sm. vector 2 deviation (V)	0.1142	119.8	0.1415	1.658
sm. vector 3 deviation (V)	0.1140	119.9	0.1441	1.725
sm. vector 4 deviation (V)	0.1155	119.8	0.1440	1.671
sm. vector 5 deviation (V)	0.1166	119.9	0.1485	1.738
sm. vector 6 deviation (V)	0.1184	119.8	0.1463	1.651

Table 5.8: Summary of the 2-norm of the drift of the voltage vectors for all three methods at half speed, rated load.

increasing the number of switching state transitions within each sampling period. Overall, Method 1 and Method 3 produce similar results in the open loop case. However, the inclusion of all redundant vectors in the switching patterns of Method 3 improves the ability of this method to reduce neutral point imbalance in a closed loop system through the dwell times of the redundant vectors.

Method 2 did not perform as well as Method 1 or Method 3 at this operating condition. In particular, with a dc bus capacitance of  $C_{bus} = 4$  mF, the drive was essentially inoperable based on the quality of the output waveforms. The poor performance of this method at low output voltages is a result of the application of only one of the redundant small vectors within a sampling period. Without applying both redundant vectors, the neutral point voltage imbalance was able to increase to the point where the output waveforms were unacceptably distorted. Even increasing the bus capacitance to  $C_{bus} = 400$  mF did not reduce the neutral point imbalance to the point where it was comparable to the low imbalance seen in both Method 1 and

Method 3. Overall, the switching pattern of Method 2 does not perform well when phase connections to the neutral point of the dc bus are made often as in the case of low speed operation.

## Chapter 6

### Conclusions and Recommendations for Future Work

#### 6.1 Conclusions

In this thesis, an introduction to both two-level space vector PWM and three-level space vector PWM was provided, and three different switching patterns for three-level space vector PWM that are found in the literature were reviewed. The first method is the simplest method and is based on the  $(0 - 1 - 2 - 7)$  two-level switching sequence. The second method, which is based on the  $(7 - 2 - 1 - 2)$  two-level switching sequence, is relatively simple and has the potential to reduce output current distortion in certain circumstances. However, the nature of the switching pattern can severely affect the neutral point voltage balance of the dc bus. The final method is similar to the first method for large modulation indices. However, as the modulation index decreases, the number of switching states per sampling period increases. By increasing the number of switching states per sampling period, this method can take advantage of all redundant switching states at the cost of a higher IGBT switching frequency.

A three-level NPC inverter model using MATLAB Simulink was created to simulate these three switching patterns when driving a case study IPM machine in a steady state configuration. The IPM machine circuit model was based on the state space representation of the synchronous machine, and all machine parameters were previously found using Finite Element Analysis. The line-to-neutral voltage, the line-to-line voltages, the phase currents, and the neutral point current were examined for each PWM method at two different machine operating conditions. By using two different operating conditions (rated speed, rated load and half speed, rated load), the three-level inverter was forced to operate in both three-level mode and two-level mode. The three space vector PWM methods were compared based on their simulation results.

From this work, some insight into the effects of a PM-induced back emf waveform from an IPM machine is gained. It was found for this particular case study machine that the harmonic content in the back emf distorted the line-to-neutral voltages for all three space vector PWM methods which led to distortion in the phase currents as well. The application of the switching states in Method 2 was found to affect the dc bus neutral point balance the most, which generally led to the worst inverter performance. The performance of Method 2 was improved by increasing the stiffness of the dc bus through a significantly larger bus capacitance. However, even with the increased bus capacitance, it did not perform as well as Method 1 and Method

3. In contrast, neither Method 1 nor Method 3 had a significant effect on the neutral point balance. The results from Method 1 and Method 3 were very similar except at low modulation indices, in which case the performance of the Method 3 inverter was slightly better than that of the Method 1 inverter. In general, each of these switching patterns has its own strengths and weaknesses. The first switching pattern has good all-around performance and is simple to implement. The second switching pattern may have some advantages in harmonic content if the neutral point balancing problem is addressed. This might be achieved by applying this switching pattern in an inverter topology that does not have a capacitor voltage balancing problem such as the cascaded H-bridge. The third switching pattern takes advantage of all redundant switching states, which can allow for more flexibility in the sharing of the dwell times among the switching states in a closed loop system.

## **6.2 Recommendations for Future Work**

Although some basic insight into the inherent properties of three space vector PWM methods is presented in this thesis, much more information about the relationship between space vector modulation methods and PM machines has yet to be found. This investigation could easily be expanded in several ways to provide a much wider view of multilevel space vector PWM in relation to PM and wound-field synchronous machines. First, this investigation should examine other PWM performance criteria

such as the balancing of power dissipation among switching devices. This is an important consideration with the constant push to improve system efficiency. Real effects of the drive, such as IGBT turn-on and turn-off times, should also be included in future work. This is very important because without a small dead time to account for the turn-on and turn-off time of the IGBTs, the phase legs could short-circuit the dc bus. The simulation of the three-level inverter should also be implemented using ANSYS Simplorer. Although controls are easily implemented in MATLAB Simulink, certain aspects of the drive operation, including the switching losses of the IGBTs, are not easily modeled. Unlike in Simulink, very detailed models of IGBTs may be built in Simplorer, which would simplify calculation of the switching losses and power dissipation imbalances in the inverter. As system efficiency requirements continue to increase, a calculation of the switching losses for each of the three switching patterns would be desirable.

This investigation could also be expanded to a much wider variety of PWM methods, both space vector methods and other methods including carrier-based PWM, selective harmonic elimination PWM, and various discontinuous PWM methods. This would provide a useful tool for comparing different PWM methods. The inherent differences between different synchronous machines might have a significant effect on the PWM methods applied to their drives as well. Thus, other synchronous machines beyond the case study in this work should be investigated with these PWM methods.

In particular, several replaceable rotors for the case study machine exist, including a rotor which induces a sinusoidal back emf. By repeating the simulations using this rotor, the effects of harmonics in the back emf may be isolated from the inherent qualities of these three switching sequences. Comparisons of these PWM methods in closed loop systems should also be investigated since modern drives generally do not operate in an open loop control configuration. This investigation might provide some insight for those who wish to choose a PWM method that is particularly effective for a specific closed loop application. Finally, these PWM methods should be implemented in a drive and compared based on the experimental results as well as the simulation results.

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## Appendix A

### Space Vector PWM Switching Tables

#### A.1 Switching Tables for Method 1

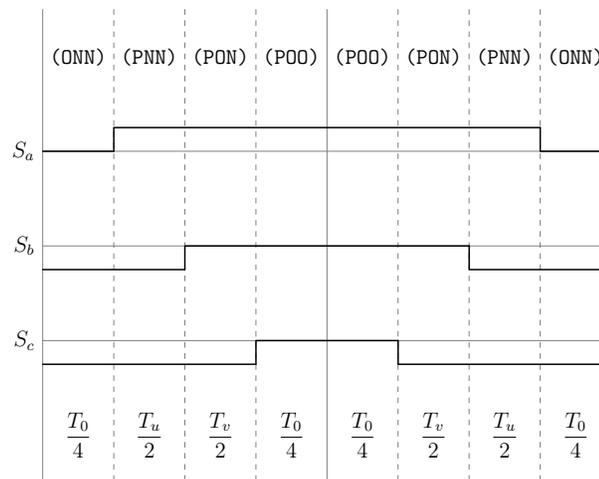


Figure A.1: Method 1 switching table Sector I, equivalent two-level sector I.

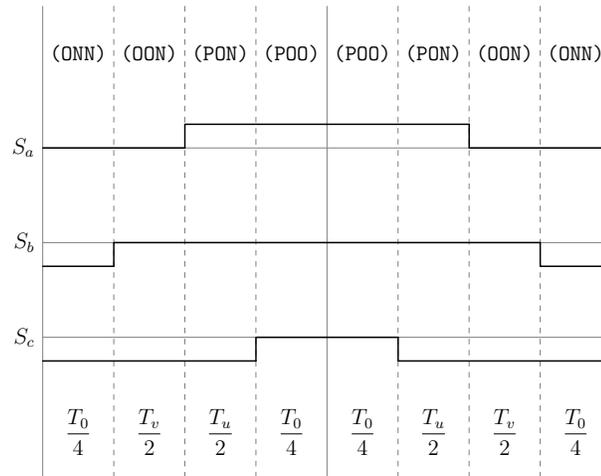


Figure A.2: Method 1 switching table Sector I, equivalent two-level sector II.

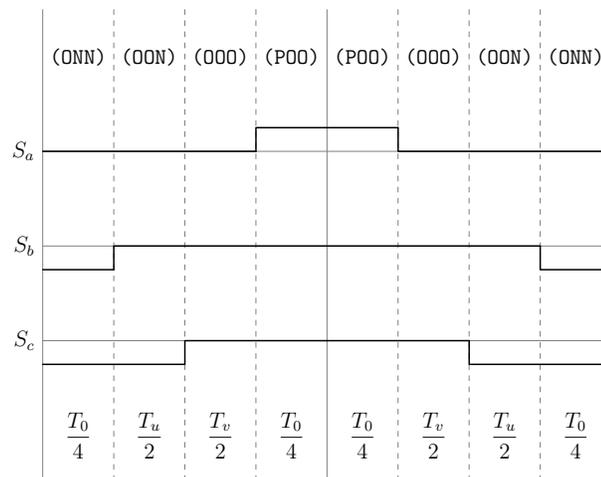


Figure A.3: Method 1 switching table Sector I, equivalent two-level sector III.

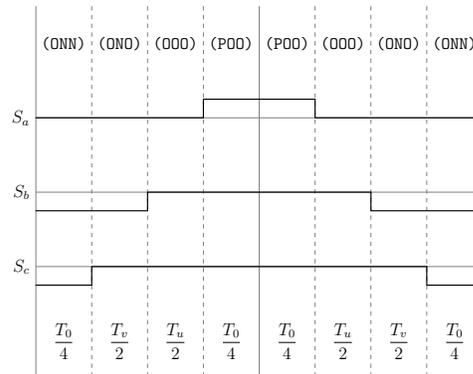


Figure A.4: Method 1 switching table Sector I, equivalent two-level sector IV.

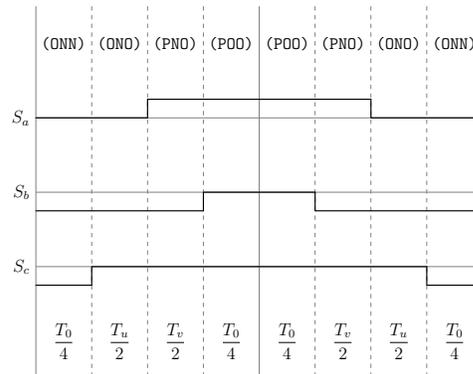


Figure A.5: Method 1 switching table Sector I, equivalent two-level sector V.

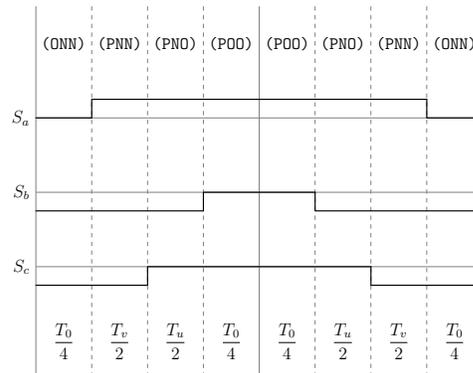


Figure A.6: Method 1 switching table Sector I, equivalent two-level sector VI.

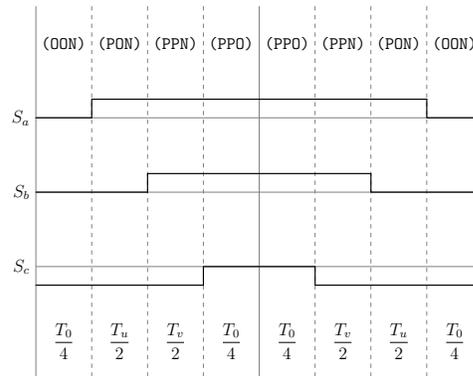


Figure A.7: Method 1 switching table Sector II, equivalent two-level sector I.

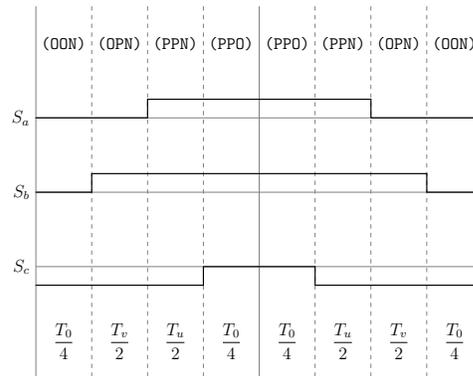


Figure A.8: Method 1 switching table Sector II, equivalent two-level sector II.

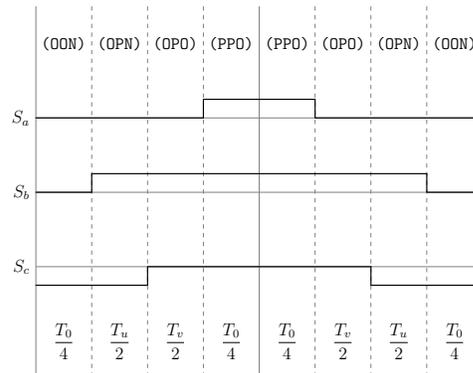


Figure A.9: Method 1 switching table Sector II, equivalent two-level sector III.

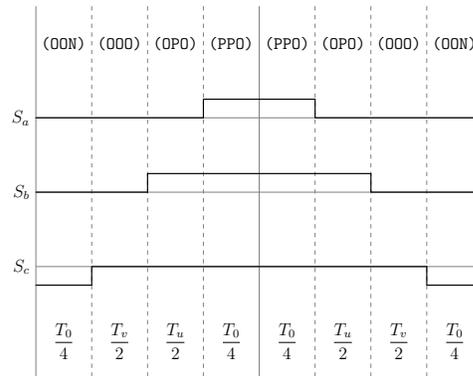


Figure A.10: Method 1 switching table Sector II, equivalent two-level sector IV.

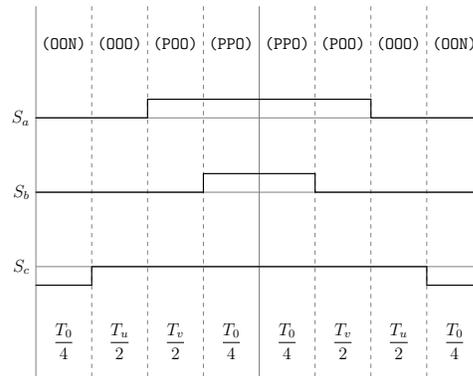


Figure A.11: Method 1 switching table Sector II, equivalent two-level sector V.

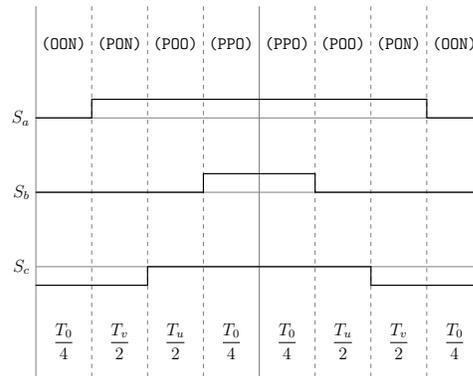


Figure A.12: Method 1 switching table Sector II, equivalent two-level sector VI.

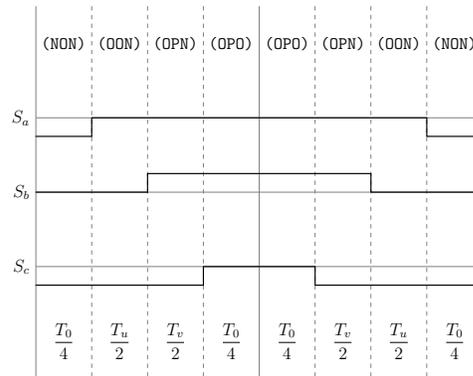


Figure A.13: Method 1 switching table Sector III, equivalent two-level sector I.

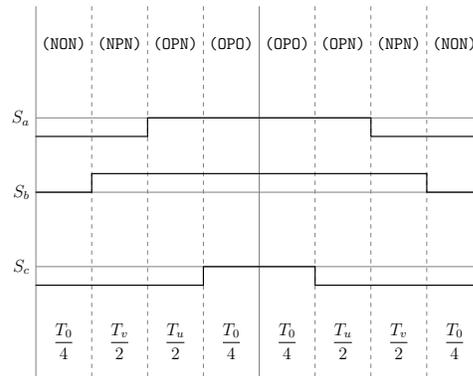


Figure A.14: Method 1 switching table Sector III, equivalent two-level sector II.

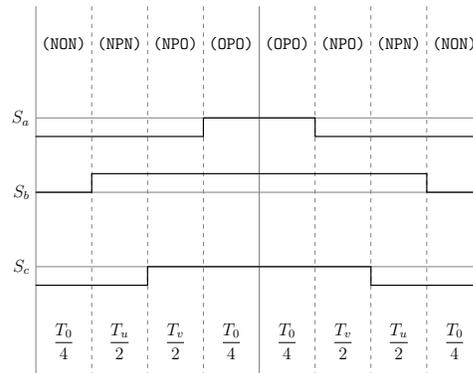


Figure A.15: Method 1 switching table Sector III, equivalent two-level sector III.

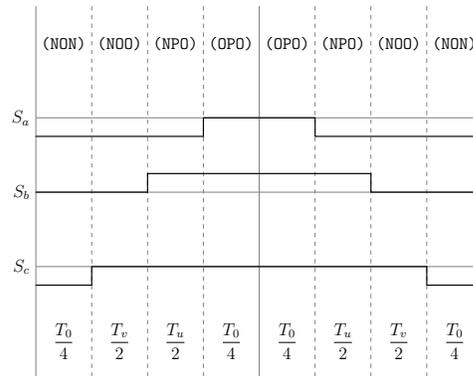


Figure A.16: Method 1 switching table Sector III, equivalent two-level sector IV.

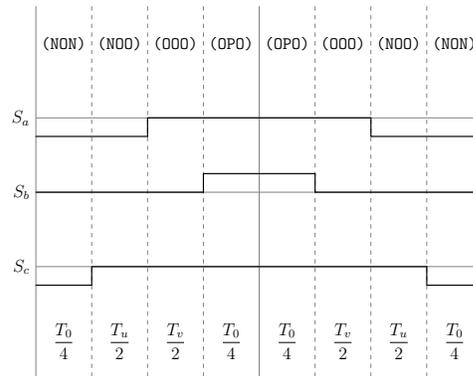


Figure A.17: Method 1 switching table Sector III, equivalent two-level sector V.

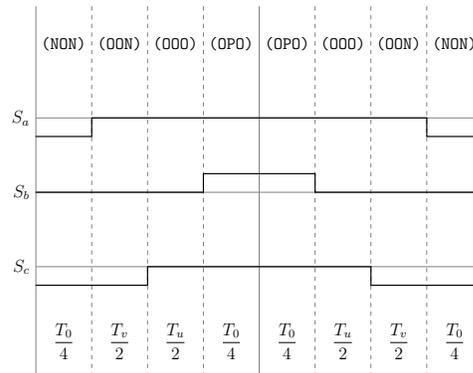


Figure A.18: Method 1 switching table Sector III, equivalent two-level sector VI.

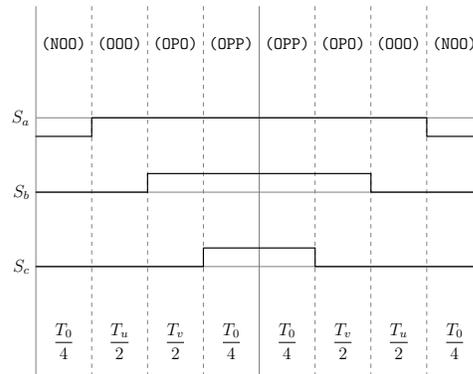


Figure A.19: Method 1 switching table Sector IV, equivalent two-level sector I.

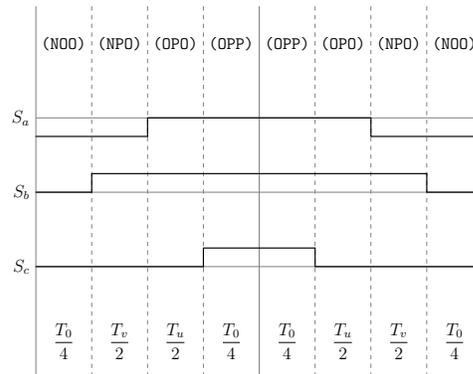


Figure A.20: Method 1 switching table Sector IV, equivalent two-level sector II.

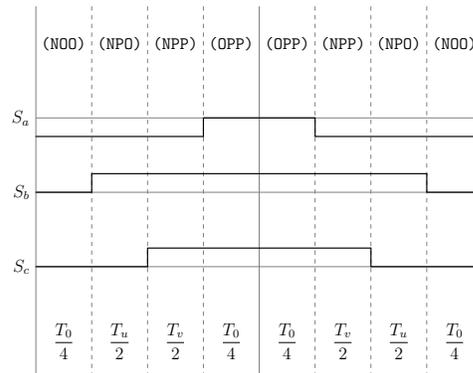


Figure A.21: Method 1 switching table Sector IV, equivalent two-level sector III.

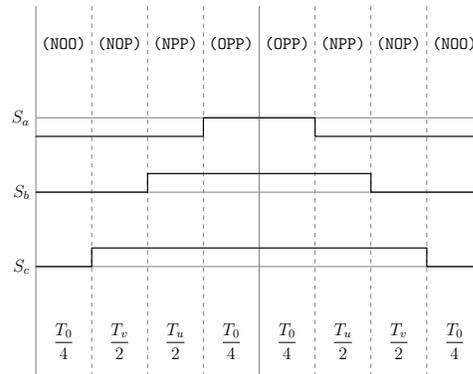


Figure A.22: Method 1 switching table Sector IV, equivalent two-level sector IV.

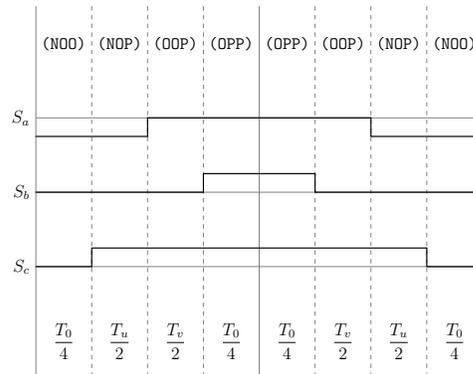


Figure A.23: Method 1 switching table Sector IV, equivalent two-level sector V.

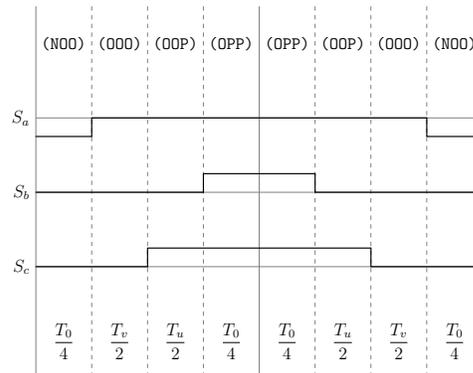


Figure A.24: Method 1 switching table Sector IV, equivalent two-level sector VI.

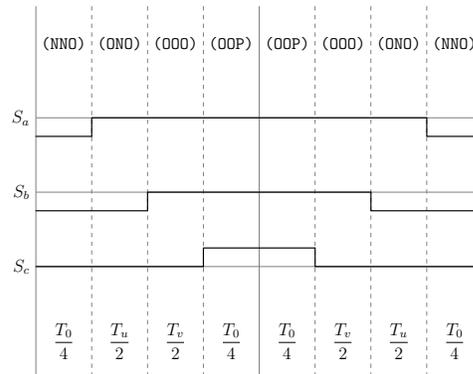


Figure A.25: Method 1 switching table Sector V, equivalent two-level sector I.

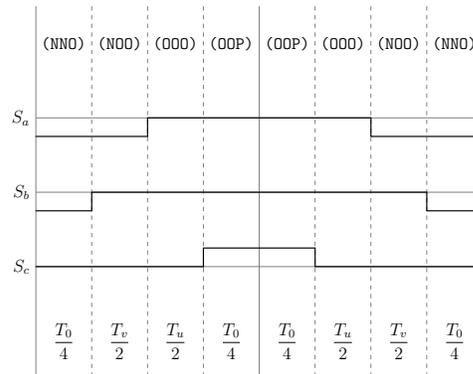


Figure A.26: Method 1 switching table Sector V, equivalent two-level sector II.

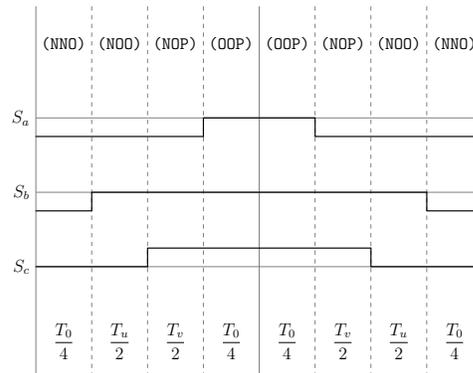


Figure A.27: Method 1 switching table Sector V, equivalent two-level sector III.

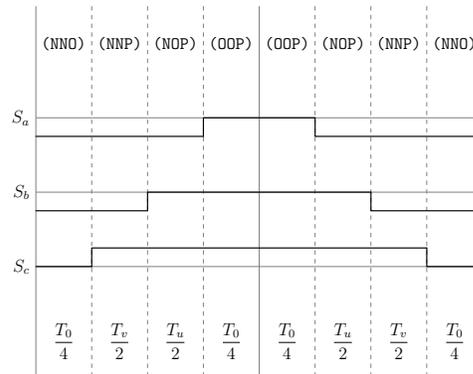


Figure A.28: Method 1 switching table Sector V, equivalent two-level sector IV.

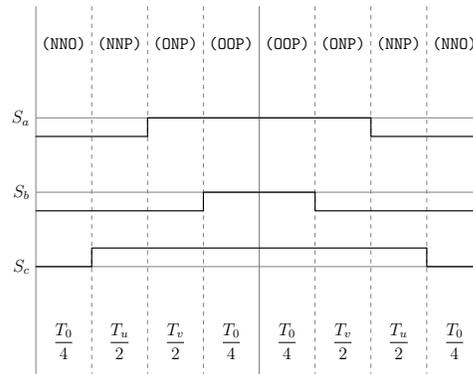


Figure A.29: Method 1 switching table Sector V, equivalent two-level sector V.

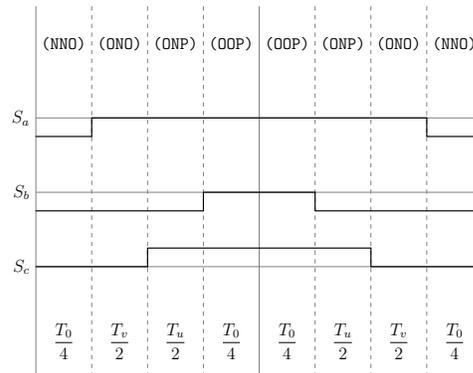


Figure A.30: Method 1 switching table Sector V, equivalent two-level sector VI.

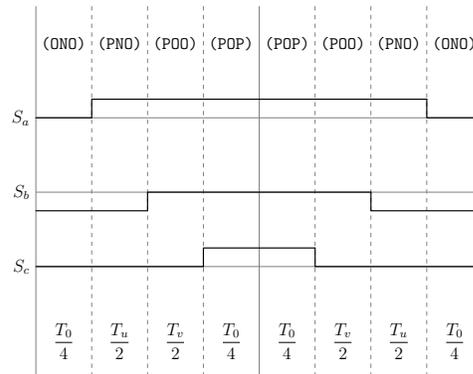


Figure A.31: Method 1 switching table Sector VI, equivalent two-level sector I.

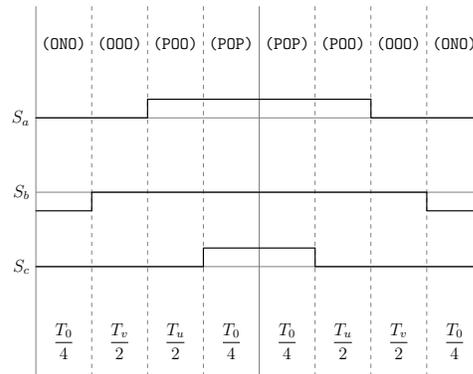


Figure A.32: Method 1 switching table Sector VI, equivalent two-level sector II.

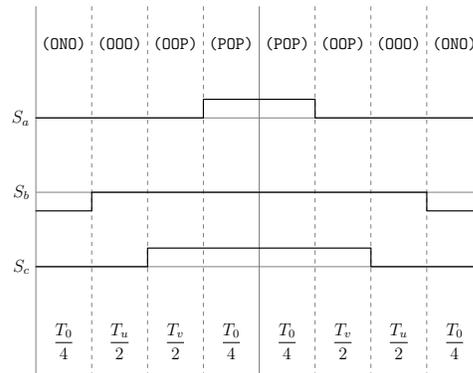


Figure A.33: Method 1 switching table Sector VI, equivalent two-level sector III.

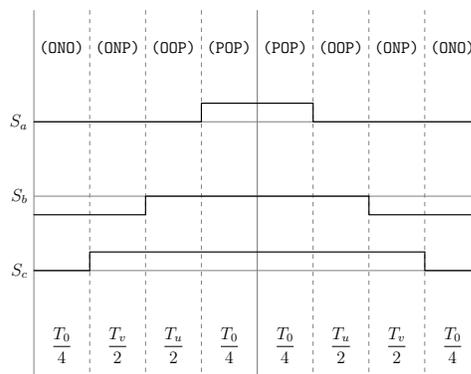


Figure A.34: Method 1 switching table Sector VI, equivalent two-level sector IV.

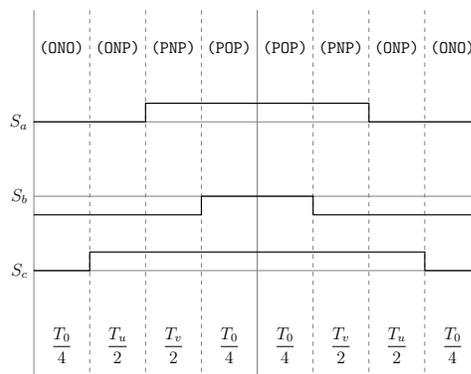


Figure A.35: Method 1 switching table Sector VI, equivalent two-level sector V.

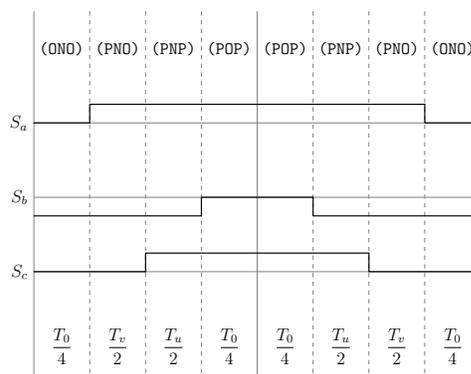


Figure A.36: Method 1 switching table Sector VI, equivalent two-level sector VI.

### A.2 Switching Tables for Method 2

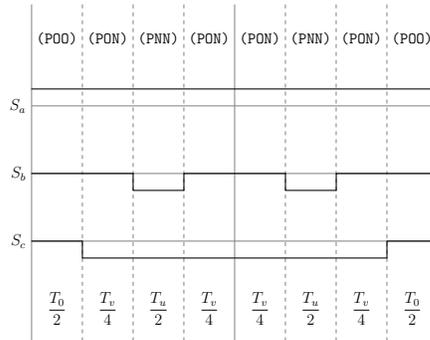


Figure A.37: Method 2 switching table Sector I, equivalent two-level sector I.

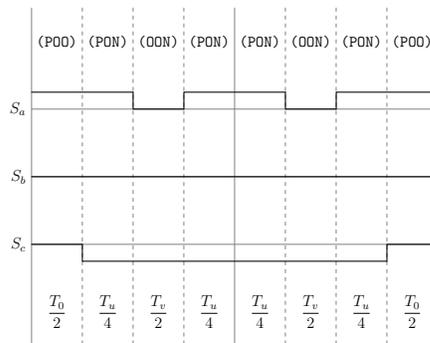


Figure A.38: Method 2 switching table Sector I, equivalent two-level sector II.

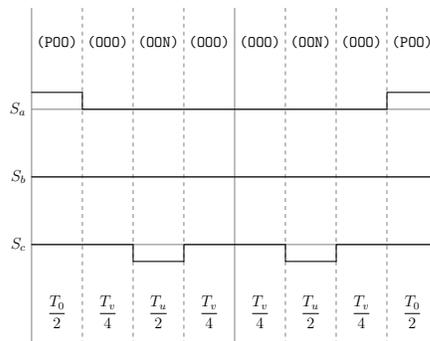


Figure A.39: Method 2 switching table Sector I, equivalent two-level sector III.

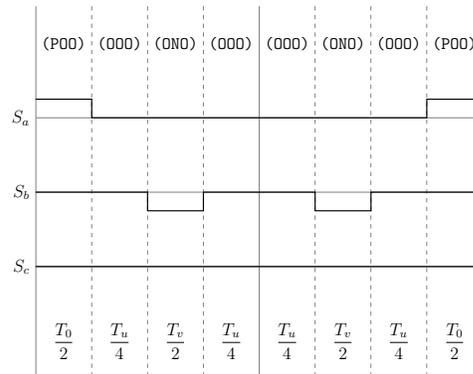


Figure A.40: Method 2 switching table Sector I, equivalent two-level sector IV.

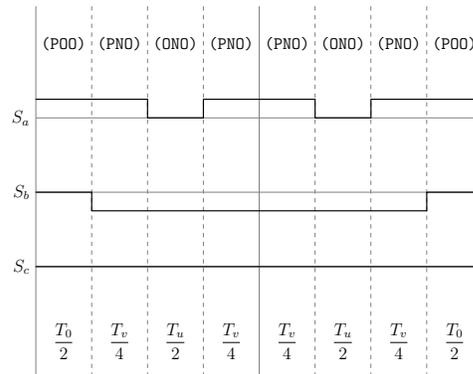


Figure A.41: Method 2 switching table Sector I, equivalent two-level sector V.

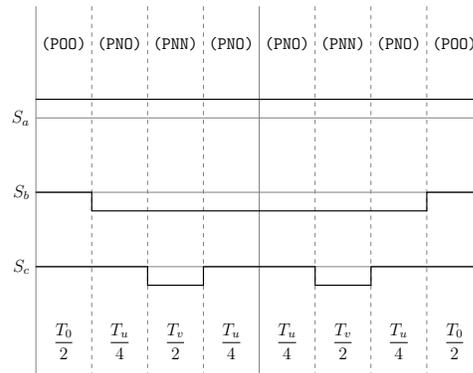


Figure A.42: Method 2 switching table Sector I, equivalent two-level sector VI.

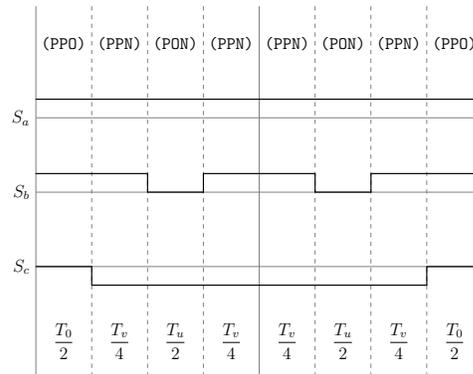


Figure A.43: Method 2 switching table Sector II, equivalent two-level sector I.

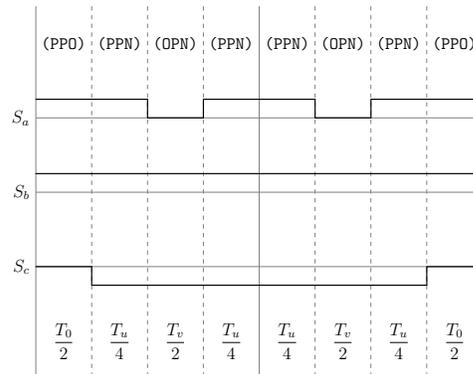


Figure A.44: Method 2 switching table Sector II, equivalent two-level sector II.

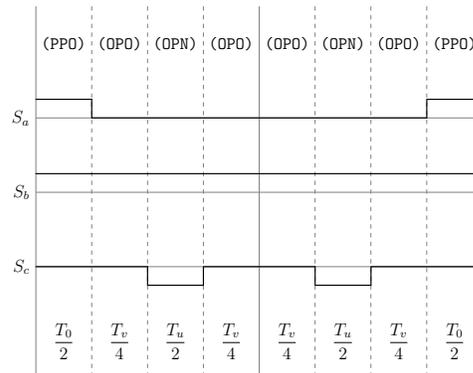


Figure A.45: Method 2 switching table Sector II, equivalent two-level sector III.

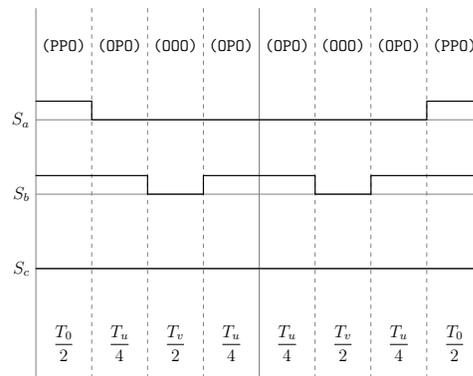


Figure A.46: Method 2 switching table Sector II, equivalent two-level sector IV.

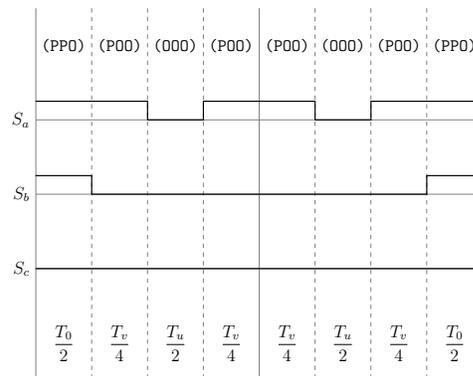


Figure A.47: Method 2 switching table Sector II, equivalent two-level sector V.

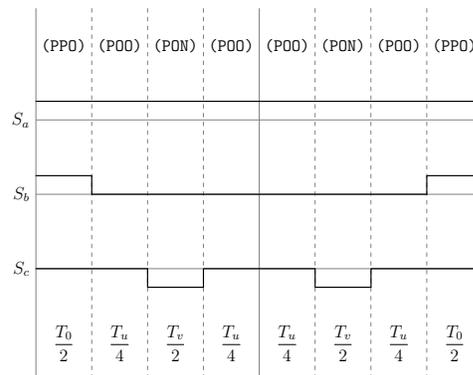


Figure A.48: Method 2 switching table Sector II, equivalent two-level sector VI.

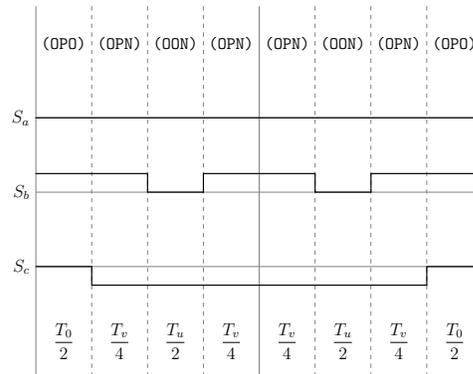


Figure A.49: Method 2 switching table Sector III, equivalent two-level sector I.

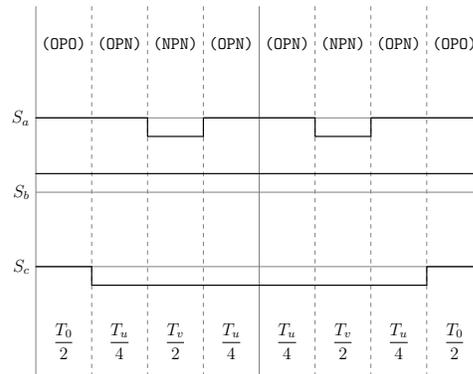


Figure A.50: Method 2 switching table Sector III, equivalent two-level sector II.

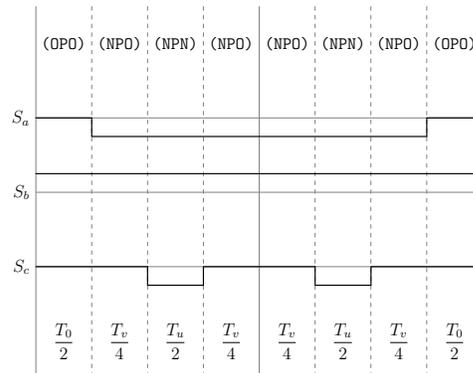


Figure A.51: Method 2 switching table Sector III, equivalent two-level sector III.

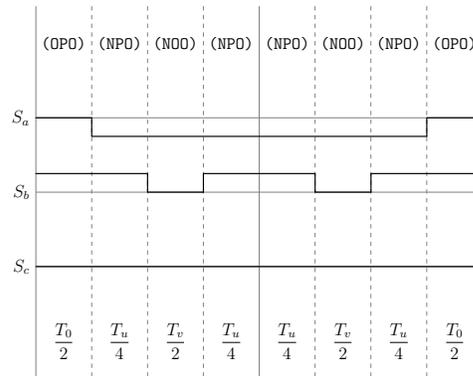


Figure A.52: Method 2 switching table Sector III, equivalent two-level sector IV.

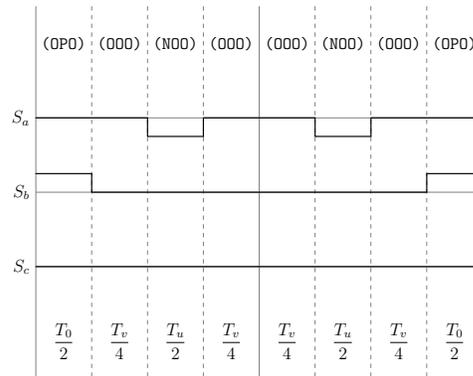


Figure A.53: Method 2 switching table Sector III, equivalent two-level sector V.

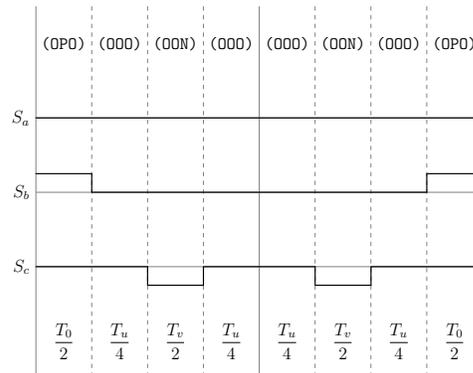


Figure A.54: Method 2 switching table Sector III, equivalent two-level sector VI.

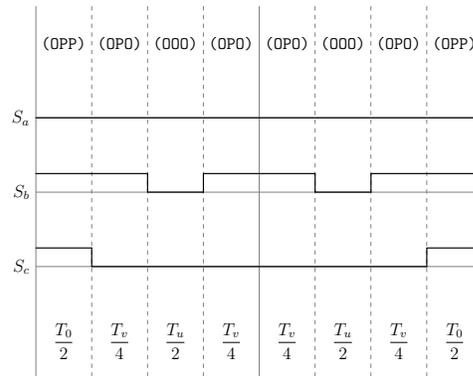


Figure A.55: Method 2 switching table Sector IV, equivalent two-level sector I.

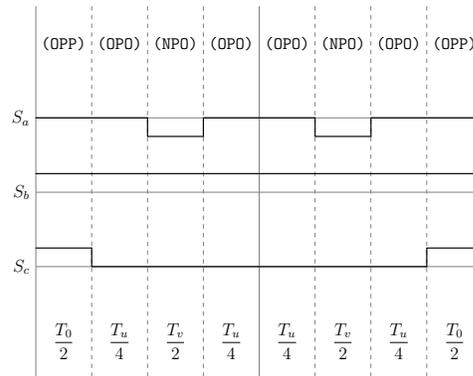


Figure A.56: Method 2 switching table Sector IV, equivalent two-level sector II.

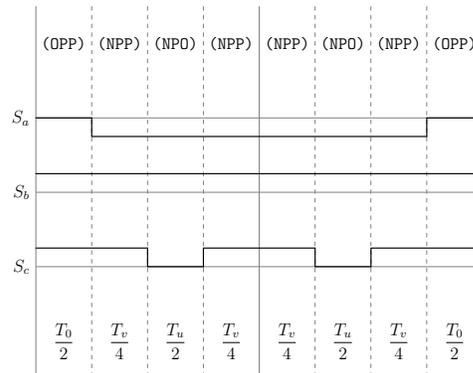


Figure A.57: Method 2 switching table Sector IV, equivalent two-level sector III.

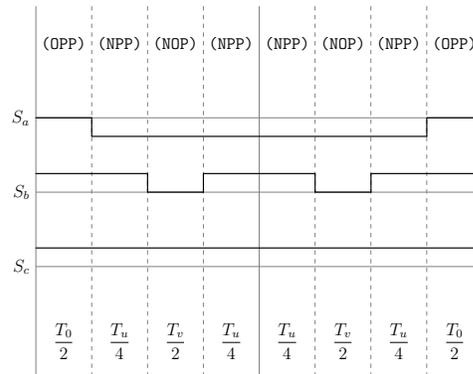


Figure A.58: Method 2 switching table Sector IV, equivalent two-level sector IV.

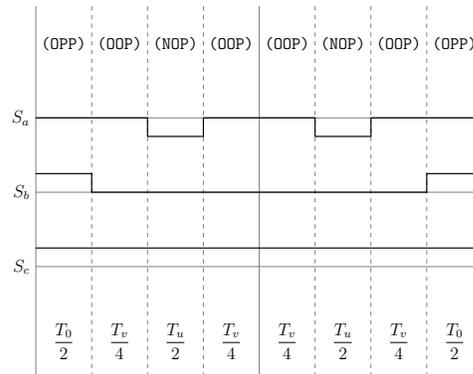


Figure A.59: Method 2 switching table Sector IV, equivalent two-level sector V.

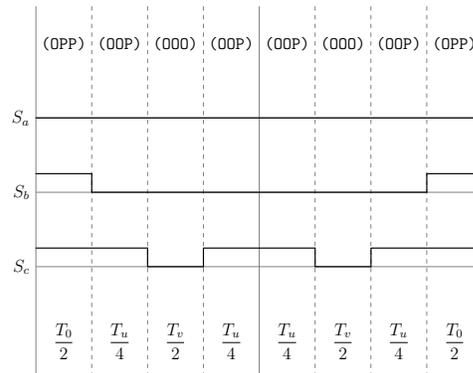


Figure A.60: Method 2 switching table Sector IV, equivalent two-level sector VI.

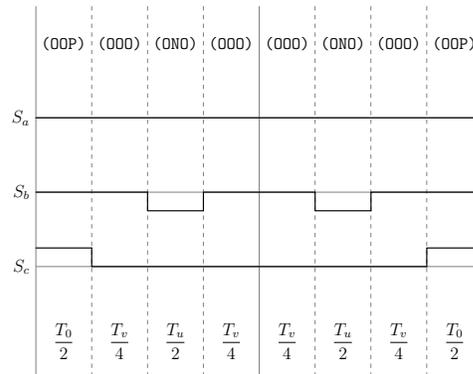


Figure A.61: Method 2 switching table Sector V, equivalent two-level sector I.

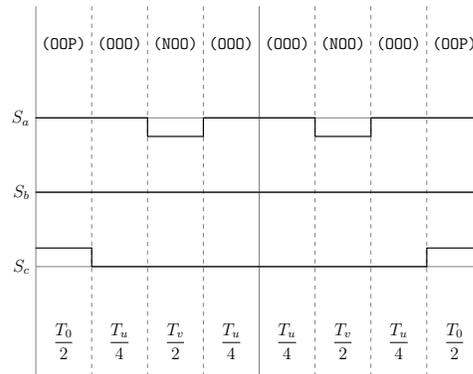


Figure A.62: Method 2 switching table Sector V, equivalent two-level sector II.

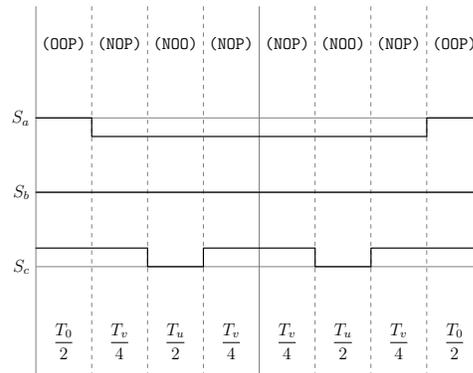


Figure A.63: Method 2 switching table Sector V, equivalent two-level sector III.

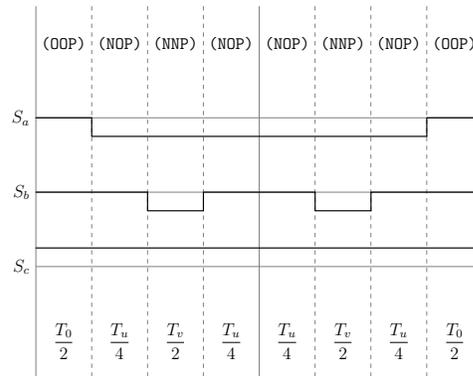


Figure A.64: Method 2 switching table Sector V, equivalent two-level sector IV.

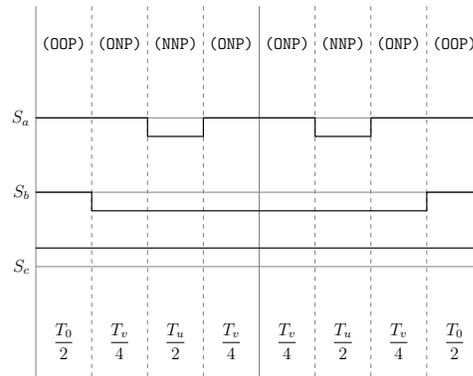


Figure A.65: Method 2 switching table Sector V, equivalent two-level sector V.

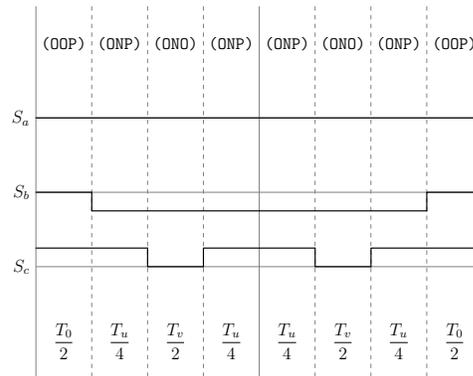


Figure A.66: Method 2 switching table Sector V, equivalent two-level sector VI.

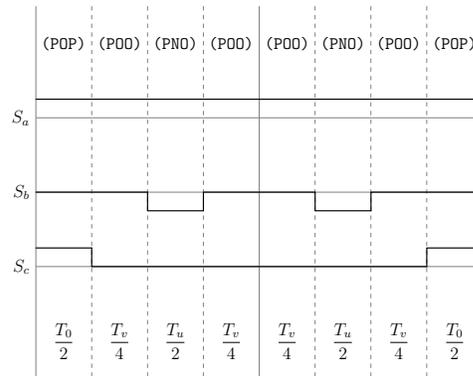


Figure A.67: Method 2 switching table Sector VI, equivalent two-level sector I.

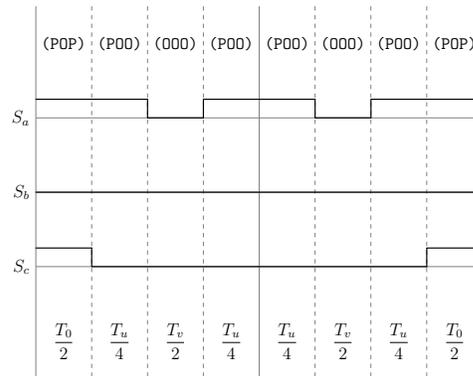


Figure A.68: Method 2 switching table Sector VI, equivalent two-level sector II.

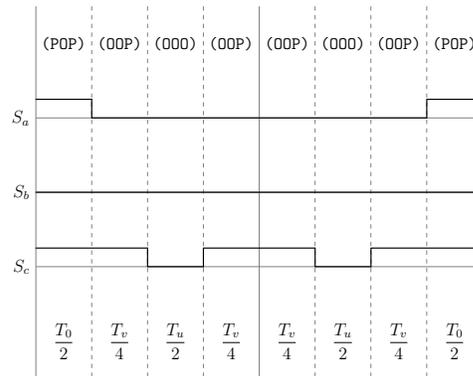


Figure A.69: Method 2 switching table Sector VI, equivalent two-level sector III.

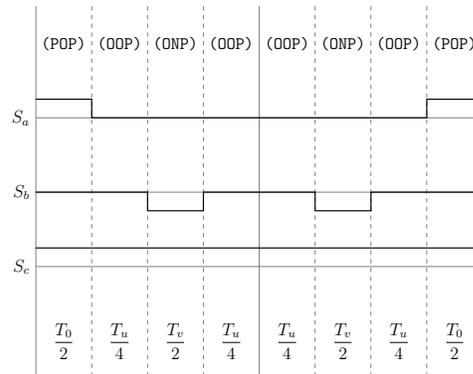


Figure A.70: Method 2 switching table Sector VI, equivalent two-level sector IV.

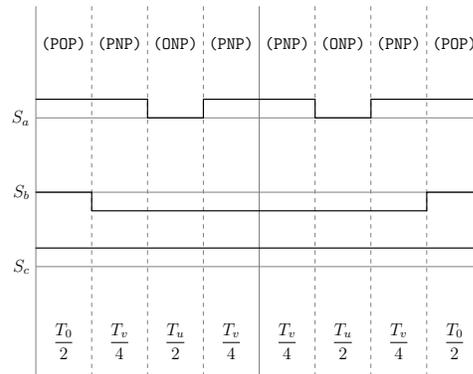


Figure A.71: Method 2 switching table Sector VI, equivalent two-level sector V.

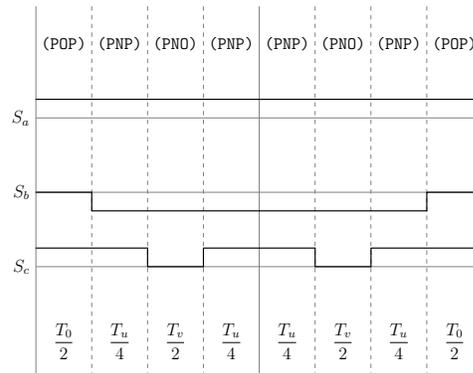


Figure A.72: Method 2 switching table Sector VI, equivalent two-level sector VI.

### A.3 Switching Tables for Method 3

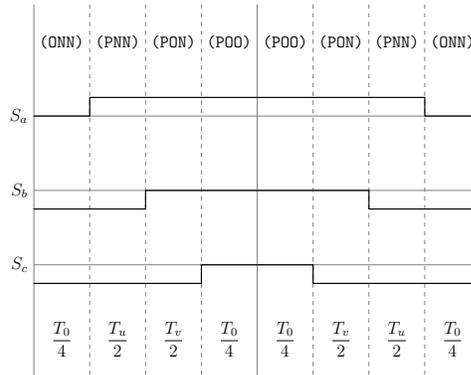


Figure A.73: Method 3 switching table Sector I, equivalent two-level sector I.

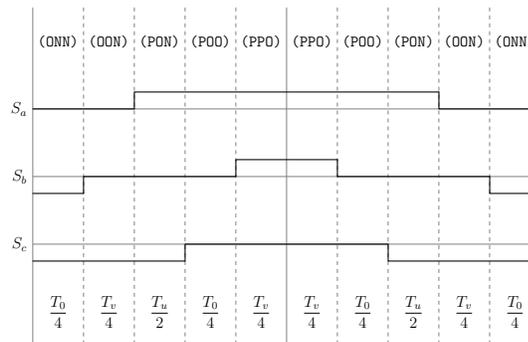


Figure A.74: Method 3 switching table Sector I, equivalent two-level sector II.

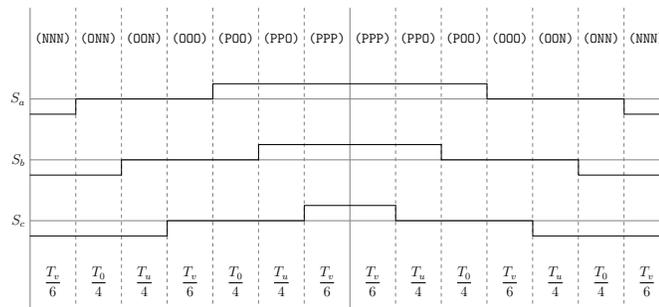


Figure A.75: Method 3 switching table Sector I, equivalent two-level sector III.

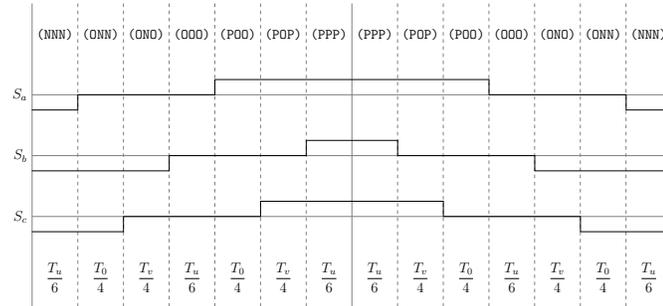


Figure A.76: Method 3 switching table Sector I, equivalent two-level sector IV.

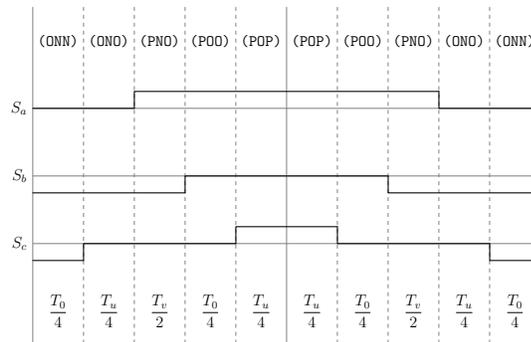


Figure A.77: Method 3 switching table Sector I, equivalent two-level sector V.

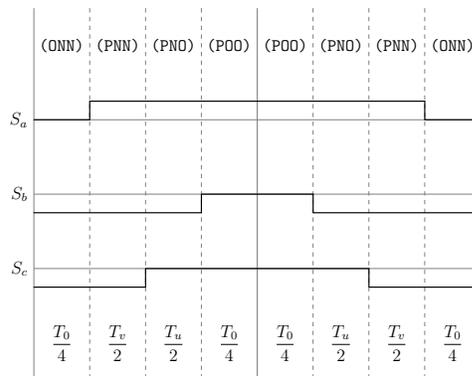


Figure A.78: Method 3 switching table Sector I, equivalent two-level sector VI.

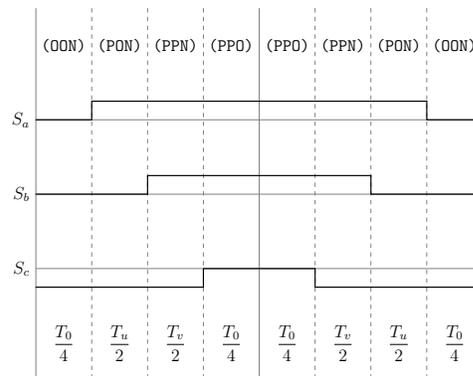


Figure A.79: Method 3 switching table Sector II, equivalent two-level sector I.

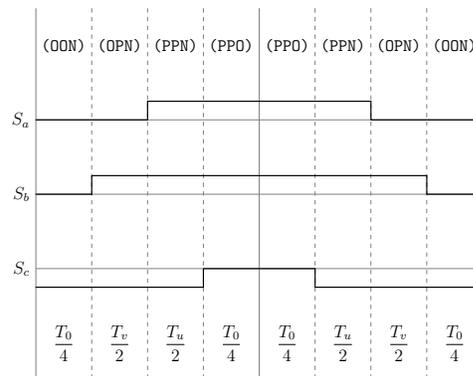


Figure A.80: Method 3 switching table Sector II, equivalent two-level sector II.

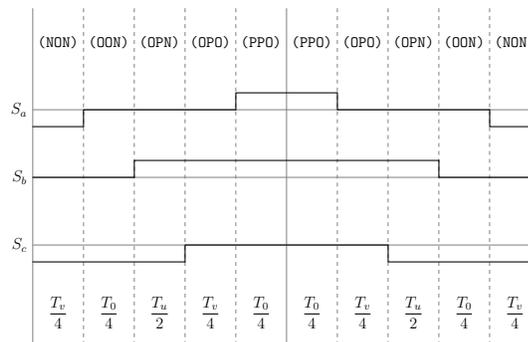


Figure A.81: Method 3 switching table Sector II, equivalent two-level sector III.

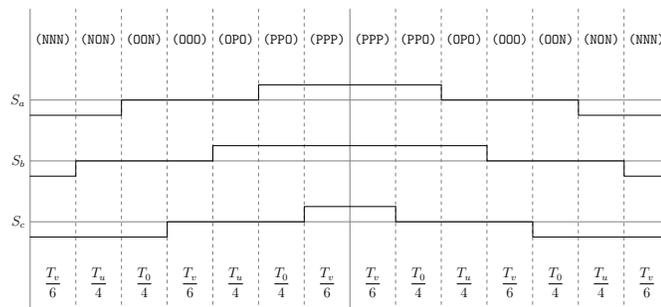


Figure A.82: Method 3 switching table Sector II, equivalent two-level sector IV.

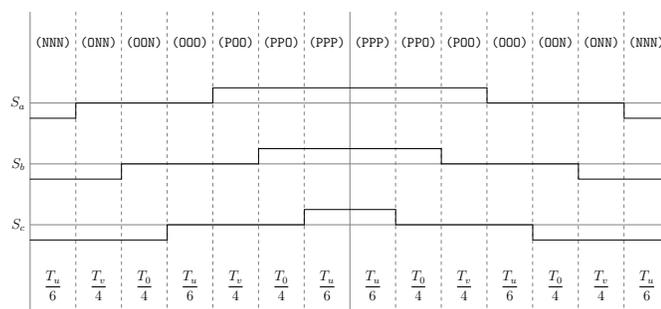


Figure A.83: Method 3 switching table Sector II, equivalent two-level sector V.

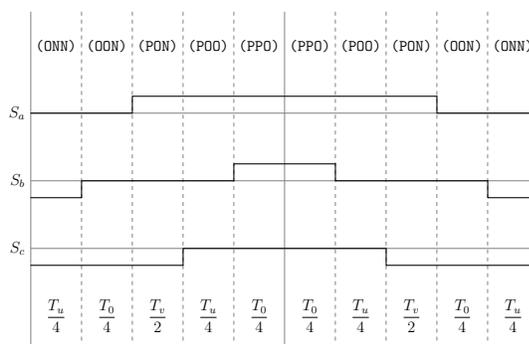


Figure A.84: Method 3 switching table Sector II, equivalent two-level sector VI.

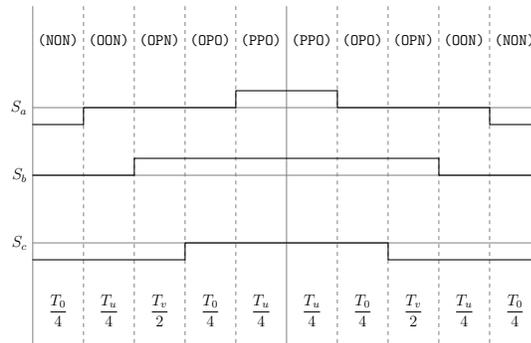


Figure A.85: Method 3 switching table Sector III, equivalent two-level sector I.

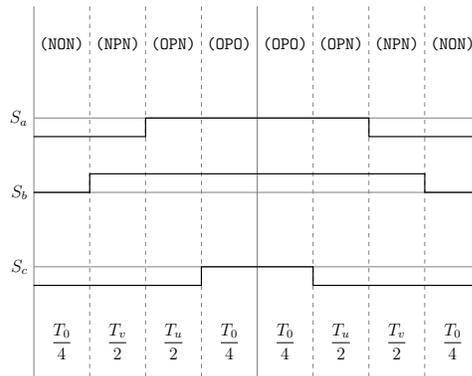


Figure A.86: Method 3 switching table Sector III, equivalent two-level sector II.

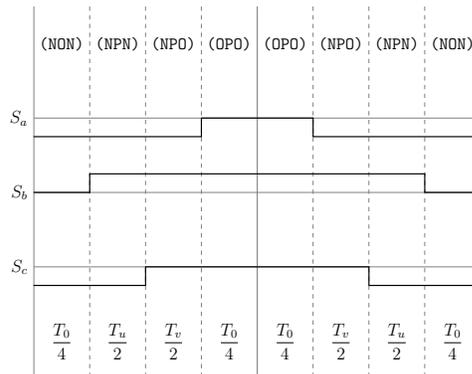


Figure A.87: Method 3 switching table Sector III, equivalent two-level sector III.

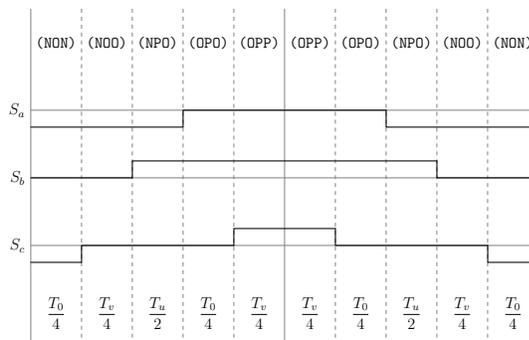


Figure A.88: Method 3 switching table Sector III, equivalent two-level sector IV.

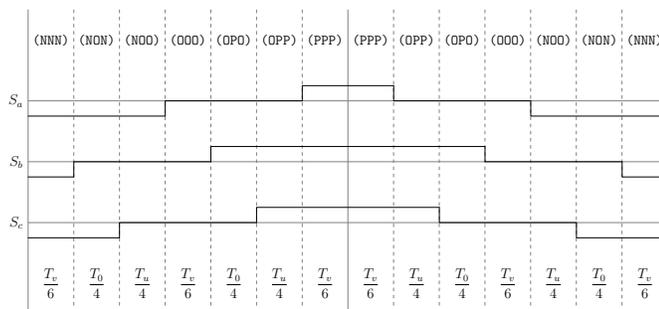


Figure A.89: Method 3 switching table Sector III, equivalent two-level sector V.

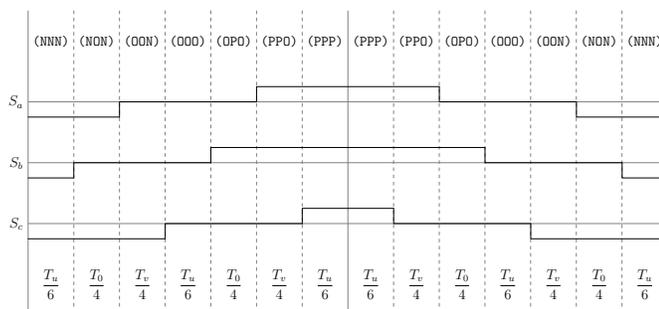


Figure A.90: Method 3 switching table Sector III, equivalent two-level sector VI.

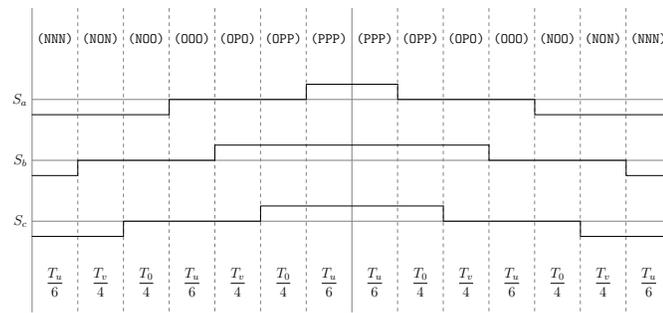


Figure A.91: Method 3 switching table Sector IV, equivalent two-level sector I.

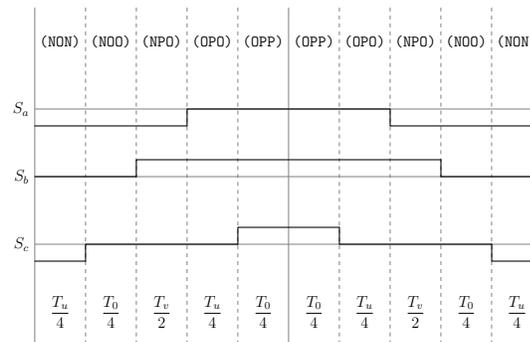


Figure A.92: Method 3 switching table Sector IV, equivalent two-level sector II.

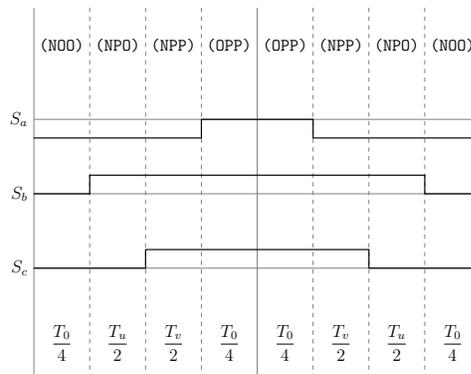


Figure A.93: Method 3 switching table Sector IV, equivalent two-level sector III.

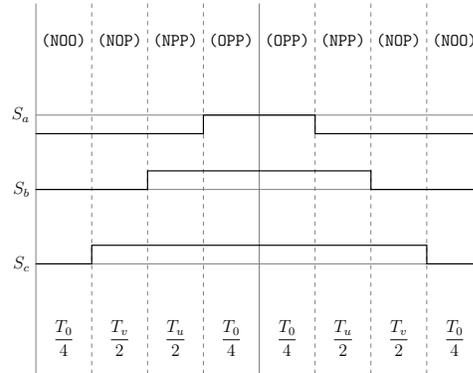


Figure A.94: Method 3 switching table Sector IV, equivalent two-level sector IV.

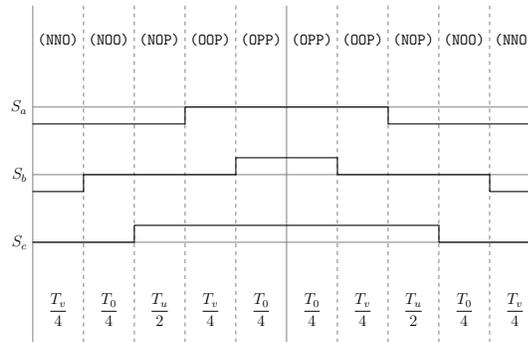


Figure A.95: Method 3 switching table Sector IV, equivalent two-level sector V.

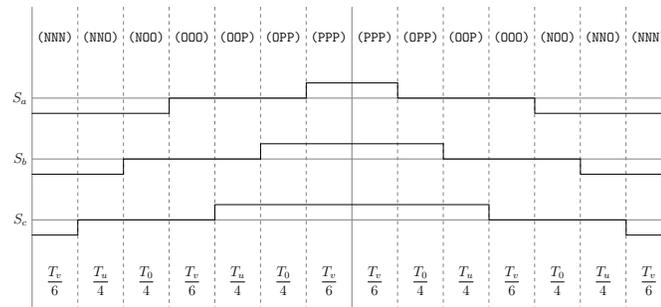


Figure A.96: Method 3 switching table Sector IV, equivalent two-level sector VI.

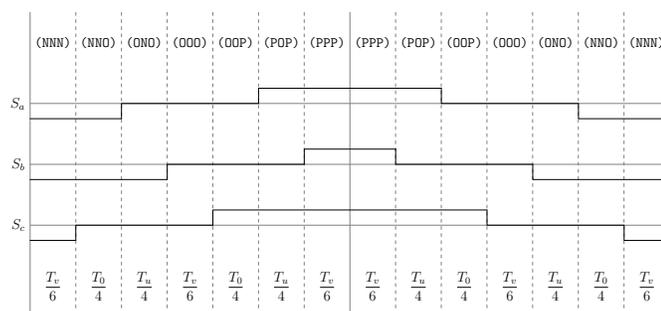


Figure A.97: Method 3 switching table Sector V, equivalent two-level sector I.

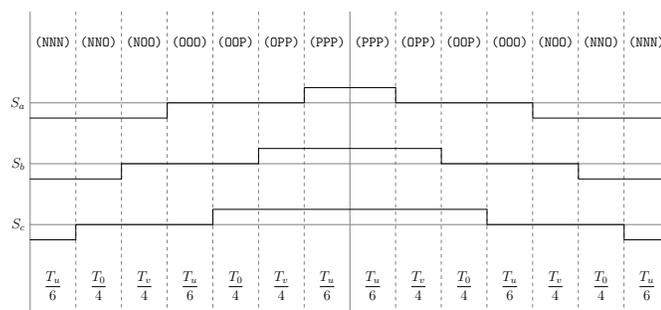


Figure A.98: Method 3 switching table Sector V, equivalent two-level sector II.

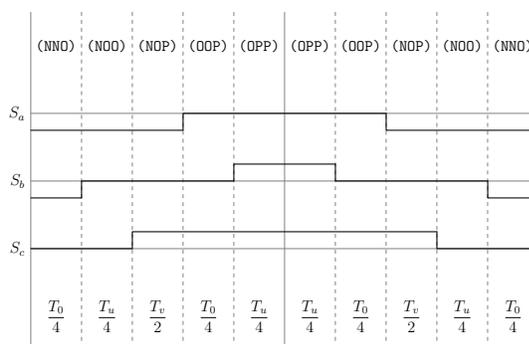


Figure A.99: Method 3 switching table Sector V, equivalent two-level sector III.

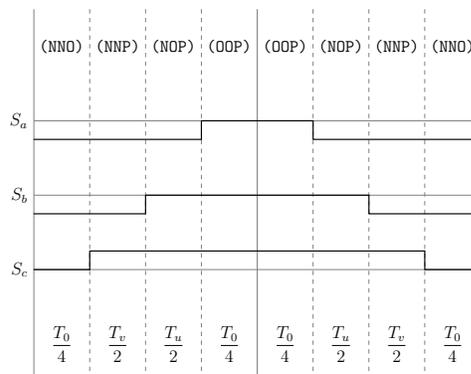


Figure A.100: Method 3 switching table Sector V, equivalent two-level sector IV.

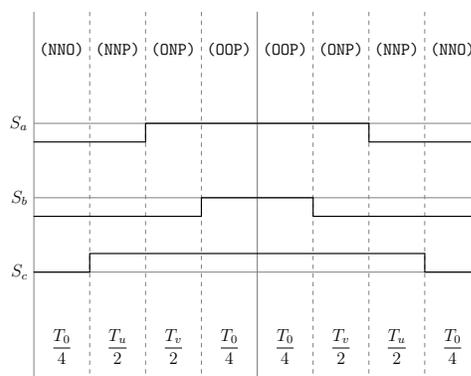


Figure A.101: Method 3 switching table Sector V, equivalent two-level sector V.

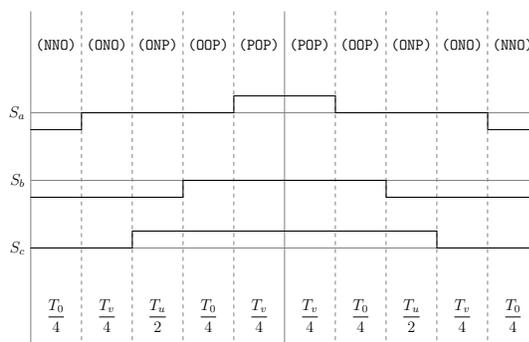


Figure A.102: Method 3 switching table Sector V, equivalent two-level sector VI.

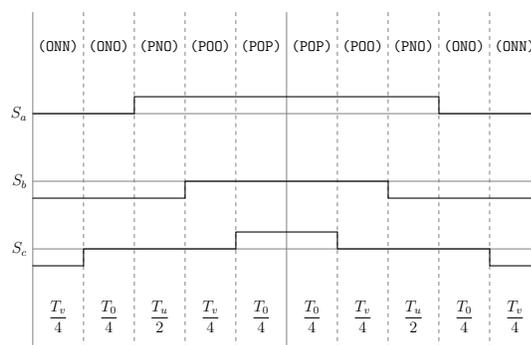


Figure A.103: Method 3 switching table Sector VI, equivalent two-level sector I.

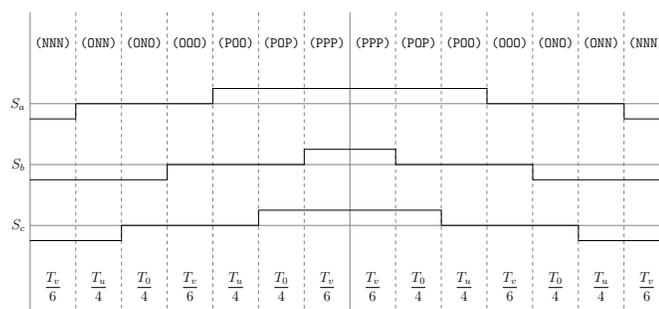


Figure A.104: Method 3 switching table Sector VI, equivalent two-level sector II.

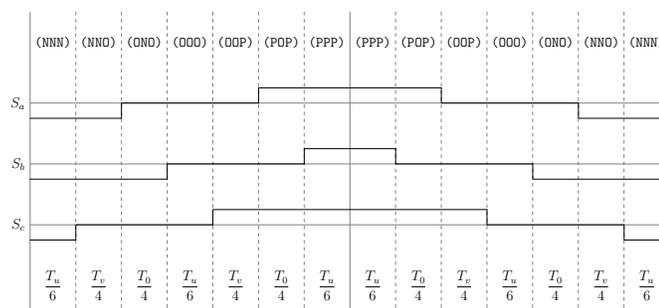


Figure A.105: Method 3 switching table Sector VI, equivalent two-level sector III.

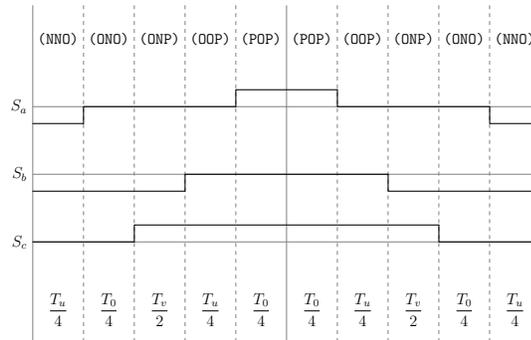


Figure A.106: Method 3 switching table Sector VI, equivalent two-level sector IV.

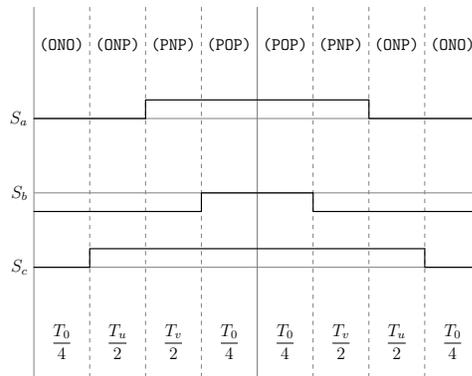


Figure A.107: Method 3 switching table Sector VI, equivalent two-level sector V.

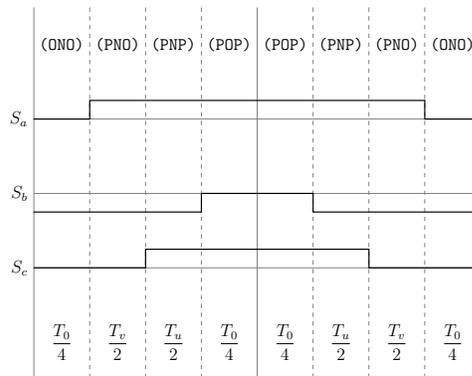


Figure A.108: Method 3 switching table Sector VI, equivalent two-level sector VI.