4-10-2011

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2011 International Reliability Physics Symposium, (April 10-14, 2011). DOI.

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Abstract:

We performed an experiment on AlGaN/GaN HEMTs with high voltage and high power as stressors. We found that devices tested under high power generally degraded more than those tested under high voltage. In particular, the high-voltage-tested devices did not degrade significantly as suggested by some papers in the literature. The same papers in the literature also suggest that high voltages cause cracks and pits. However, the high-voltage-tested devices in this study do not exhibit cracks or pits in TEM images, while the high-power-tested devices exhibit pits.

SECTION I. Introduction

GaN high electron mobility transistors (HEMT) are attractive to the United States Department of Defense for application in communications and sensing systems due to their ability to operate at high frequencies, high voltages, high temperatures, and high power. Interest in this technology is demonstrated by the Defense Advanced Research Projects Agency's Wide Bandgap Semiconductor initiative and by the Multidisciplinary University Research Initiatives funded by the Office of Naval Research and Air Force Office of Scientific Research. Despite the advantages of GaN HEMTs, there is concern that they do not have sufficiently long lifetimes for military systems. This concern has hampered their widespread acceptance and use.

Various stressors are claimed in the literature to cause degradation in GaN HEMTs. Stressor examples include high electric fields, high temperature with electrical stimulus, current with high electric field, and high drain bias with large rf drive. These stressors may result in various degradation mechanisms identified by signatures such as drain current degradation (itself a result of other signatures such as a decrease in transconductance, shifted threshold voltage, or increased on-resistance), an increase in gate leakage current, and/or reduced rfpower output.

Two failure mechanisms of concern for GaN HEMTs are identified in [1]. Traps are formed by high electric fields, “hot” electrons (accelerated by high electric fields to energies much greater than the thermal-equilibrium value), and high temperatures within the devices. HEMT performance is degraded since charge collects in the traps and is not available for conduction. The second mechanism, structural damage (called lattice disruptions, pits, or cracks), occurs due to high temperatures in combination with electrical stimulus. The authors propose a current and contaminant interaction that creates the lattice disruptions by an etching process. Device performance is degraded in this case due to a conduction path created in the material beneath the gate.

Another prominent theory of crack formation has been presented. In [2], [3], [4] a critical voltage V_{DG}, inducing the inverse piezoelectric effect, is claimed to cause the pits and cracks in the AlGaN barrier layer of a GaN HEMT. The theory is that the high electric field on the drain side of the gate causes increased mechanical strain in the piezoelectric materials of the HEMT. As the electric field is increased in this region, the mechanical stress causes the lattice to crack at a critical voltage. Once this defect is formed, electrons tunnel from the gate to the conduction channel, which degrades the drain current. Drain current degradation, as measured by a decrease in maximum drain current I_{Dmax}, reportedly occurs in high power state, OFF state, and, most severely, $V_{DS} = 0$ state tests. Degradation occurs in minutes as the stress voltage V_{DG} is applied in steps of 1 V per minute. I_{Dmax} is measured between steps.

Hot electron degradation is highlighted in [5]. Decreases in saturated drain-source current I_{DSS} and transconductance gm were caused by hot electrons created by simultaneous high current and high electric field, and not by electric field alone. GaN HEMTs tested in semi-ON-state conditions ($V_{DS} = 20\text{V}, V_{GS} = -5.5\text{V}$) experienced a 15% decrease in maximum gm, while the maximum gm of devices stressed in ON-state conditions ($V_{DS} = 20\text{V}, V_{GS} = 0\text{V}$) and OFF-state conditions ($V_{DS} = 20\text{V}, V_{GS} = -7.7\text{V}$) decreased less than 5%.

In addition, devices tested in ON-state conditions exhibited threshold voltage shifts while the same type of devices tested in OFF-state conditions did not.

Gate leakage current due to tunneling electrons as a dominant failure mechanism in GaN HEMTs is emphasized in [6]. When a HEMT is under a high drain voltage and driven by a large rf signal, the electric field at the drain side of the gate is sufficient to cause electrons to quantum mechanically tunnel from the gate electrode. These electrons can accumulate on the semiconductor surface, and thus be unavailable for conduction. They can also travel over the surface to the drain or through the A1GaN layer beneath the gate. Conduction from the gate to the drain along the surface is the dominant leakage path. The secondary path is through the A1GaN layer to the channel. Field plates can be used to reduce rf power degradation by decreasing the electric field at the gate. However, their use is detrimental to X-band and Ka-band devices due to the feedback capacitance the plates create. Surface passivation is a method to reduce the dominate leakage path over the surface.

With so many proposed stressors, degradation mechanisms, and degradation signatures, it is important to differentiate which stressors cause which effects. Due to this variety of stressors, mechanisms, and signatures, we have begun testing GaN HEMTs under multiple stressors to discover the relevant stressor or stressors, degradation mechanisms, and signatures. Knowing the limitations of a component in terms of potential parameter degradation is important to a circuit designer.

Two objectives of this study were to investigate the effects of different stressors and, specifically, to investigate whether high electric fields alone cause significant degradation.

SECTION II. Experiment Description

The devices used in this study were pulled from two wafers from the same lot. The A1GaN/GaN HEMT structure (from a commercial foundry) consists of a SiC substrate, a gate integrated field plate, and a source-connected field plate. Gate length is $0.5\ \mu m$ and periphery is $2 \times 50\ \mu m$. See Fig. 1 for a schematic diagram of the tested devices. Additional structure details can be found in [7] and [8].

Two different sets of test conditions were used: one was high voltage ($V_{DS} = 60$ V and 100 V) and low current with the gate pinched off ($(V_{GS} = -10\text{V})$) and the other was high dc power ($\geq 11\text{W/mm}$). In all cases, testing was conducted in the dark under dry nitrogen in an Accel-RF dc test station. The baseplate temperatures (Tbp) of the power test Conditions 1, 2, and 3 were selected so that the devices had similar estimated peak channel temperatures (based on device modeling). The highvoltage test Conditions 4 and 5 also had similar estimated peak channel temperatures. Fifteen devices were placed on test, with three devices at each of the five conditions listed in Table I.

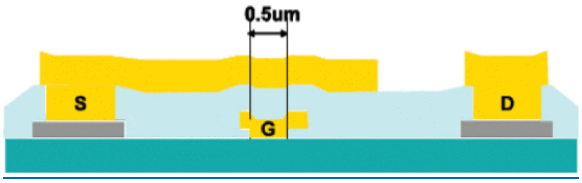

Figure 1. Schematic diagram of tested devices. [9]

For the upper set of power test conditions, the drain voltage V_{DS} was set and the gate voltage V_{GS} was adjusted until the target drain current I_D was reached (within the capabilities of the test station). After the initial setting of V_{GS}, V_{GS} was maintained for the duration of the test. The expected values of V_{GS} for the upper test conditions were based on previous testing and were not anticipated to cause forward gate current based on previous testing at $V_{GS} = 2$. For the lower set of high-voltage test conditions, both V_{DS} and V_{GS} were set, and the expected I_D was based on values seen during testing in a probe station.

The intended test sequence for the power test conditions was an initial characterization, followed by stress until I_D degraded to a pre-determined failure criterion, and ending with a post-failure characterization. However, test station measurement was not sufficiently precise and drift was too great to track I_D during stress, and the test was ended at 300 hours to conduct a characterization. The test station has since been upgraded to measure I_D with more precision and less drift.

The devices in the high-voltage set were characterized before stress and after each 100 hours of stress until reaching 300 total hours of stress. Their degradation was tracked with I_{DSS} and I_{Dmax}.

The characterization consisted of 1-V and transfer curves conducted at $T_{bp} = 70°\text{C}$ The 1-V curves swept V_{GS} from -5 to 1V in I-V steps and V_{DS} from 0 to 10 V in 19 steps. The transfer curve was conducted at $V_{DS} = 10$ V with V_{GS} being swept from -5 to 1 V in 0.333-V steps. The characterization was shown to be benign in on-wafer testing. I_{DSS} was measured at $V_{DS} = 10$ V and $V_{GS} = 0$. I_{Dmax} was measured at $V_{DS} = 10$ V and $V_{GS} = 1$. On resistance R_{on} was calculated with V_{DS}/I_{DS} at $V_{DS} = 0.556$ V and $V_{GS} = 0$ V ·.

To investigate whether the changes seen after 300 hours of testing would recover with rest, an additional period of testing was begun after more than 48 hours of rest at room temperature in the dark under dry nitrogen. Most devices did not complete the intended additional period of testing for various reasons. The main reason was system glitches that appear to have been caused by building power fluctuations, which also knocked offline a chiller for the cleanroom in the same building.

After testing, four devices were selected for analysis by thermal and photoemission imaging to find apparent weak spots. Then, those select devices were reviewed by scanning electron microscope prior to being imaged by tunneling electron microscope to reveal physical degradation.

TABLE I. TEST CONDITIONS FOR PRELIMINARY STUDIES

Condition	$T_{bp}(°\text{C})$	V_{DS} **(V) _**	**Target** I_D **(mA/mm)**	P_{diss} **(Wimm)**	**Expected** V_{GS} **(V)**
1	245	20.0	550	11.0	2
2	133	40.0	550	22.0	<2
3	130	60.0	367	22.0	< 0.5
			Approx. I_D **(mA/mm)**		**Set** V_{GS} (V)
4	245	60.0	0.03	0.0018	−10
5	245	100.0	2	0.2	−10

SECTION III. Results and Discussion

The results of thirteen of the fifteen devices placed on test are compared. Of the two devices that are not included in the comparison, one device tested at Condition 4 apparently suffered infant mortality before 100 hours. Another device tested at Condition 3 reached the pre-determined failure criteria for I_D at 133 hours. Two devices that are included in the comparison did not achieve 300 hours. One device tested at Condition 3 reached the pre-determined failure criteria for I_D during stress at 253 hours due to the test station's I_D measurement drift; this device is included in the comparison because other devices (not included in this study) tested at similar conditions showed no significant changes in transfer curves at 200 at 400 hours. The other device was tested at Condition 5 and reached only 263 hours also due to the test station's $I_D$measurement drift; this device is included because it showed less than 2% change in transfer curves from 263 to 1017 hours in subsequent testing.

A summary of the results of the thirteen devices is in Table II. The percentages are average absolute changes from the pre-stress to the post-stress characterizations since two high-voltage-tested devices were exceptions to the general trends in changes to the selected parameters. One device at Condition 4 and one device at

Condition 5 exhibited increases in I_{DSS} and negative threshold voltage V_T shifts. The same device at Condition 5 also exhibited an increase in I_{Dmax} (see Fig. 3). All devices experienced decreases in peak transconductance g_{mp} and increases in R_{on}. The other general trends were positive threshold voltage shifts and decreases in $I_{Dmax}$and I_{DSS}.

Fig. 2 shows the transfer and transconductance curves of a typical (meaning, following the general trends in I_{Dmax}, I_{DSS}, and V_T) high-voltage-tested device. Fig. 3 shows the transfer and transconductance curves of one of the two exceptional high-voltage-tested devices. Figs. 2 and 3 illustrate the variability in the performance of the tested HEMTs. Although discovering the cause of the negative threshold voltage shift in Fig. 3 was not an objective of this study, a possible explanation is a trapping phenomenon near the gate [10], [11]. The transfer and transconductance curves of Fig. 4 are representative of the power-tested devices. Figs. 3 and 4 contain the transfer and transconductance curves from testing subsequent to the initial 300 hours; these curves show little change after 300 hours.

Comparing the two sets-high voltage and high power since estimated peak channel temperatures were similar for the respective sets, the devices tested at high power changed more significantly than the devices tested at high voltages and low current, except in g_{mp}. The high-power-tested devices changed more in V_T (13.0%), I_{Dmax} (11.3%), I_{DSS} (14.8%), and R_{on} (11.5%) than the devices tested at high voltage (6.01%, 4.89%, 6.28%, and 4.64%, respectively). Unlike [5], threshold voltage shifts were seen from both ON- and OFF-state conditions. Peak transconductance g_{mp} changed more for the devices tested at high voltage (4.10%) than for the devices tested at high power (2.25%). Similar to [5], the decrease in g_{mp} of devices tested in ON-state and OFF-state was less than 5%. The different degradation signatures in the two sets indicate different degradation mechanisms.

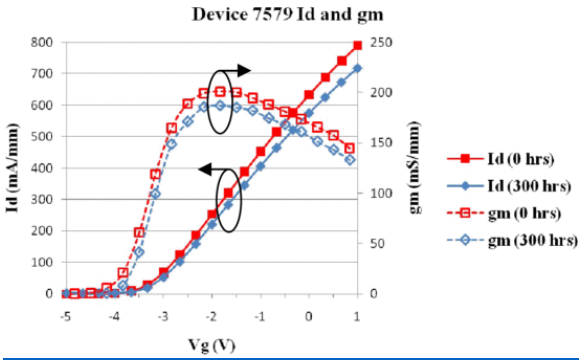

Figure 2. Transfer and transconductance curves at 0 and 300 hours of typical high-voltage-tested device. Device 7579 was tested at Condition 5.

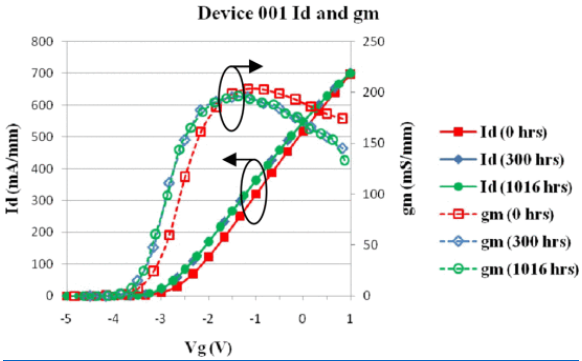

Figure 3. Transfer and transconductance curves at 0, 300, and 1016 hours of exceptional high-voltage-tested device. Device 001 was tested at Condition 5.

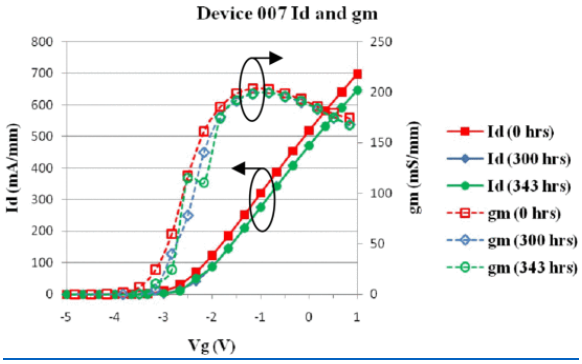

Figure 4. Representative transfer and transconductance curves at 0, 300, and 343 hours of high-power-tested device. Device 007 was tested at Condition 1.

TABLE II. AVERAGE ABSOLUTE PERCENTAGE CHANGES IN PARAMETERS AFTER 300 HOURS

Condition	g_{mp}	V_T	I_{Dmax}	I_{DSS}	R_{on}
1	1.68%	10.8%	8.80%	11.8%	8.06%
2	1.98%	10.9%	10.9%	13.2%	12.23%
3	3.53%	19.4%	15.7%	21.5%	15.43%
4	3.45%	5.95%	4.51%	5.09%	3.78%
5	4.53%	6.05%	5.15%	7.08%	5.21%

There appears to be a correlation between higher drain biases and greater degradation. Although the estimated peak channel temperatures were similar for Conditions 1, 2, and 3 and separately for Conditions 4 and 5, the average absolute change for the four parameters increased with drain voltage (see Table II). Despite that apparent drain bias and degradation correlation, significant drain current degradation (> 10%) caused by high biases alone was not seen. Comparing Conditions 4 and 5 with other published OFF-state conditions [2], [3], the biases of Conditions 4 and 5 were at least 10 V higher. Yet, the significant degradation seen at the lower voltages after minutes of stress in the other studies was not seen at the higher voltages after hours of stress in this study.

The changes that occurred in the devices during stress seem to be unrecoverable with rest. The average change in I_{Dmax} between the value measured at 300 hours of stress and the value measured after rest was 0.01% with a maximum of 2.3% and a minimum of -2.37%. For I_{DSS}, the average change was 0.12% with a maximum of 2.26% and a minimum of-2.29%. Both maximums were measured on one device and both minimums were measured on another. All other percent changes were less than 1% in absolute value. In addition to the changes in I_{Dmax} and I_{DSS} before and after rest, four of six power-tested devices that began the additional testing period required greater gate voltages to attain the target drain current-an indication of permanent degradation.

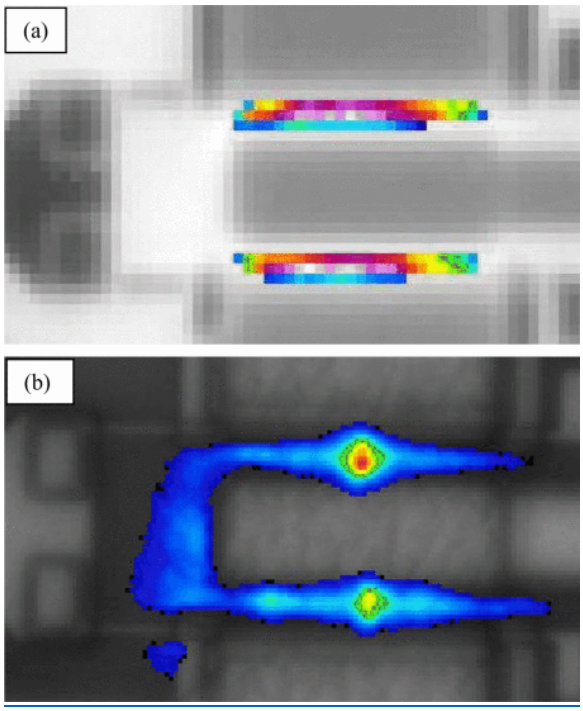

Figure 5. Device 001 (high-voltage-tested) at a baseplate of 85°C. The upper middle spot was targeted for TEM imaging. (a) IR (radiance) image at 15X magnification. $V_{DS} = 40\text{V}, I_D = 10\text{mA}, V_{GS} = -2.42\text{V}, I_G = -5\mu\text{A}$ (b) PE image at 20X magnification. $V_{DS} = 100\text{V}, I_D = 11\mu\text{A}, V_{GS} = -10$.

After stress testing, we investigated the four select devices by thermal and photoemission imaging in a Quantum Focus Instruments InfraScope™. In three of the four devices, hot spots corresponded with bright spots. We delivered these four devices to NanoTEM for transmission electron microscope (TEM) imaging at the hot and bright spots. Although Device 001 is exceptional (with a negative V_T shift and increases in I_{Dmax} and I_{DSS}), its transfer and transconductance curves and its infrared (IR), photoemission (PE), and TEM images are shown since it had notable IR and PE images, whereas the other imaged high-voltage-tested device did not. Fig. 5contains IR (radiance) and PE images for the high-voltage-tested Device 001 whose transfer and transconductance curves are in Fig. 3. (An insufficient number of samples were imaged by IR and PE to determine whether the features of Fig. 5 correlate to the negative threshold voltage shift of Fig. 3.) The IR (radiance) and PE images in Fig. 6 are those of the power-tested Device 007 whose transfer and transconductance curves are in Fig. 4.

The TEM images of Devices 001 and 007 are in Fig. 7. As in the TEM image of Device 001 (stressed at Condition 5), the other high-voltage-tested part that was imaged by TEM, Device 7632 (stressed at Condition 4), does not exhibit a crack or pit at the drain edge of the gate. This is contrary to the findings reported in [4]. However, *i*n the TEM images of the two high-power-tested devices, Devices 007 and 008 (not shown), that were both stressed at Condition 1, small pits have formed at the drain edge of the gate. Thus, current appears necessary to create the pits in the AlGaN layer.

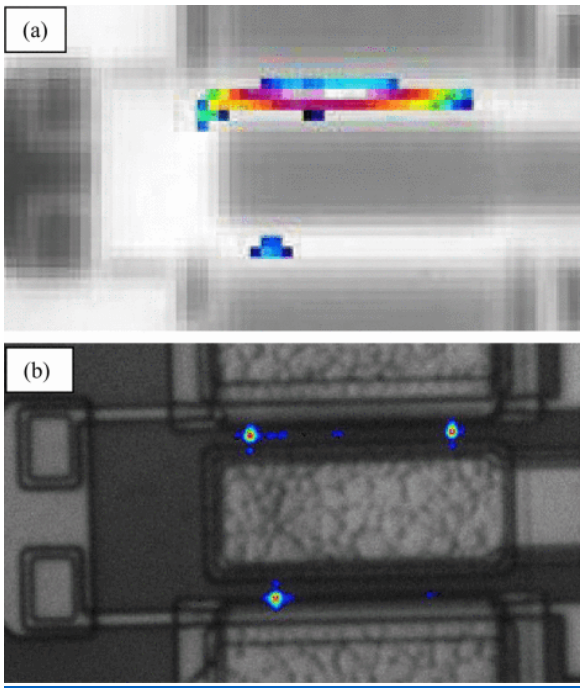

Figure 6. Device 007 (high-power-tested) at a baseplate of 85°C. The lower left spot was targeted for TEM imaging. (a) IR (radiance) image at 15X magnification. $V_{DS} = 28\text{V}, I_D = 10\text{mA}, V_{GS} = -1.69\text{V}, I_G = -3.3\mu\text{A}$, (b) PE image at 50X magnification. $V_{DS} = 10\text{V}, I_D = 3.2\text{mA}, V_{GS} = -1\text{V}, I_G$ in nA range.

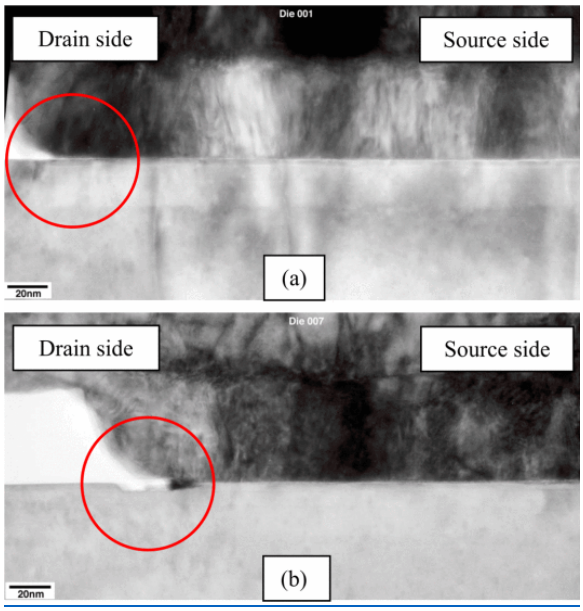

Figure 7. TEM images of (a) Device 001 (high-voltage-tested) and (b) Device 007 (high-power-tested). Notice absence of a pit or crack in Device 001 and the presence of a pit in Device 007.

SECTION IV. Conclusion

We have studied the degradation of AIGaN/GaN HEMTs subjected to the conditions of high dc power and high voltage with the gate pinched off. More degradation was generally observed due to the high-power conditions than to the highvoltage conditions. The degradation seen appears to be unrecoverable with rest. Severe drain current degradation due to high drain biases was not observed as has been reported elsewhere. Pits in the AIGaN layer on the drain side of the gate were observed in the high-power-tested devices. However, pits or cracks were not seen in the high-voltage-tested devices, which is contrary to published reports. Thus, electric

field alone does not appear to cause significant degradation, and current in conjunction with high electric fields seems to be required for pit or crack formation. Possible reasons for the differences between our and others' observations include material quality, fabrication processes, device structure, and bias conditions. The AlGaN/GaN HEMT structure studied herein is robust to high drain biases.

ACKNOWLEDGMENT

B.D.C. thanks the Air Force Research Laboratory High Reliability Electronics Virtual Center team for fruitful discussions, Steve Tetlak for TEM sample preparation, and Fred Shaapur for TEM imaging.

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