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Design and Analysis of Novel Ge-GeTe PN Junction for Photovoltaics

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***Abstract*—The continuing rise in demand for energy places a similarly increasing demand to improve power production methods and efficiency. In regards to solar power generation, one major limiting factor with existing photovoltaic (PV) systems is the management of heat produced and photon interactions with the PV device. Typical devices operate within the 300-1000 nm range of the solar spectrum, greatly limiting the range of photons used for power generation. Furthermore, since infrared light (>1200nm) incident upon Silicon PV devices are not utilized in electron-hole pair creation, the device temperature immediately increases during operation. Due to these factors, a novel approach was pursued to develop a more efficient single crystalline PV cell. Fabrication of the device began with an antimony (Sb) doped germanium (Ge) wafer, followed by a thin film (i.e. 200nm) of amorphous germanium telluride (a-GeTe) deposited using RF sputtering. Utilizing the chalcogenide phase change (PC) characteristics of a-GeTe, the wafer was transitioned at 400°C for the 200nm deposited film, crystallizing the a-GeTe forming crystalline germanium telluride (c-GeTe). The device was annealed at 650°C activating the junction. Initial results show promise and indicate methods in which improvements can be made. The goal of this study was to identify materials and processes available to develop a low band gap PV cell responsive light ranging from blue to near infra-red (NIR) region.**

***Index Terms*—germanium, germanium telluride, photovoltaics**

I. Introduction

Many great strides have been made in the solar industry in an effort to reduce dependence on fossil fuels. The most recent record setting efficiency of 46% under solar concentration, 29.8% under one sun [1] is just one stride in this effort. While achievements like this are phenomenal, they all tend to have one thing in common: they use silicon (Si) or gallium (Ga) based devices. Until recently little research has been published regarding the use of other bulk materials for use in solar cell fabrication.

The most recent non-organic, photovoltaic materials include: cadmium telluride (CdTe), bismuth telluride (BsTe), zinc telluride (ZnTe), perovskite ($CH_3NH_3PbI_3$), indium (In) and phosphorous (P)[2][3][4]. It is clear that great achievements have been made in these research endeavors where CdTe was boasted as the "basis for the market-leading thin-film solar-cell technology"[5]. While this trend continues to direct attention towards chalcogenide (ChG) based solar devices, little attention has been placed on the previous precursor to the semiconductor age, Ge.

One particular ChG consisting of Ge is germanium telluride (GeTe). GeTe has long since been studied for its unique amorphous-crystalline transitioning behavior with change in temperature. In earlier works it was observed that ratios of $Ge_{1-x}Te_x$ where x $\approx$ 0.5, exhibited p-type behavior [6]. It was also determined through X-ray spectroscopy that GeTe has a band gap of approximately 0.87 electron Volts (eV)[7]. The band gap is usually denoted by E_g, and is defined by difference in energy between the conduction and valence bands of the material[8]. The band gap is also referenced as the amount of energy necessary to excite an electron from a resting state in the material to the conduction band, where it can be extracted for use in electronic devices. Based on this gap value, GeTe should readily absorb photons from wavelengths zero to λ defined by:

$$E_g = \frac{hc}{\lambda} \rightarrow \lambda \approx \frac{1.23984193 \text{ eV}}{\text{Eg}} \approx 1.425\mu\text{m}, \quad (1)$$

where h is planks constant and c is the speed of light[9]. This indicates that GeTe and Ge junctions should perform slightly better than traditional Si devices. Since a PV device is essentially a PN - junction, the equations governing diode operations can be used to determine operation and predict performance. These can be used to predict efficiency and operating characteristics. When characterizing a device, three main values of concern are the open circuit voltage (V_{oc}), short circuit current (I_{sc}) and the fill factor (FF) which is a measure of the operating capacity of a device. From [8] the FF is:

$$FF = \frac{V_{mp}I_{mp}}{V_{oc}I_{sc}}, \quad (2)$$

where V_{mp} and I_{mp} are the optimum operating values for the solar cell. Also from [8], Eqns. 3 - 5 describe the theoretical values of V_{oc} and I_{sc}:

$$V_{oc} = \frac{kT}{q} ln(\frac{I_{sc}}{I_{01}} + 1) = \frac{kT}{q} ln(\frac{N_A N_D}{n_i^2}), \quad (3)$$

$$I_{sc} = I_{01}[exp(\frac{qV_{oc}}{kT}) - 1], \quad (4)$$

$$I_{01} = qn_i^2 A_j (\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}). \quad (5)$$

[1]*Disclaimer:* The views expressed in this paper are those of the author, and do not reflect the official policy or position of the United States Air Force, Department of Defense, or the U.S. Government.

In these equations, k is the boltzmann constant, T is the temperature, I_{01} is the reverse saturation or dark current, q is the electron charge in Coulombs, n_i is the intrinsic carrier concentration of the material, A_j is the 2-dimensional area of the junction, D_p and D_n are the diffusion velocities of the dopants, L_p and L_n are diffusion lengths and N_A and N_D are the dopant concentrations. In applying these concepts, this work demonstrates a functional PV device using n-Type Ge (n-Ge) and GeTe.

II. Methodology

The first step to form a PN-Junction with GeTe and n-Ge, was to deposit GeTe on a prepared n-Ge wafer. To get the materials to interact and form ionic bonds, GeTe had to be properly crystallized. The process used to form this crystallization was based on findings by Betts *et al.* in which it was determined that the bonding between GeTe and another material was more covalent in the amorphous than in the crystalline state [10]. In order to test this, two samples were selected, 1A and 1B. Both samples consisted of Sb doped Germanium with $\approx$ 200nm of $Ge_{0.5}Te_{0.5}$ which were deposited using the Discovery 18 plasma sputtering system. Sample 1A was heated to 400°C for 30 minutes in atmosphere to crystallize the GeTe. According to studies accomplished by individuals at Samsung Electronics Co. Ltd., this temperature successfully converted amorphous GeTe to cubic crystalline GeTe with minimal material losses or oxidization[11]. Sample 1B was not heated significantly until the annealing process.

In samples 1A & 1B an anti-reflective coating (ARC) was applied before the formation of the contacts in order to attempt to eliminate some processing steps. However, the temperature ranges proved to be too great and another sample 2A was created in the same fashion as 1A in order to properly test the junction formation. Initial band structure calculations predicted that the open circuit voltage could be quite low. In order to counteract this, two samples were created with an inter-facial layer between the n-Ge wafer and GeTe layer. Therefore, Samples 3A and 3B were fabricated with such a layer consisting of Al_2O_3. From Eqns. 3 and 5, the choice to add an inter-facial layer instead of another method was favored as an increase in the area of the diffusion region combined with an increase the band separation was the best method based on the equations derived.

Samples 1-3 had the exposed side of the wafer as the polished side which raised a concern regarding the reflectivity of the exposed surface, in this case GeTe. If it was, then it would act to reflect energy which might otherwise be utilized. In order to investigate this, samples 4A and 4B were created in the same manner as sample 3A. For these samples, the GeTe layer was on bottom and the n-Ge layer was the exposed layer.

The crystallization of GeTe for all samples, was confirmed using a JANDEL four-point probe to determine sheet resistances. Since GeTe has a higher sheet resistance in its amorphous state than its crystalline state[12], this was deemed a reliable method to determine crystalline state of the samples. Reflectance and transmittance tests were also accomplished following crystallization on samples 2A, 3A, 3B and 4A using the Filmetrics spectrometer, shown in Figs. 3,5,7 and 9 respectively. Following these tests, all samples had front and back contact metals applied. After this, all samples were annealed for 20 seconds at 650°C using the Solaris 150 rapid thermal processing system (RTA). This process not only set the contacts but also allowed for formation of the junction.

Formation of an ohmic metal contact to n-Ge has been proven to be a challenge in prior studies. However, research completed by Yoshitake *et al.* [13], Nishimura *et al.*[14], Dimoulas *et al.*[15] and Dumas *et al.*[16] as well as research completed locally at the Air Force Institute of Technology (AFIT), demonstrated that the use of a tunnel junction and fermi-level pinning were able to make an ohmic contact to the n-Ge surface. Since GeTe is a p-type material, gold was used to form contacts with GeTe surfaces.

Testing of all samples was accomplished during each applicable stage of processing to monitor the impact steps had on junction formation. The tests consisted of electrical characterization using an Alessi (REL-6100) parameter analyzer and the Solar Light (16S-300) solar simulator. Diode tests were performed on the Alessi using -5 to +5 volts with a current cut off of 100 mA due to system limitations of the parameter analyzer. The V_{oc} and I_{sc} values were obtained on the solar simulator at 1.5 ATM, 25°C and $1000\frac{W}{m^2}$ test conditions. Reflectance of each sample was measured by counting the light packets reflected over a period of 40ms. The tester limitations are 200-1100nm and 0-4000 counts for wavelength and number of packets returned, respectively.

III. Results

All solar simulation results are shown in Tab. I. Diode testing results for all samples are shown in Figs. 2 - 8. Samples 1A,1B and 2A consist of only GeTe and n-Ge and as shown, had highly diode-like behavior. Samples 3A and 3B had partial diode behavior, with a greater current density, however the negative effects of the inter-facial layer appear to negate the junction formation. Samples 4A and 4B appeared to have the best of all the samples in regards to solar test data. Sample 3A had the best performance in regards to the diode test characteristics as shown on Fig. 4.

Sheet resistance measurements of c-GeTe, a-GeTe and n-Ge were taken on a four point probe resulting in Ω-cm values of 0.5346, $3.83\text{x}10^3$ and 0.1212 respectively. Using the approximation for sheet resistance, from [8]:

$$\rho \approx \frac{1}{q\mu \mathrm{N}} \tag{6}$$

and inserting the measured values for ρ, solving for N yields the approximate dopant concentrations to be: $6.16x10^{15}cm^{-3}$, $85.9x10^{9}cm^{-3}$ and $13.3x10^{15}cm^{-3}$ respectively. Using these values with Eqn. 3 the expected values for V_{oc} ranged between 17 mV to 300 mV, which were consistent with the values obtained in Tab. I. Negative values indicate a reverse polarity of the junction during test.

As shown in Figs. 3, 5, 7 and 9 for samples 2A, 3A, 3B and 4A respectively, this device has high reflectivity, suggesting improved performance could be achieved by utilizing an ARC coating. With the high reflectivity count measured, compared to a commercial device (Fig. 10), applying an appropriate ARC is expected to lead to a significant improvement in efficiency. All n-Ge/GeTe samples showed high reflectance in the visible range and high energy wavelengths which indicated a great deal of potential power was lost due to high reflectivity.

A. Sample Run 1

During processing of samples 1A/B, an ARC layer was added before contact formation which prevented most in line testing. The annealing temperature was also too high for the ARC resulting in virtually no contacts available for testing. Because of this, the results for 1A/B were believed to be misleadingly low, which prompted sample run 2. Samples 1A/B were the only samples crystallized in atmosphere and had the worst contacts due to the ARC step during fabrication. Regardless of the state of the junction, this sample run indicated that it was possible to form a PN-junction using GeTe and n-Ge which led to continued tests.

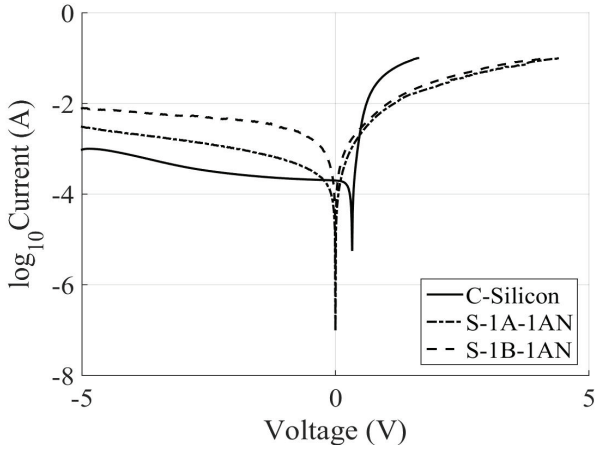

Fig. 1. Sample 1A diode test data semi-log plot, compared to commercially available silicon solar cell. Low difference in measured current from positive and negative voltages.

B. Sample Run 2

The formation of a junction was confirmed with this test run. The formation of the junction appeared to have mostly formed during the annealing step with slight formation starting during the crystallization step. Due to sample 1B crystallizing during the ARC application in vacuum and the fact that it had better test results than 1A, sample 2 was also crystallized in vacuum. This appeared to help reduce oxygen contamination during crystallization, coinciding with findings by Kim *et al.* [11]. At the final stage of fabrication, pitting was noticed on the metal contacts which was attributed to the annealing step as normal.

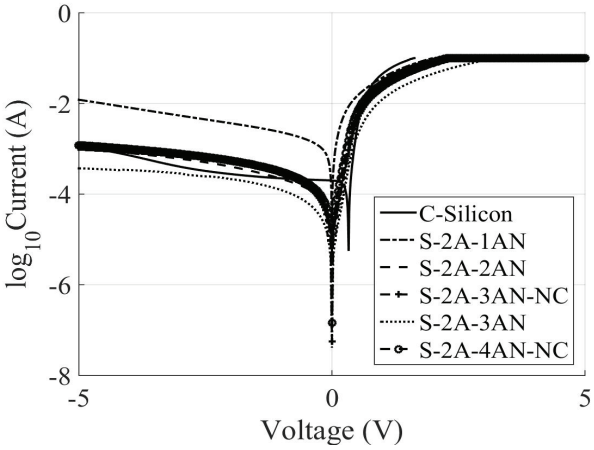

Fig. 2. Sample 2A diode test data semi-log plot, compared to commercially available silicon solar cell. Much higher current difference with increasing voltage indicating diode like behavior.

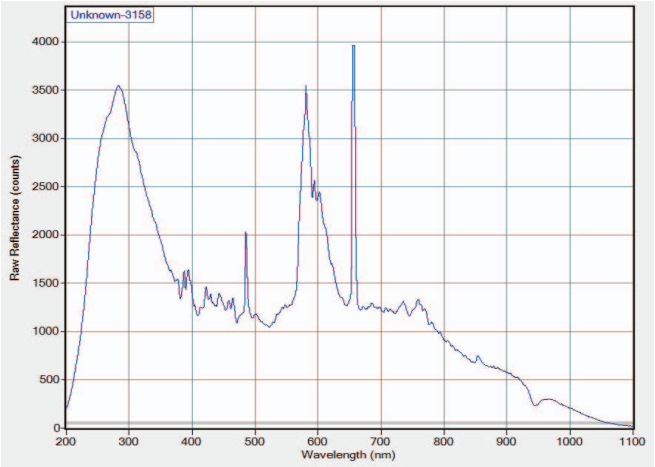

Fig. 3. Sample 2A Reflectance Response, showing high reflectivity at <400nm and in the visible light spectrum.

C. Sample Run 3

Due to the low open circuit voltage from sample 2A, the introduction of an inter-facial Al_2O_3 layer between n-Ge and GeTe was implemented in order to increase this voltage. Sample 3A had a 3nm layer, while 3B had 5nm in order to assess the affect of the layer thickness on the voltage

performance. The results in Tab. I show that the intent of the layer was achieved as the V_{oc} measurements for this sample were greatest. The thicker layer on 3B had worse performance leaving the conclusion that 3nm or less is an ideal thickness for an Al_2O_3 inter-facial layer. Both 3A and 3B also had pitting on the contacts attributed to the RTA process. Given the low breakdown voltage observed in these sample tests, it was believed that the RTA process may be too aggressive and later tests may prove more successful at lower temperatures and/or shorter duration.

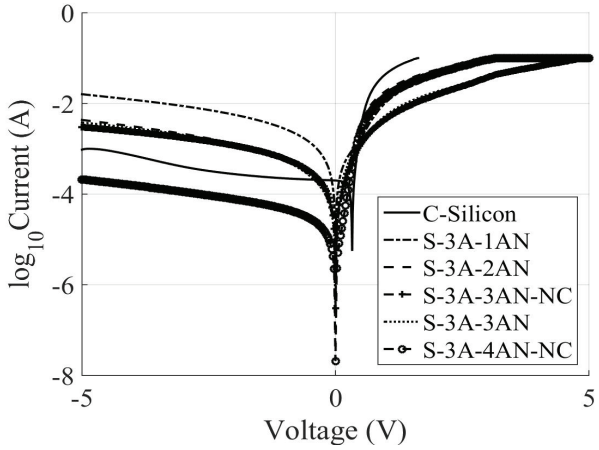

Fig. 4. Sample 3A diode test data semi-log plot, compared to commercially available silicon solar cell. Slightly higher current difference with increasing voltage than the values indicated in Fig. 2.

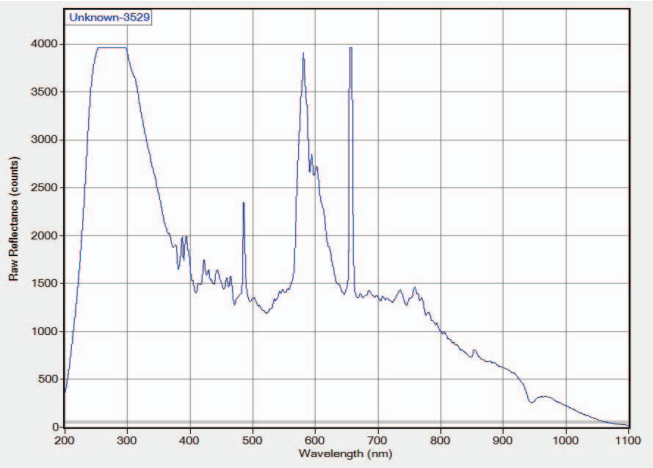

Fig. 5. Sample 3A Reflectance Response, showing high reflectivity at <400nm and in the visible light spectrum. Slightly more reflective in the same regions than Fig. 3 possibly due to inter-facial layer.

D. Sample Run 4

During the testing of sample run 3, it was observed that the unpolished side performed better than the polished side of the sample. In order to see if any improvement could be gained by changing the orientation of the contacts, these

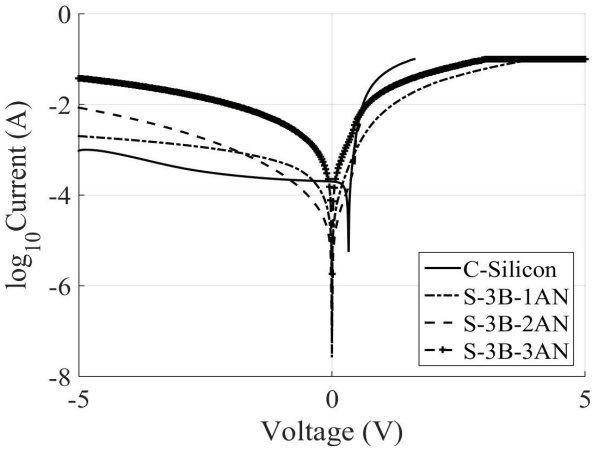

Fig. 6. Sample 3B diode test data semi-log plot, compared to commercially available silicon solar cell. Much lower current difference with increasing voltage than the values indicated in Fig. 4. Indicating weaker junction formation due to larger inter-facial layer.

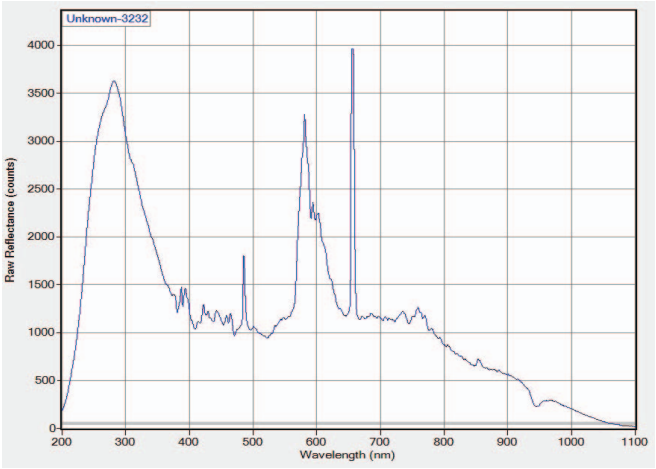

Fig. 7. Sample 3B Reflectance Response, showing high reflectivity at <400nm and in the visible light spectrum similar to that of Fig. 3.

samples were created. Sample 4B was a full 2 inch germanium wafer while 4A was a small sample. Both sample 4A and 4B had very similar voltage responses and only sample 4A is presented graphically. As shown in Tab. I the V_{oc} and I_{sc} were not greatly affected by this configuration in comparison to previous samples. The larger sample had a greater current as shown in Tab. I due to its greater surface area. The greater impact seen with this configuration was with the diode response, shown in Fig. 8. These samples had a much sharper rise in current under forward bias and at a much lower voltage than that of a commercial silicon PV cell. This unfortunately also indicated a low breakdown voltage which only worsened with longer annealing times, further indicating that the RTA selected is too high or long for the Al_2O_3 layer.

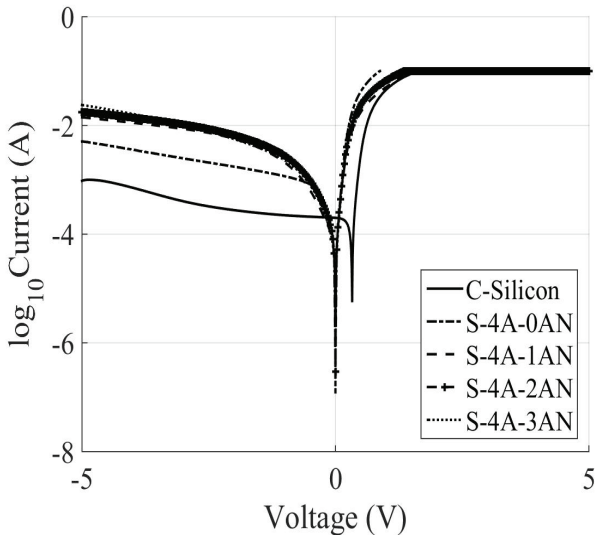

Fig. 8. Sample 4A diode test data on parameter analyzer, compared to commercially available silicon solar cell

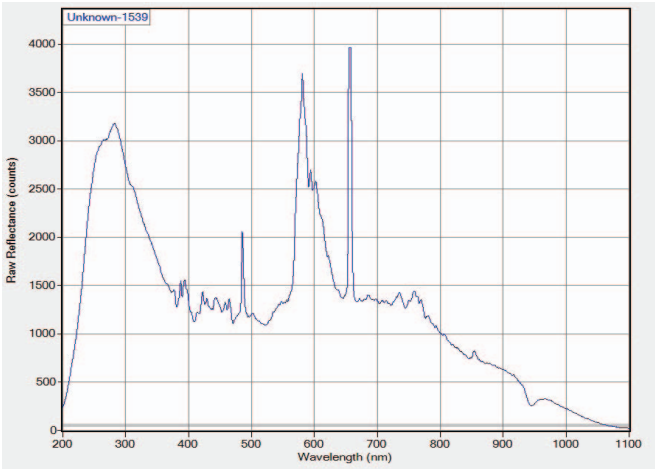

Fig. 9. Sample 4A Reflectance Response, showing high reflectivity at <400nm and in the visible light spectrum similar to ,but slightly better than ,that of Fig. 3. This indicates that the improvement in V_{oc} comes from the lower reflectance of the unpolished surface.

Sample ID (side facing up)	Voc (mV)	Isc (mA)
1A (P)	-1.45	-0.0053
1B (P)	-9.1	0.0168
2A (P)	10.3	0.0131
3A (P)	-1.6	0.0043
3B (P)	-1.28	-0.0033
4A (U)	63.7	0.154
4B (U)	60	0.25
1A (U)	2.23	0.0083
1B (U)	6.2	0.0229
2A (U)	45.8	0.1334
3A (U)	85.3	0.3199
3B (U)	68.6	0.3283
4A (P)	-1.7	-0.002
4B (P)	-1.95	-0.007
P - Polished; U - UnPolished		

TABLE I
MEASURED V_{oc} AND I_{sc} FOR SAMPLES TESTED ON SOLAR SIMULATOR UNDER STANDARD TEST CONDITIONS.

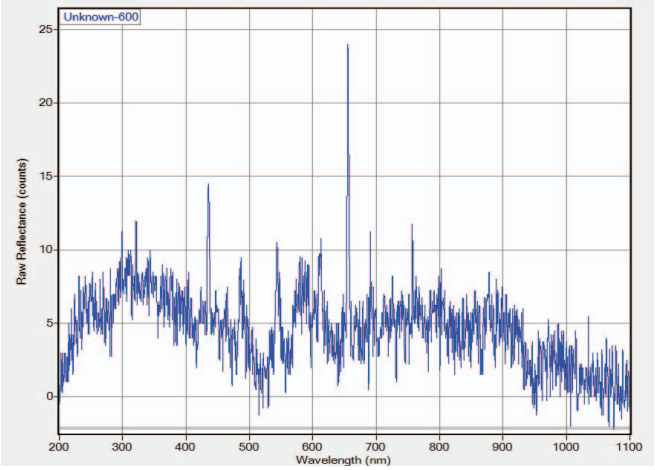

Fig. 10. Commercial Silicon PV Cell with appropriate ARC indicating low reflectance from 0-1100nm.

IV. CONCLUSION

In this work, the formation of a functioning PN junction using n-Ge and GeTe was demonstrated. A best recorded total power of 27μW with a FF of 21.42% was measured. Further investigations into junction configurations would improve short circuit current and open circuit voltages. The limiting factor for power generation in this n-Ge/GeTe structure was the open circuit voltage. Based on band theory and semiconductor physics calculations this appeared to be due to a low difference between Ge and GeTe conduction band energy levels [7],[8]. Increasing the difference in these energies would improve the overall power generation of a Ge/GeTe PV device.

Furthermore, application of an appropriate ARC would improve response since it was observed that GeTe is highly reflective at higher energy wavelengths. Reducing the reflectivity by using the unpolished side of the wafer as the exposed side in sample run 4 did improve the open circuit voltage measured. With an appropriately designed ARC, the small effects observed here would be much more significant.

One fabrication issue was noted in conjunction with long periods of time between tests on the solar simulator. Between tests, an oxide layer formed on the aluminum contacts causing lower readings during consecutive solar simulator tests. Because of this, a thin layer (100-200Å) of gold should be used as a capping layer to prevent oxidation of aluminum contacts for future fabrications.

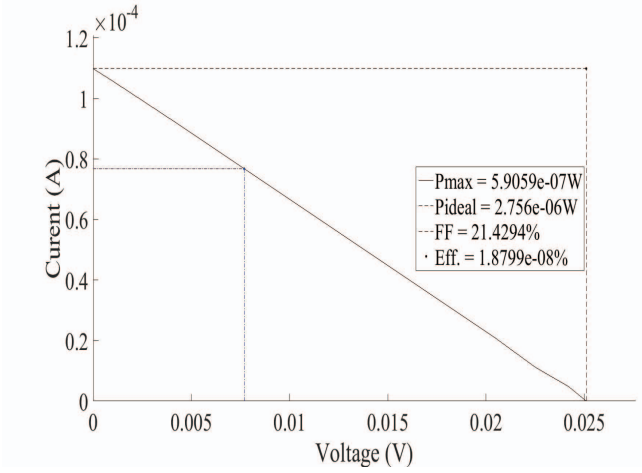

Fig. 11. IV plot of sample 4A measured over load resistances of: 10, 50, 100, 1000, 2000 and 5000 ohms. Calculated maximum power, optimum power out put at FF and cell efficiency percentage are displayed in the inset.

Introduction of the inter-facial layer did improve performance but placed greater limitations on the RTA process. It was also noticed that applying this layer required greater precision as a thickness of only a couple nanometers caused a large change in performance.

V. Acknowledgments

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