

# Low-Cost, Water Pressure Sensing and Leakage Detection Using Micromachined Membranes

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LOW-COST, WATER PRESSURE SENSING AND LEAKAGE DETECTION  
USING MICROMACHINED MEMBRANES

by

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ABSTRACT

LOW-COST, WATER PRESSURE SENSING AND LEAKAGE  
DETECTION USING MICROMACHINED MEMBRANES

Farhana Anwar

Marquette University, 2019

This work presents the only known SOI membrane approach, using Microelectromechanical systems (MEMS) fabrication techniques, to address viable water leakage sensing requirements at low cost. In this research, membrane thickness and diameter are used in concert to target specific stiffness values that will result in targeted operational pressure ranges of approximately 0-120 psi. A MEMS membrane device constructed using silicon-on-insulator (SOI) wafers, has been tested and packaged for the water environment. MEMS membrane arrays will be used to determine operational pressure range by bursting.

Two applications of these SOI membranes in aqueous environment are investigated in this research. The first one is water pressure sensing. We demonstrate that robustness of these membranes depends on their thickness and surface area. Their mechanical strength and robustness against applied pressure are determined using Finite Element Analysis (FEA). The mechanical response of a membrane pressure sensor is determined by physical factors such as surface area, thickness and material properties.

The second application of this device is water leak detection. In devices such as pressure sensors, microvalves and micropumps, membranes can be subjected to immense pressure that causes them to fail or burst. However, this event can be used to indicate the precise pressure level that malfunction occurred. These membrane arrays can be used to determine pressure values by bursting.

We discuss the background information related to the proposed device: MEMS fabrication processes (especially related to proposed device), common MEMS materials, general micromachining process steps, packaging and wire bonding techniques, and common micromachined pressure sensors. Besides, FEA on SOLIDWORKS simulation module is utilized to understand membrane sensitivity and robustness. In addition, we focus on theories supporting the simulated results. We also discuss the device fabrication process, which consists

of the tested device's fabrication process, Deep Reactive Ion Etching (DRIE) for membrane formation, two different realizable fabrication technique (depending on sensing material) of sensing element, metal contact pads, and connectors deposition. In addition, a brief description and operation procedures of the device fabrication tools are provided as well. We also include detailed electrical and mechanical testing procedures and the collected data.

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# Low-Cost, Water Pressure Sensing and Leakage Detection Using Micromachined Membranes

## I. Introduction

Microelectromechanical Systems (MEMS) membranes are widely used in various applications ranging from stiffness tuning to gas pressure sensing. Superior properties such as higher sensitivity of MEMS membranes can be utilized in water-related applications [1,2]. However, lack of reliable processing, testing procedure and packaging methods leads to electrical and mechanical failures and thereby restrict their progress in water applications. In this research, membrane thickness and diameter are used in concert to target specific stiffness values that will result in targeted operational pressure ranges of approximately 0-120 psi. A MEMS membrane device constructed using silicon-on-insulator (SOI) wafers, has been tested and packaged for the water environment. Microelectromechanical systems (MEMS) membrane arrays will be used to determine operational pressure range by bursting.

Two applications of these SOI membranes in aqueous environment are investigated in this research. The first one is water pressure sensing. We demonstrated that robustness of these membranes depends on their thickness and surface area. Their mechanical strength and robustness against applied pressure were observed with Finite Element Analysis (FEA). The mechanical response of a membrane pressure sensor is determined by physical factors such as surface area, thickness and material properties (e.g. Elastic modulus and Poisson's ratio). This is the only known SOI membrane approach, using MEMS fabrication techniques, to meet a low-cost water pressure sensing requirement.

Another application of this device is water leak detection. Devices such as pressure sensors, microvalves, and micropumps, membranes can be subjected to immense pressure that causes them to fail or burst [3]. Once the membrane bursts, the device will stop functioning. However, this event can be used to indicate the precise pressure level that malfunction occurred. These microelectromechanical systems (MEMS) membrane arrays can be used to determine pressure values by bursting. The failure event can be used to detect leakages in household appliances, ranging from automatic sinks to dishwashers.

The next chapter discusses about background information related to the proposed device like MEMS fabrication processes (especially related to proposed device), common MEMS materials, general micromachining process steps,

packaging and wire bonding techniques, and common micromachined pressure sensors. Chapter III is on analytic models and simulations that were used to develop the initial designs. Finite Element Analysis (FEA) and SOLIDWORKS simulation module is discussed briefly. Material properties (i.e. Si, SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, Au) used for the simulations were also studied. This chapter also focused on theories supporting the simulated results. Chapter IV is based on the device fabrication process. It consists of the tested device's fabrication process, Deep Reactive Ion Etching (DRIE) for membrane formation, two different realizable fabrication technique (depending on sensing material) of sensing element, metal contact pads and connectors deposition. Mask set designs for each fabrication step is given here. Besides, brief description and operation procedures of the device fabrication tools are provided here. Chapter V includes testing procedures and results. Detailed electrical and mechanical testing procedures and collected data are discussed here. Lastly, conclusion and future works by modifying the MEMS membrane device are discussed in chapter VI.

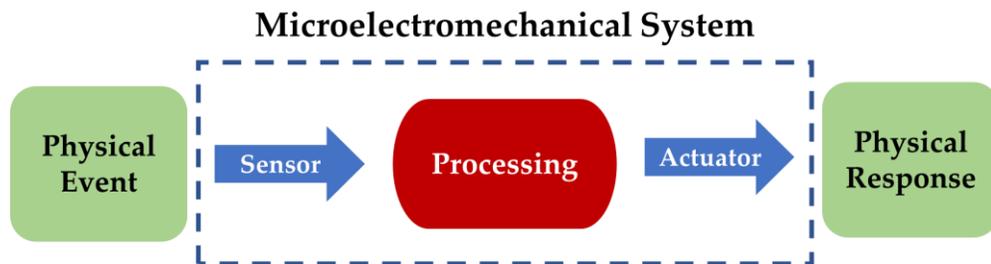
## II. Background

This chapter provides background information about common pressure sensors, sensing materials, MEMS fabrication processes, packaging and wire bonding techniques. Piezoresistive and Piezoelectric material properties are described. Micromachining technologies are discussed. Apart from these, common MEMS fabrication processes relevant to the proposed device like diffusion, oxidation, implantation, photolithography, etching, lift-off, deposition etc. are also described in a brief.

### 2.1 MEMS

MEMS are sub-millimeter to centimeter sized mechanical systems with individual features of a few micrometers or less fabricated utilizing microfabrication techniques. MEMS devices are categorized depending on their complexity, ranging from simple structure with no moving component to complex structure with several moving parts. Microelectromechanical Systems (MEMS) is the amalgamation of mechanical elements, sensors, actuators and electronics on a

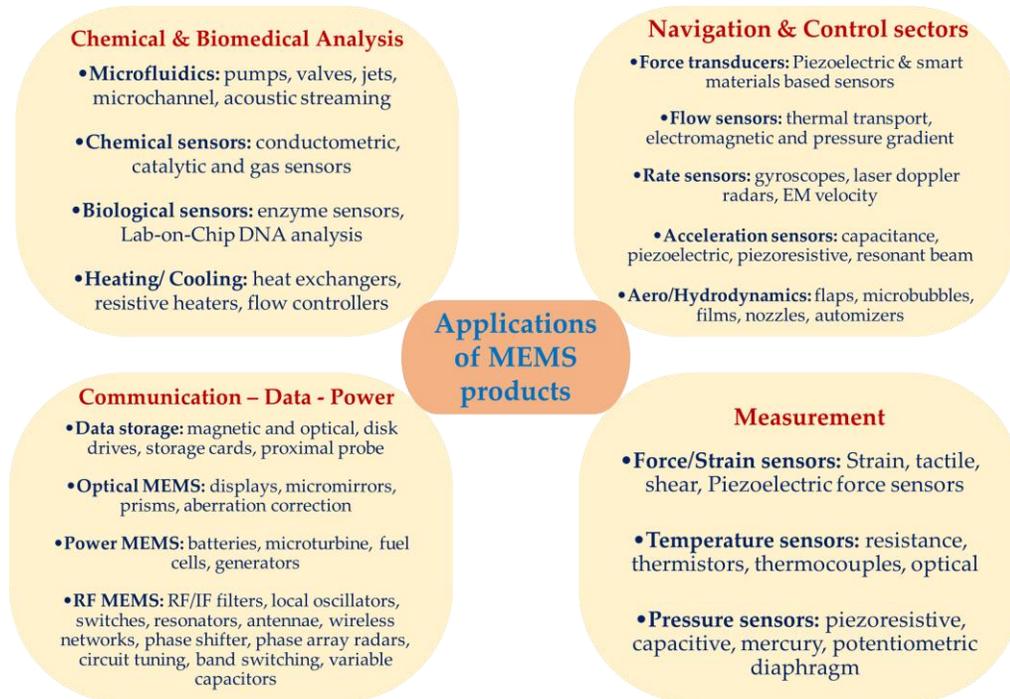
common substrate [4]. Among these, microsensors and microactuators are most interesting as their combination with Integrated Circuits completes a loop allowing completely interactive systems (Figure 1). Sensors and actuators are considered as transducers because they convert energy from one form to another.



**Figure 1.** Schematic illustration of interaction between MEMS components.

MEMS is an enabling technology. Micro-sensors and actuators are not counted as products by themselves, but they can be integrated as components in products. MEMS products are in widespread use and often referred to as solid state sensors and actuators, or solid-state transducers. There are numerous possible applications of MEMS devices in biomedical, automotive, industrial and military sectors [5]. The MEMS pressure sensors and Lab-On-Chip have widespread application in medical sector. RF-MEMS are exploited in high frequency communication circuits as they can improve circuit performance, while reducing the total circuit area, power consumption and cost [6]. MEMS gyroscopes

and accelerometers are vastly used in automobile industries. Figure 2 illustrates some common application fields of MEMS devices.

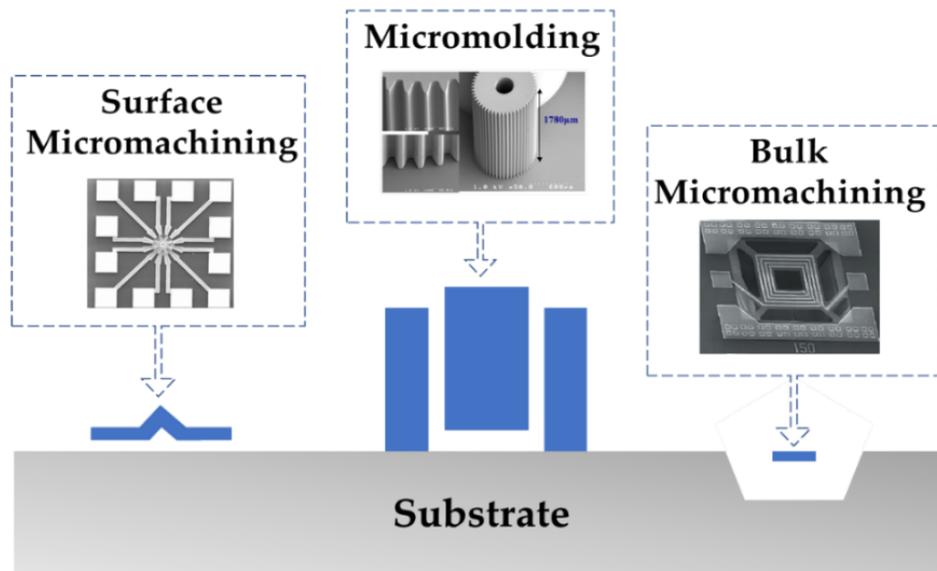


**Figure 2.** Typical Applications of real MEMS devices.

## 2.2 Micromachining Processes

MEMS is an engineering discipline that studies the design and fabrication of micrometer to centimeter scale mechanical systems [7]. MEMS fabrication is commonly referred to as micromachining. Micromachining consists of four separate areas: Substrates and Dopants – Starting point, Patterning – Lithography,

Additive Processes – Deposition, Subtractive Process – Etching. There are three types of specialized MEMS fabrication processes. These are: Surface Micromachining, Bulk Micromachining, and Micromolding. Figure 3 illustrates cross sectional views of MEMS devices fabricated on a substrate exploiting these micromachining processes.



**Figure 3.** Basic micromachining Processes.

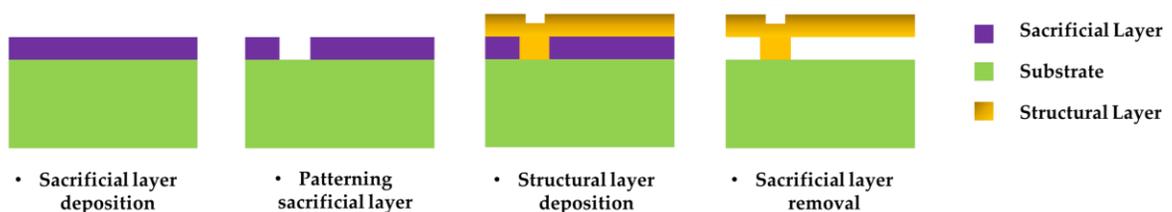
### **Surface Micromachining**

Surface Micromachining is the process of constructing movable structures onto non-movable platforms, then etching away the platform material. It is an additive process as multiple layers are formed upon the surface of a substrate [8]. The process varies depending on the platform materials and etchants. Table I shows common structural layer-sacrificial layer pairs for surface micromachining.

TABLE I  
COMMON STRUCTURAL LAYER-SACRIFICIAL LAYER PAIRS

Structural Layer	Sacrificial Layer
Si <sub>3</sub> N <sub>4</sub>	SiO <sub>2</sub> , Photoresist
Al, SiO <sub>2</sub>	Polysilicon
Polysilicon	SiO <sub>2</sub>
Al	Photoresist
Polyimide	Al

In surface micromachining process, multiple thin layers (<50 $\mu$ m) are formed on a specific side of wafer. At first, a sacrificial layer is deposited by physical or chemical vapor deposition technique on the substrate's surface. A photoresist layer is deposited and exposed to transfer pattern. The photoresist layer is developed to etch out the sacrificial layer from the places where the polysilicon layer will be deposited to form the movable part. Then, the structural polysilicon material was deposited by CVD or sputtering – PVD [9]. Dopants are introduced by ion implantation for making the structure conductive. The structural layer undergoes patterning by Reactive Ion Etching (RIE) and hardening. After that, structure is released by eliminating the sacrificial layer by exploiting selective etching (Figure 4).



**Figure 4.** Basic steps of surface micromachining.

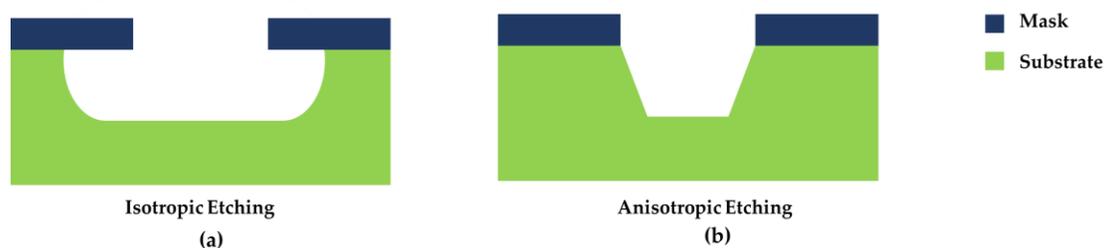
One of the main reasons behind the surface micromachining's popularity is that it allows precise dimensional control in the vertical direction. Also, it is compatible with CMOS and single-sided wafer processing. Moreover, it ensures small and low-cost devices [8-10].

However, there are some drawbacks of this process. The mechanical properties of deposited thin-films are generally unknown, making the mechanical properties difficult to reproduce. Thus, they must be measured beforehand. Besides, thin structural layer films experience high residual stress; resulting film cracking, delamination and void formation. Therefore, annealing should be done frequently to diminish this residual stress. Structural layers often suffer from stiction. This stiction may be related to hydrogen bonding, Residual contamination and Vander Waal's forces. An anti-stiction coating material or stand-off bumps on the underside of the structural layer help to avoid stiction [9,11].

**Bulk Micromachining:**

This is the oldest micromachining technology. Usually diaphragms, cavities, and cantilevers are fabricated utilizing this method. This technique is a subtractive process as it involves the selective removal of the substrate material [10-6]. There

are various ways to remove the substrate material. Among these, anisotropic/ dry etching and isotropic/ wet etching are the most common. In isotropic etching, substrate material is etched out in all directions at an equal rate. This process undercuts the mask material (Figure 5(a)). Hydrofluoric acid (HF) is commonly used to etch silicon dioxide. Isotropic etching is much faster than anisotropic etching. The etch rate depends on etchant's concentration and agitation grade [12]. On the other hand, etchants for anisotropic etching etches different crystallographic planes at different rates (Figure 5(b)). For example, etch selectivity between the Si (100), (110), and (111) planes for KOH etchant is 100:16:1. In silicon, the (111) plane has more bonds per area than the (110) plane or the (100) plane. As a result, etch rate is slowest in Si (111) plane. Common etchants for anisotropic etching processes are: Potassium hydroxide (KOH)/ H<sub>2</sub>O solutions, ethylene diamine pyrocatechol (EDP), tetramethyl ammonium hydroxide (TMAH) and hydrazine. Here, KOH is the most popular etchant.

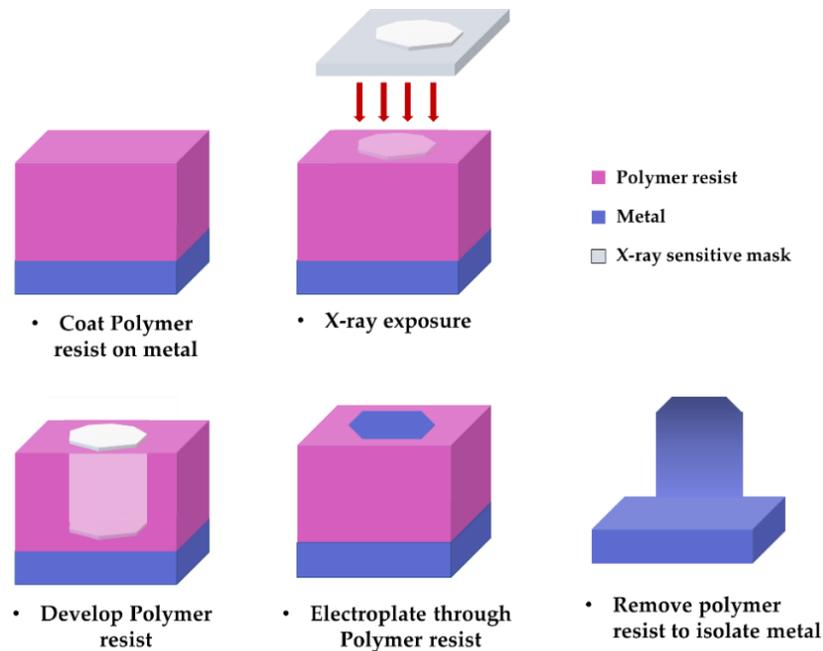


**Figure 5.** Bulk Micromachining, (a) Isotropic etching; (b) Anisotropic etching.

Appropriate protection of the wafer's backside is essential for both isotropic and anisotropic etching. For this, a special holder can be used for preventing the backside liquid from liquid exposure. Otherwise, the backside should be coated with a chemical protection layer [13].

### **Micromolding**

Micromolding/ Microforming/ Lithographie, Galvanoformung and Adformung (LIGA) is another specialized micromachining process. By applying this process, it is possible to form microstructures having 100:1 aspect ratio and 90° angled sidewalls [14]. Unlike the previous two processes, this is a non-silicon process and needs synchrotron generated x-ray radiation. LIGA is a hybrid fabrication technique incorporating lithography, electroplating and molding. LIGA Technology can be categorized into two major types: X-ray LIGA and Extreme Ultraviolet (EUV) LIGA. In X-ray LIGA process, at first an x-ray sensitive photoresist coated onto the substrate. Then, an x-ray mask is used to selectively expose the resist. X-ray breaks the polymer chain of exposed regions and then the exposed resist is developed away. Figure 6 illustrates the steps involved in X-ray LIGA process.



**Figure 6.** Primary steps involved in the X-ray LIGA process.

The prime advantages of this process are: high aspect ratio, large structural height and sidewall properties. Micromolding is comparatively expensive and slower than the other two processes as it involves unique X-ray mask and x-ray source. The fabricated metal parts are often reused for making polymer molds to eradicate the necessity of an x-ray radiation source for reproducing the same parts [9].

## 2.3 MEMS Materials

This section covers the common materials used for MEMS device fabrication. Short description of typical Si based MEMS materials and other materials for substrate, structural and sacrificial layers are given here.

### *2.3.1 Common Substrate Materials for Micromachining*

In microelectronics, substrate is defined as a flat macroscopic body on which microfabrication processes take place [Ruska, 1987]. Primary Micromachining Substrates can be divided into three groups: (1) Elemental Semiconductors (Group IV) (i.e. Silicon, Germanium), (2) Compound Semiconductors (III-V) (i.e. Gallium Arsenide, Gallium Nitride, Indium Phosphide), and (3) Non-Semiconductor Substrates (i.e. Quartz).

#### **Silicon (Si)**

Silicon is the most popular substrate for MEMS processes as it is abundant on earth. Usually, it exists as compound material with other elements. However, Single-crystal silicon is vastly used as substrate material for MEMS product fabrication. In MEMS products, Si can be found in various forms like single crystal

substrate (SC-Si), amorphous thin film (a-Si), polycrystalline thin, film (Poly-Si), and single crystalline thin film. There are several reasons behind its unmatched popularity in MEMS field. Silicon crystal structure can be considered as an ideal structure. Even though its Young's modulus is similar to steel ( $\sim 188_{(111)}$  GPa), but its density is as low as aluminum ( $\sim 2.32$  g/cm<sup>3</sup>). Its melting point (1400°C) is almost double than aluminum's (Al). melting point. Therefore, Si remains in shape even at high temperature. Besides, silicon maintains its elastic strength at high temperatures ( $< 600^\circ\text{C}$ ) without showing any significant plastic deformation. Silicon shows almost zero mechanical hysteresis, which makes it an ideal material for transducers. Furthermore, it has a native oxide (SiO<sub>2</sub>) with good electrical properties [15,16].

### **Germanium (Ge)**

Like Si, Ge also has the diamond cubic crystal structure. They share similar properties due to their position in periodic table of the elements. Ge has lower values for the Young's modulus ( $\sim 155_{(111)}$  GPa), fracture strength ( $\sim 2.2_{(\text{poly})}$  GPa), melting point (938°C) and mechanical quality factor compared to Si. Yet, Ge still shows better performance in MEMS processes than aluminum (Al) [17].

### **Gallium Arsenide (GaAs)**

Gallium arsenide (GaAs) is a compound semiconductor which has same numbers of gallium and arsenic atoms in its unit cell. It is a highly used material for photonic devices as its electron mobility ( $0.85 \text{ m}^2/\text{Vs}$ ) is almost six times higher than Si ( $0.145 \text{ m}^2/\text{Vs}$ ). Moreover, it has excellent thermal insulation property and superior dimensional stability at high temperature. Unlike Si, it has piezoelectric property ( $2.6 \text{ pN}/^\circ\text{C}$ ). However, its hardness ( $7 \text{ GPa}$ ) and fracture strength ( $2.7 \text{ GPa}$ ) is lower compared to Si. Its yield strength ( $2700 \text{ MPa}$ ) is three times lower than Si. Therefore, it is very brittle and not good enough for micromachining like Si. The major drawbacks are its high cost, fragility and processing difficulty [15,18].

### **Gallium Nitride (GaN)**

Even though GaN's properties are compatible with MEMS processes, it is not as common as the previous materials in MEMS sector. Gallium nitride exhibits superior mechanical and thermal stability along with inherent semiconducting-piezoelectric property. The main weakness of GaN in aqueous environmental applications is that it dissociates to gallium oxide and nitrogen at around  $650 \text{ }^\circ\text{C}$  in as oxygen is present [19,20].

## Quartz

Quartz is a compound of  $\text{SiO}_2$  and it is inexpensive. Its unit cell is tetrahedron shaped. It is almost an ideal material for MEMS transducers as it shows close to absolute thermal dimensional stability. At high temperatures, quartz exhibits higher dimensional stability than silicon. Even though it is difficult to machine quartz, it offers more flexibility in geometry than Si.

### *2.3.2 Common Isolation and Sacrificial Layer Materials for Micromachining*

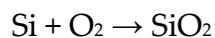
Dielectric materials are commonly used as electrical and thermal insulators in MEMS devices. In surface micromachining process, sacrificial layers are used for constructing movable parts. Etchant selectivity of structural and sacrificial layer should be high, and the sacrificial material must be compatible to the substrate material and fabrication process. As discussed before, this layer is selectively etched out after forming the desired movable part. Another interesting topic regarding MEMS fabrication process is masking. Masking is the process of protecting the substrate material from a following etch process. Sometimes direct deposition causes high stress between two materials, leading to device failure. In such situation, an isolation layer can help to passivate surface stress. For example, Direct  $\text{Si}_3\text{N}_4$  deposition on Si can produce high stress at the interface. In this case,

$\text{Si}_3\text{N}_4/\text{SiO}_2/\text{Si}$  stacks can allow good surface passivation.  $\text{Si}_3\text{N}_4/\text{SiO}_2/\text{Si}$  stacks shows improved thermal stability due to hydrogen in the nitride layer, in the form of N-H and Si-H bonds. Here  $\text{SiO}_2$  acted as screening/ isolation/ masking layer.  $\text{SiO}_2$  and  $\text{Si}_x\text{N}_x$  are common masking material. For masking, a thin masking layer is deposited onto the substrate. While choosing masking material we need to make sure that it does not react with the substrate/ bulk material etchant. Besides, it should be easy to deposit, pattern and remove.  $\text{SiO}_2$  and  $\text{Si}_x\text{N}_x$  are commonly used as masking material.

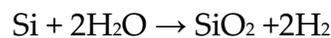
### **Silicon Dioxide ( $\text{SiO}_2$ )**

$\text{SiO}_2$  is silicon's native oxide. There are three major uses of silicon oxide in MEMS processes: (1) as a thermal and electric insulator, (2) as masking layer in case of etching silicon substrates, and (3) as a sacrificial layer in surface micromachining [15].  $\text{SiO}_2$  is popular for Si substrates as it can be easily grown by thermal diffusion/ oxidation process. Chemical reactions for this process are given below.

For dry oxidation:



For wet oxidation:

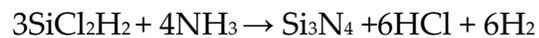


$\text{SiO}_2$  is diffused much faster in case of wet oxidation due to  $\text{H}_2\text{O}$  molecules presence in steam. The resultant oxide layer from this technique has high chemical

stability and it strongly sticks to the substrate below [16].

### **Silicon Nitride (Si<sub>3</sub>N<sub>4</sub>)**

Silicon Nitride is well known as electrical insulator between conductive layers. It acts as an excellent barrier for alkali ions. It is often used as masking layer for deep etching due to its chemical stability and high resistance to oxidation and many etchants. It requires boiling phosphoric acid to a wet etch Si<sub>3</sub>N<sub>4</sub>. Silicon nitride can be produced from silicon-based gases and NH<sub>3</sub> by low-pressure chemical vapor deposition (LPCVD) method and the plasma-enhanced chemical vapor deposition (PECVD) method as shown below [15,16]:

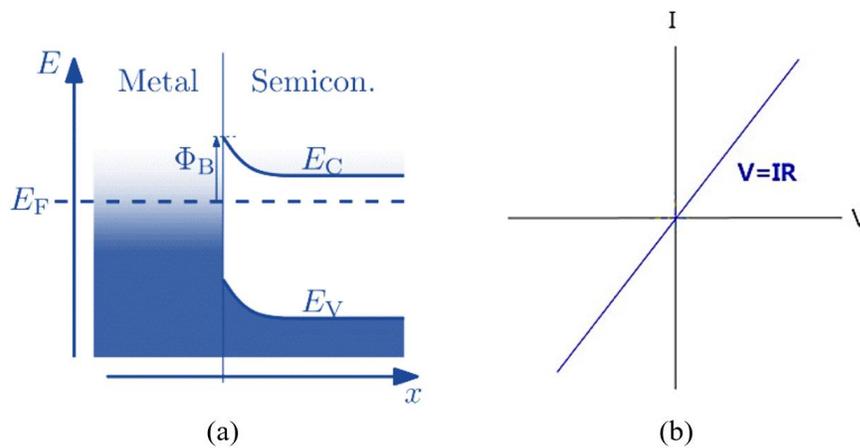


However, Si<sub>3</sub>N<sub>4</sub> properties varies depending on the chemical vapor deposition processes.

### *2.3.3 Common Metallization and Adhesion Materials for Micromachining*

It is essential to know the underlying physics at the metal-semiconductor interface to understand the reason of using adhesion materials. Most of the MEMS

devices use Si substrate and gold (Au) metal contact. At close contact, metal and semiconductor try to align their Fermi levels by rearranging their energy levels. So, the conduction band is pulled down to change energy level and develops built in voltage at the interface. Any metal-semiconductor contact can cause either ohmic contact or Schottky contact. Here, ohmic contact is preferred over Schottky contact as it allows current to flow in both directions (Figure 7) [21].



**Figure 7.** (a) Metal- n-type Semiconductor put in close contact; (b) Ohmic Contact IV curve.

Metallization is an important step for MEMS device fabrication. In MEMS industry, silicon is the leading material as it is cheap and abundant. Along with Si, metals are used in MEMS devices for their exclusive properties to improve the functionality of MEMS products. Metals can boost up the electrical, mechanical and optical properties of MEMS products. Mainly, metal layers are deposited to produce contact pads and connectors so that the device can take electrical signals

and provide appropriate output. While selecting metal for MEMS devices, three major conditions must be fulfilled. Firstly, the metal must have good conductivity to reduce power losses. Secondly, the metal should be inert or remain passive in operating environments if high reliability is required. Lastly, the metal should be compatible with the underlying material and manufacturing processes [22].

Gold (Au), Silver (Ag), Nickel (Ni), Aluminum (Al) are some common candidates for metallization. Although Au is expensive, it is widely used in MEMS devices for its superior properties. It has low resistivity ( $2.4 \mu\Omega\cdot\text{cm}$ ) and it does not corrode even at harsh environment. Even though Au undoubtedly fulfills the first two criteria, it does not tend to adhere well to Si and oxide surfaces. To combat this, one or more metals are normally used at the gold-substrate interface so that they stick together.

Traditionally, chromium (Cr) and titanium (Ti) are used as adhesion layer for sticking Au to Si or Si based materials. These materials have the unique property of adhering well onto common materials, even on semiconductors. Usually, thin Cr and Ti layers (5-10 nm) do not modify the substrate's and the device's properties. They enhance wetting at the interface by forming Ti-Au and Cr-Au chemical bonds [23]. Compared to Au/Ti combination, Au/Cr combination is highly immune to corrosion in normal atmospheres. However, even a negligible presence of halogens can alter the situation. Also, chromium is very mobile in the

Au grain boundaries. Corrosion immunity of Au/Ti combination can be enhanced by involving palladium (Au/Pd/Ti). Then again, this will increase the metallization resistivity [22, 24].

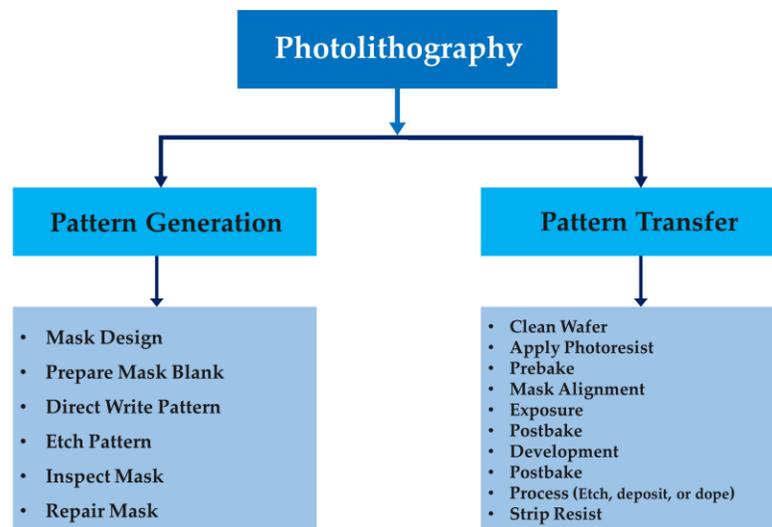
## 2.4 MEMS and Microelectronics Fabrication Techniques

MEMS and Microelectronics fabrication processes follow the same techniques. Many techniques (i.e. diffusion, oxidation, implantation, photolithography, deposition) and materials used in microelectronics fabrication are also exploited in MEMS fabrication for assuring low-cost, high reliability and high performance. Yet there is still some difference between these processes. For example, plating, molding, and wafer bonding are more common in MEMS than in microelectronics fabrication. Unlike microelectronics fabrication, MEMS fabrication focuses more on mechanical properties like Young's modulus, yield strength, residual stress, strain, density etc. As a result, MEMS devices tend to be bigger for achieving desired sensitivity. So, it requires some additional fabrication techniques for attaining deeper etch, and thicker deposition layer. Deep Reactive Ion Etching (DRIE) is exclusively used in MEMS fabrication process to etch deep cavity. Likewise, starting material for MEMS fabrication process is bulkier than

that of microelectronics fabrication process [25]. MEMS fabrication usually need wafer bonding to for protecting devices or the tool when deep etching is needed. Sometimes MEMS device fabrication can be simpler than microelectronics fabrication as they require lesser mask sets. This section focuses on specialized MEMS techniques such as: DRIE, wafer bonding along with other fabrication, packaging and wafer bonding techniques related to this research.

### 2.4.1 Photolithography

Photolithography is a mandatory technique in MEMS device fabrication. It can be divided into two steps: (1) Pattern Generation, (2) Pattern Transfer. These steps are combination of repeated techniques.



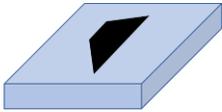
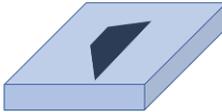
**Figure 8.** Lithographic processing steps.

## Pattern Generation

Mask designing is the primary step of pattern generation. A photolithography mask is an opaque/ transparent plate with some transparent/ opaque patterns which allows light to shine through the transparent areas to transfer patterns on the substrate underneath. Quartz, green soda lime, white crown, borofloat, borosilicate glass are some common mask substrate materials. Masks are usually coated with chromium to make opaque regions. The mask designer should try to fit in as many devices as possible onto a single mask set to get maximum number of devices at a time. The reliable function of MEMS devices largely depends on mask sets design and alignment. Even a slight misalignment can make a whole batch of dysfunctional devices. Therefore, some alignment marks are added along with desired geometrical patterns. The alignment mark's size depends on the minimum pattern size. For millimeter sized devices, alignment marks can be in nanometer range.

Other interesting topics are mask parity and tone (Figure 9). These are important if the design involves "mirror asymmetric" patterns. In mask designing, the original pattern shape is called as "Right-Reading". Similarly, the mirror image of the intended pattern as Wrong-Reading. Based on transparent and opaque regions, masks can be divided into two types: Light Field and Dark Field. If only the patterns are transparent, and the entire mask has chrome on it, then it called

dark field mask or dark tone mask. This type of mask is compatible with positive photoresists (i.e. S-1800 series, SPR 220 etc.). Light field/ light tone masks are the exact opposite of this and they are used for negative photoresists (i.e. SU-8).

	<p><b>Polarity: Light Field (LF)</b>  <b>Parity: Right Reading Chrome Up (RRCU)</b>            (Do <i>not</i> mirror the data)</p>
	<p><b>Polarity: Light Field (LF)</b>  <b>Parity: Right Reading Chrome Down (RRCD)</b>            (Mirror the data)</p>
	<p><b>Polarity: Dark Field (DF)</b>  <b>Parity: Right Reading Chrome Up (RRCU)</b>            (Do <i>not</i> mirror the data)</p>
	<p><b>Polarity: Dark Field (DF)</b>  <b>Parity: Right Reading Chrome Down (RRCD)</b>            (Mirror the data)</p>
<p>*the side with  is the, chrome, emulsion, or "contact" side.</p>	

**Figure 9.** Pictorial explanation of Parity and Polarity.

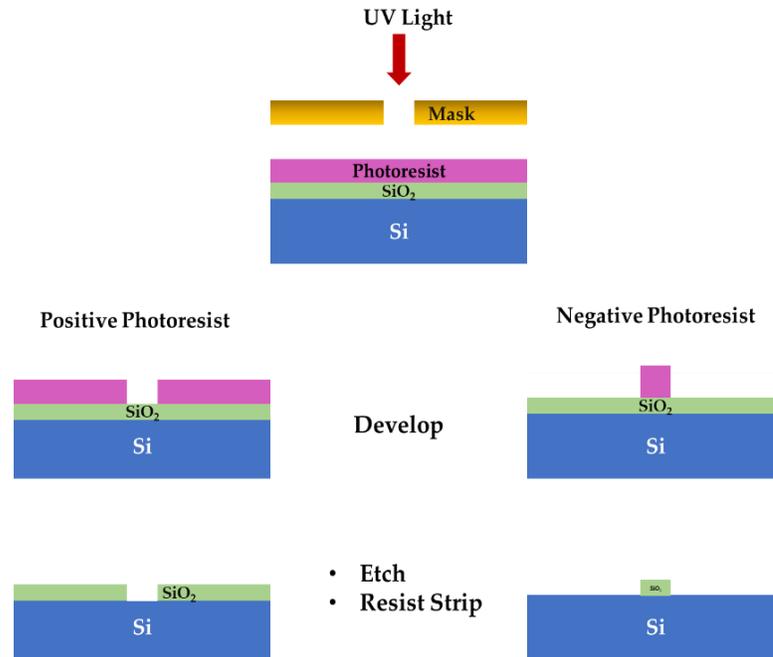
## Pattern Transfer

Photolithography is the process step used for transferring a pattern to a layer on the wafer. The photolithography process is done for fabricating each layers of a MEMS device. A light source must be used to transfer patterns from a mask to a photosensitive layer (i.e. photoresist) on a substrate or another thin film. The general sequence of processing steps for a typical photolithography process is given as: substrate preparation, photoresist spin coat, prebake, exposure, post-

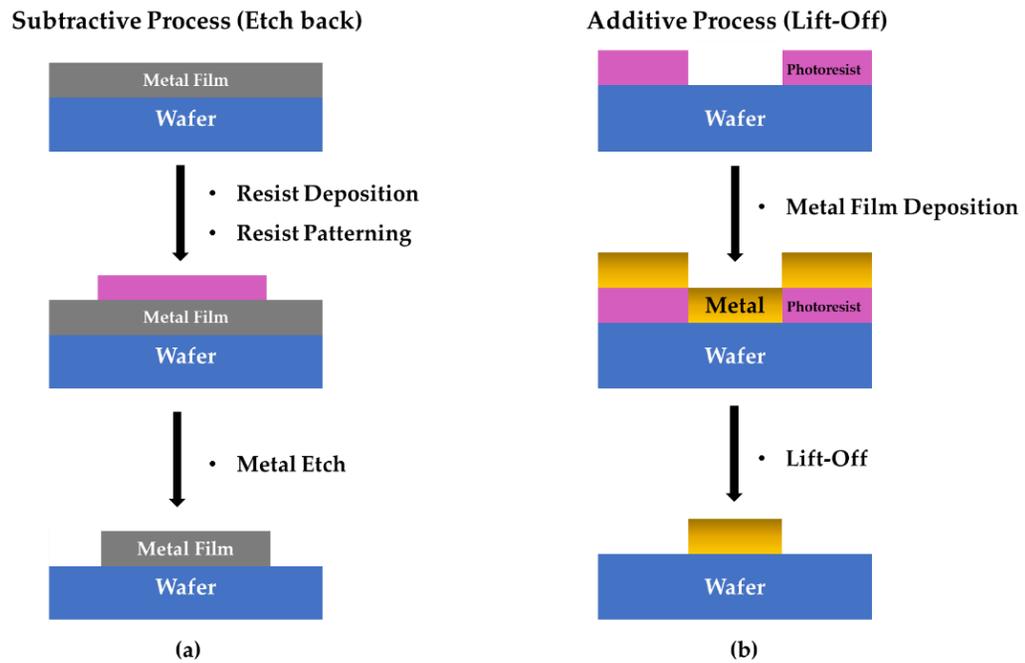
exposure bake, development, postbake, and resist strip [26]. Depending on how the resists react to the light source, there are two basic types of photoresist: negative and positive (Figure 10). For positive photoresist, the UV exposed region becomes soluble and dissolves when developed, only the unexposed resist remains. Positive resists are usually used in MEMS fabrication as they are easy to handle. For negative photoresists, the UV exposed region of photoresist layer become insoluble. When developed, non-exposed resist dissolves, leaving the exposed resist only.

Photolithography can be either an additive or a subtractive process. Etch back and lift-off are very popular techniques for MEMS metallization. Photoresists are often used as a temporary mask layer to etch the layer beneath (i.e. Aluminum). In this way, pattern from the original mask is transferred to that layer (Figure 11(a)). The photoresist layer is removed afterwards. This is a subtractive process and it is also called etch back process. In this case, selectivity is an important issue.

Photoresist are also used as a template to deposit material in a pattern after performing lithography. The material deposited on the resist is "lifted off" along with the photoresist layer (Figure 11(b)). Therefore, this additive process is also called Lift-off process. This allows us to use materials which are difficult to etch (i.e. Gold).



**Figure 10.** Photolithography process for positive photoresist and negative photoresist.

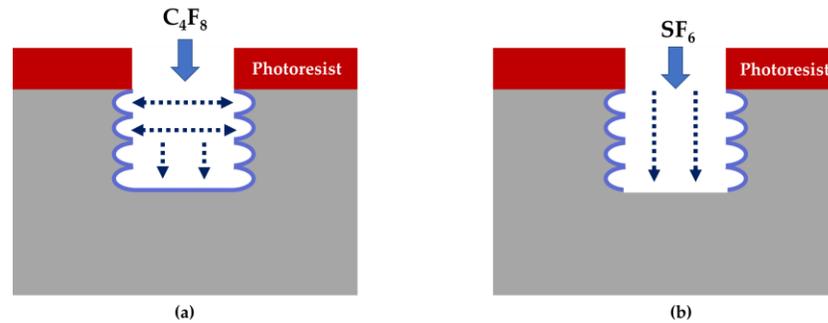


**Figure 11.** Photolithography process for positive.

### 2.4.2 Deep Reactive Ion Etching (DRIE)

Deep reactive-ion etching (DRIE) is a highly anisotropic etch process used to create vertical deep cavities and trenches in wafers with high aspect ratios (~30:1) in silicon-based MEMS devices. Unlike Reactive Ion Etching (RIE), DRIE systems have an inductively coupled power (ICP) source to provide a high-density plasma, and an independent substrate power bias to provide directional ion bombardment during the etch cycle [27].

There are two main technologies for high-rate DRIE: cryogenic and Bosch. Bosch technology exploits switched gas scheme for alternating surface passivation cycle and etch cycle (Figure 12). During surface passivation cycle,  $C_4F_8$  gas is used to make polymer coating on the entire upper surface of silicon. At etch cycle,  $SF_6$  gas is used for the silicon isotropic etching. After every etch cycle, a passivation cycle runs to protect the sidewalls for keeping the anisotropic high aspect ratio. Due to the alternating cycles, scallops occur at the sidewalls. While keeping the sidewalls intact, the passivation layer on the bottom of the trench is selectively removed by the vertical ion bombardment. Then, the  $SF_6$  isotopically etches the bottom silicon layer. The whole process keeps repeating until reaching the desired depth [28].

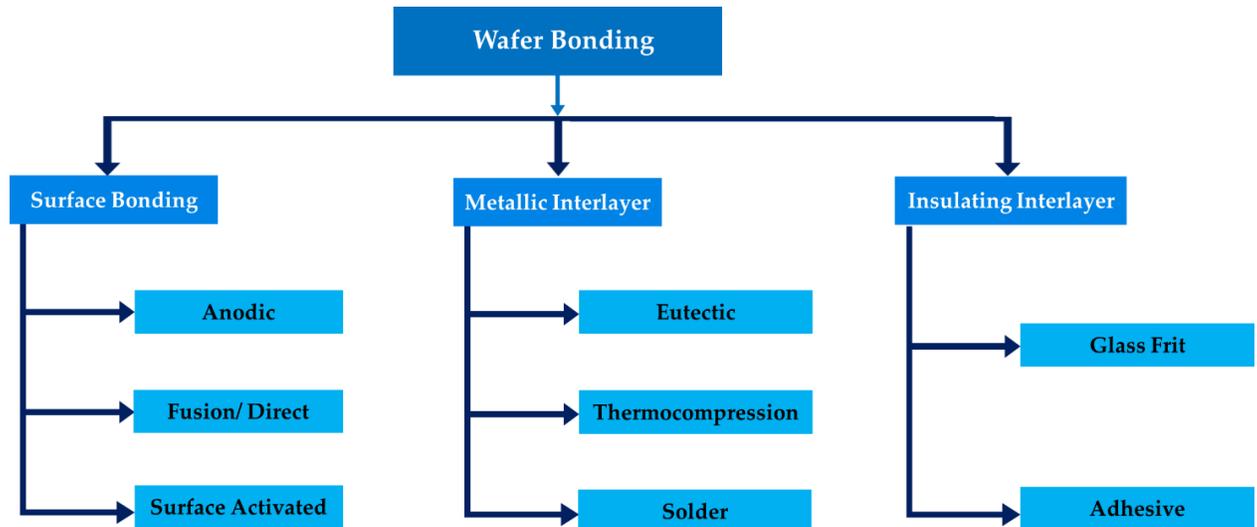


**Figure 12.** Deep reactive ion etching (DRIE) process: (a) sidewall passivation with  $C_4F_8$  gas; (b) silicon isotropic etching with  $SF_6$  gas.

### 2.4.3 Wafer Bonding

Many MEMS devices need to operate or process in a vacuum or hermetic environment where extra protection is needed to keep the device and the equipment unharmed. For this reason, wafer bonding used in MEMS processes. Unlike microelectronic devices, MEMS devices has several layer and complex mechanical structures for which wafer bonding is necessary. It is a packaging technology for MEMS devices to ensure a mechanically stable and hermetically sealed encapsulation. Along with wet and dry etching techniques, wafer bonding is often used for (1) fabricating pressure sensing membranes having thickness in micron range, (2) making multilayered complex structures for acceleration sensing, (3) fabricating multilayered devices for microfluidic applications, and (4)

fabricating high aspect ratio structures [29]. Figure 13 shows available Si wafer bonding techniques.



**Figure 13.** Wafer Bonding Methods

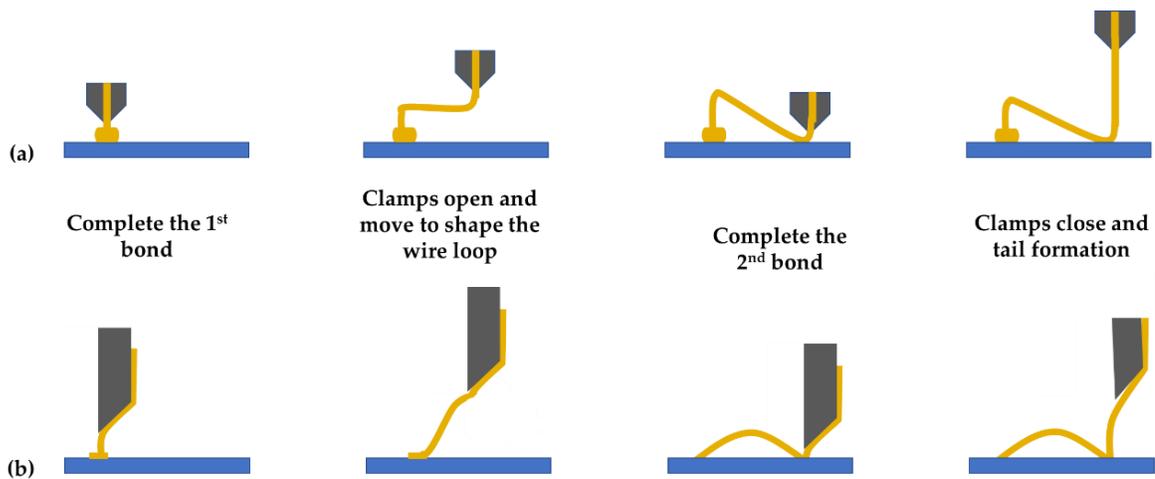
Anodic bonding is implemented to make bonding between silicon wafer and glass wafer with high amount of sodium. It requires low bonding temperature (300 °C – 500 °C) which increases design flexibility. The main difference among these methods is the material used as the bonding agent. However, all these wafer bonding techniques require high pressures and/ or high temperatures. Fusion/ Direct bonding is used to attach two or more Si wafers. It has three basic steps: Surface preparation, contacting, and annealing. In Surface activated bonding (SAB), surface is activated by fast atom bombardment. Semiconductor, metal, and dielectric materials can be bonded at room temperature utilizing this technique.

Eutectic bonding exploits eutectic point in metal-Si phase diagrams to form silicides. Thermocompression is generally done with electroplated Au, other soft metals. It requires low temperature and can attach rough surfaces as well. Solder bonding is a low temperature process and it can make successful bond even between slightly rough surfaces. Glass frit bonding is a widely used encapsulation technology for MEMS devices. A glass frit intermediate layer is used to bond Si with other oxide, nitride, metal or glass layer as long as their Coefficient of Thermal Expansion (CTE) matches. Adhesive bonding bonds two substrates of same or different materials. It is a high temperature process (~1000 °C). Usually, photoresists (i.e. SU-8), polymers (i.e. benzocyclobutene (BCB)) and gules (i.e. crystal bond) are used as adhesive for MEMS devices.

#### 2.4.4 *Wire Bonding*

There are three wire bonding technologies available in the industry. They are: thermosonic ball bonding, ultrasonic wedge bonding and thermocompression ball bonding. Choice of the technique depends on the device application. The formation of a ball bond requires deformation of the FAB on the heated substrate by the application of ultrasonic energy and bonding force. On the other hand, the wedge bond is formed by deformation of the wire by the application of bonding force and ultrasonic energy [30]. Usually, ball bonding applications are related

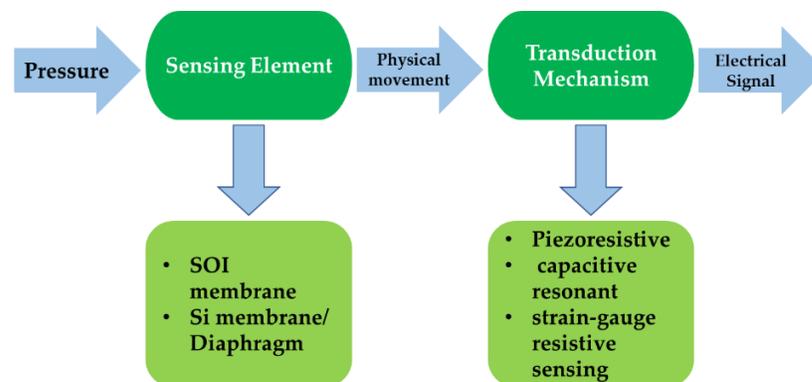
with thermocompression (T/C) and thermosonic (T/S) joining methods. The ball bonding process is suitable for high resolution applications around 40 microns or less. In general, it offers faster speed than wedge bond. Thermo-compression wire bonding can be implemented for our device. Au wire and Al pads on PCB board is cheap and reliable for such operation. The gold wire should be annealed to decrease its rigidity and improve the elongation. This improved elongation will ensure breakage free wire bonding process. Before bonding, Au wire should be heated up to form a ball approximately twice its diameter. 20 – 40  $\mu\text{m}$  diameter and ~20 mm length has been used before for chip bonding [31].



**Figure 14.** Wire bonding techniques; (a) Typical ball bonding steps; (b) Typical wedge bonding steps.

## 2.5 MEMS Pressure Sensors

General MEMS sensors convert physical stimuli from the optical, mechanical, thermal, and chemical domains to the electrical domain. Micromachined pressure sensors are commercially available for numerous applications like automotive, biomedical, environmental monitoring, and aerospace [32]. The MEMS pressure sensors utilize various techniques to convert mechanical pressure into electrical signals, such as piezoresistive, capacitive, resonant, and strain-gauge resistive sensing (Figure 15). However, commercial MEMS products are usually either piezoresistive or capacitive. Popular designs of pressure sensors are micromachined flexible membrane and diaphragm. Shape and size of the device depends on the application. Device surface area ranges from tens to thousands of microns in width and from a few to hundreds of microns in thickness [33,34].



**Figure 15.** Basic components and operating principle of MEMS pressure sensor.

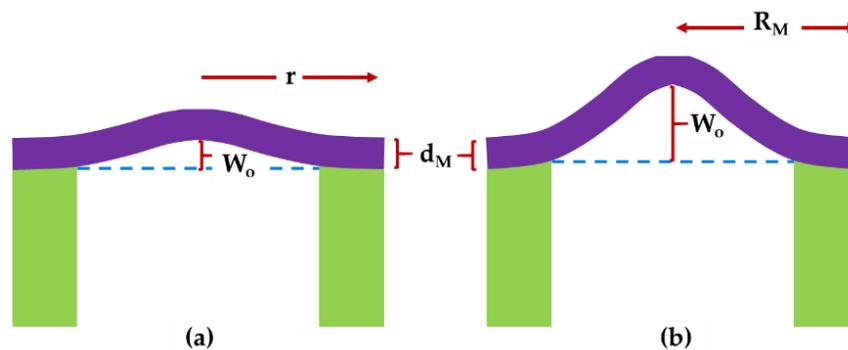
Pressure sensors are divided as absolute, gauge and differential pressure sensors based on the reference pressure with respect to which the measurement is carried out [8]. Absolute pressure sensors compare the applied pressure to a reference vacuum encapsulated within the sensor. Such devices are used for atmospheric pressure measurement, for automobile ignition and airflow control systems [35]. Gauge pressure sensor measures relates applied pressure to atmospheric pressure. These are used for measuring Blood Pressure (BP), Intra-Cranial Pressure (ICP), gas cylinder pressure etc. Differential pressure sensors measure the difference between two pressures across the sensing element. All the pressure sensors above uses membranes or diaphragms, which deflects when pressure is applied on them [8]. The key advantages of MEMS pressure sensors are low-cost, small size and weight, and quick response time in pneumatic applications [34].

### *2.5.1 Membranes*

Membranes are another type of thin films. They are an important mechanical basic element in micro technique. Microscopic membranes are compared to macroscopic gaskets, bearings, and springs. Silicon, oxides, nitrides, glasses, polymers, and metals are commonly used to fabricate MEMS membranes. Membranes can be up to 500  $\mu\text{m}$  thick. However, it is difficult to produce

membranes thinner than  $0.5 \mu\text{m}$  as they are prone to holes and not strong enough to withstand normal loads [34,35].

In MEMS products, there are two common shapes of membranes: Thick membranes and thin membranes. When a membrane's maximum deflection  $w_0$  is much smaller than its thickness  $d_M$ , it is considered as thick membrane. In the same way, when the deflection is larger than the thickness, it is called thin membrane. A thick membrane can be turned into a thin one when the pressure drop rises and the deflection is increased (Figure 16) [34].



**Figure 16.** Membranes; (a) Thick membrane; (b) Thin membrane.

The deflection curve of a circular, thin membrane takes a parabolic shape, and this is explained by the following equation:

$$W = W_0 \left( 1 - \frac{r^2}{R_M^2} \right) \quad (1)$$

where,  $W$  is deflection of a circular membrane,  $W_0$  is deflection at the center,  $r$  stands for membrane radius,  $R_M$  is the membrane radius for maximum deflection.

For thin membranes, the deflection is higher than the thickness. In response to applied pressure, thin membranes show a unique effect, called the ballooning effect. For this reason, there is an additional stretching stress ( $\sigma_s$ ) along with membrane bending stress ( $\sigma_b$ ).  $\sigma_s$  is always positive, regardless to the direction of force but  $\sigma_b$  can be either positive (pressure at front) or negative (pressure at back).

### 2.5.2 *Strain Gauges on Membranes*

To quantify pressure sensing Si membrane's deflection, strain gauges are often deposited/ implanted on/ in the membrane. For a typical Si membrane, deflection is less than a micrometer which is hard detect. Hence, strain gauges are used as their resistance change more than Si with pressure and temperature change due to strain. Two or four strain gauges are placed to form a Wheatstone bridge circuit for deflection measurement. As pressure is applied, the membrane along with the strain gauges stretch (Figure 17). The resistance change of strain gauges will change the Wheatstone bridge circuit's output voltage. This change is proportional to the applied pressure. The resistance of strain gauges varies for different

numbers and positions of gauges. The formula below is used to calculate the resistance (R) of the strain gauge material:

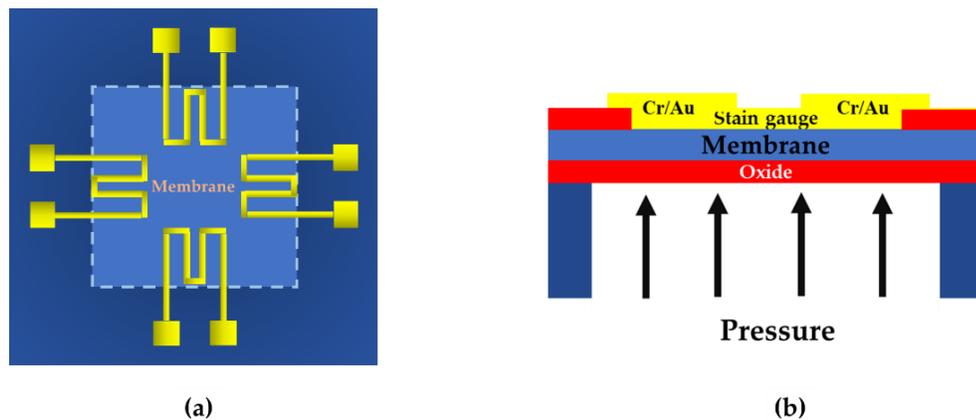
$$R = \rho \frac{L}{A} \quad (2)$$

here, R stands for resistance,  $\rho$  is the resistivity, L and A are the length and area of the strain gauge, respectively.

In the Wheatstone bridge application, the resistivity ( $\rho$ ), is a physical property of the material and it stays constant for constant pressure and temperature. Resistivity of a material, is inversely proportional to its conductivity,  $\sigma$ :

$$\sigma = \frac{1}{\rho} \quad (3)$$

The equation (2) and (3) indicate that as the material stretches, the length increases while the area decreases. This causes an increase in overall resistance [36].



**Figure 17.** Pictorial illustration of a strain gauge pressure sensor; (a) top view showing strain gauges connected in a Wheatstone bridge fashion; (b) cross sectional view.

### 2.5.3 *Piezoresistive MEMS Pressure Sensors*

Piezoresistive sensors depend on the piezoresistive effect. This is a phenomenon where the material's resistance changes when the applied mechanical strain changes [37]. The piezoresistive effect in silicon depends on the changes at atomic level. The Average effective mass of the carriers in the silicon may increase or decrease as stress is applied and it depends on the direction of the stress, current flow, the crystallographic orientation, and the direction of current flow. This change modifies the silicon's carrier mobility. As a result, its resistivity changes. Temperature plays a vital role in the operation of membrane based piezoresistive sensor. The design of such devices should ensure that the change in conductivity with temperature of PZR on membrane is minimum. The doping concentration should be properly optimized to accomplish this. Nowadays, SOI wafers are used for making diaphragm or membrane based piezoresistive pressure sensors [38]. SOI technology isolates the piezoresistive sensing elements from the substrate and from each other by a non-conductive isolation layer of silicon dioxide. This lets the sensor to behave predictably from cryogenic temperatures to 1000°F and above. SOI piezoresistive sensor technology has industrial usage because of its small size and high flexibility in packaging than

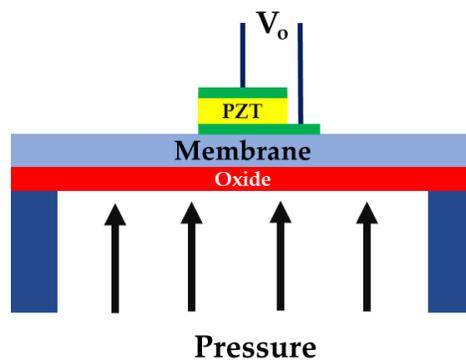
other renowned technologies. It has automotive applications like engine air, oil, cooling and fuel systems, brake systems, transmissions etc. [39].

The piezoresistive pressure sensors have a micromachined silicon membrane and a substrate. The piezoresistive resistors are diffused or implanted into the pressure sensing membrane [37]. When pressure is applied on the membrane, it causes stress on the membrane surface. As a result, deflection occurs. This deflection adds strain at the piezoresistive materials which changes in their resistance. Usually, the piezoresistors are connected in a Wheatstone bridge circuit fashion which converts the resistance change into an electrical signal. The piezoresistor should be placed at the location where maximum stress occurs to maximize the sensitivity. Now-a-days, boron-doped silicon piezoresistors are used instead of metal strain gauges to achieve higher sensitivity. Piezoresistors are embedded directly on the silicon membrane by implanting or diffusing boron in the regions of maximum stress [4].

#### *2.5.4 Piezoelectric MEMS Pressure Sensors*

Piezoelectric MEMS pressure sensors rely on the piezoelectric effect. When stress is applied on a crystal, it reorients and forms an internal polarization. Consequently, charge is generated on the crystal face that is proportional to the

applied stress [40]. For this reason, unlike other strain gage and piezoresistive sensors, piezoelectric sensors do not need external excitation. Lead Zirconate Titanate (PZT), zinc oxide (ZnO), quartz, tourmaline, and several other naturally occurring crystals have piezoelectric effect and often used in piezoelectric sensors. As a response to applied pressure, the membrane deflects and induces strain in the piezoelectric material above it. Thus, the piezoelectric material generates a charge. However, such pressure sensors are appropriate only for dynamic pressure measurement but not for static pressure sensing since piezoelectric materials respond only to varying strains [4]. Figure 18 shows a basic piezoelectric MEMS pressure sensor.



**Figure 18.** Schematic diagram of a Piezoelectric pressure sensor.

### 2.5.5 Heat Transfer

Heat transfer is the flow of thermal energy because of temperature difference between two mediums. There are three primary methods of Heat transfer method is categorized into three kinds: convection, conduction and radiation. In convection process, heat is transferred from high temperature region to low temperature region via heated particle movement due to density difference. It happens mostly with the liquid and gaseous elements. Conduction is a process by which heat is transferred from hotter to cooler portion of a substance only by molecular vibration. Generally, it occurs with solids. Another heat transfer process is radiation. Here, thermal energy does not require any medium and heat is transferred through electromagnetic radiation.

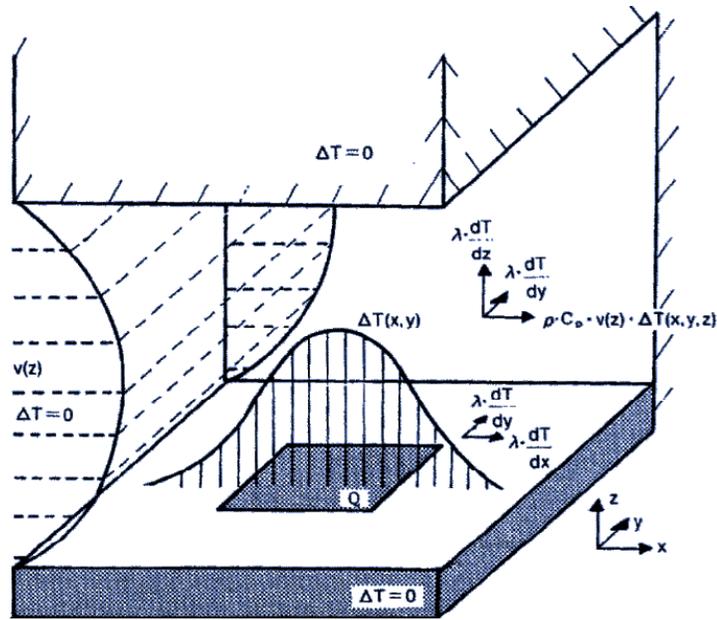
Heat energy is transferred with a combination of all the processes mentioned above. Among the three processes, conduction is the most effective one for a small device like our SOI membrane. When a small device similar to our membrane is heated up, almost 98% of the heat energy transferred is through conduction [41]. For this reason, we will be using a conduction- based approach to heat up and actuate our MEMS device. The heat flux due to convection in  $W/m^2$  is given as [42]:

$$q_{\text{cond}} = -k \frac{dT}{dx} \quad (4)$$

here,  $k$  refers to the material's conductivity, and temperature gradient across the material is denoted by  $\frac{dT}{dx}$ .

### **Joule Heating**

Joule/ resistive/ ohmic heating is a process of heating up a substance by producing heat from electric current flow through a resistance. Here, electric energy is transformed into heat through resistive losses in the material. For introducing thermal stress to the membrane, we will heat it through Joule heating from a gold resistive heating element/ strain gauge fabricated on top of the membrane. When external voltage will be applied through the resistive heating element, a current will be produced, and this will heat up the membrane. Several research groups had used this technique to evaluate membrane buckling. Bouwstra *et al.* for fabricated resistive heater onto device for detecting mass flow rates using a unique sensor design to measure flow rates of fluids by detecting the natural frequency shift of a thermally actuated, unbuckled membrane [41].



**Figure 19.** Two-dimensional thermal conduction within the membrane showing components of heat transfer, boundary conditions and gas velocity profile [41].

Their model considers conductive heat transfer to membrane from the heating resistor at the center. Temperature across the membrane is given by,

$$\Delta T_{\text{avg}} = \frac{H}{4\pi\lambda t} \quad (5)$$

where,  $H$  is the heat generation per unit time,  $\lambda$  is the heat conduction coefficient, and  $t$  is the membrane's thickness. However, heat transfer depends on the heater's thermal resistance as shown in equation (2) [41]. In a model considering meandering resistor, resistance is given as,

$$R = R_s(N + (k'N_{cb})) \quad (6)$$

where,  $R$  is the total resistance,  $R_s$  stands for sheet resistance,  $N$  is the number of straight regions blocks,  $k$  is the corner block correction factor, and  $N_{cb}$

is the number of corner blocks [33]. Electrical power lost through the resistor converts to heat. This can be expressed as,

$$P = I^2R \quad (7)$$

where, I and R is the current and resistance, respectively.

### III. Methodology

This chapter provides details of the device structure, its working principle, design and fabrication procedures. The first two sections of this chapter tell the device structure and its operational principle. The following two sections describes fabrication and packaging techniques. The last section briefly discusses finite element analysis (FEA) methods for estimating device performance.

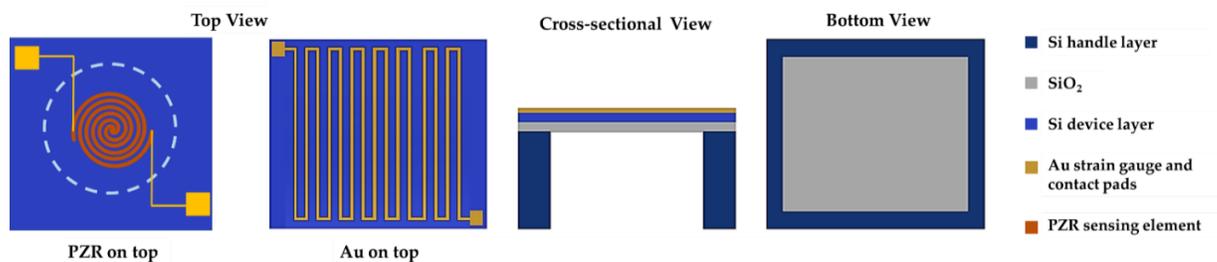
#### 3.1 Device Structure

The fabrication procedure of this pressure sensor can be divided into two sections: resistive heater or sensing element fabrication and membrane fabrication.

The starting material or SOI wafer consists of three main parts (1) Si handle wafer

(~500  $\mu\text{m}$ ), (2) thin  $\text{SiO}_2$  layer (~2  $\mu\text{m}$ ), and (3) Si device wafer (~5-20  $\mu\text{m}$ ) [7]. Silicon – On – Insulator (SOI) wafers are fabricated by wafer bonding process. At first, a silicon dioxide layer of the desired thickness (~ 0.25  $\mu\text{m}$  to 2  $\mu\text{m}$ ) is grown on a polycrystalline silicon substrate or handle wafer. Afterwards, a crystalline silicon wafer is bonded on top of it at high temperature. Hence, the silicon dioxide layer becomes sandwiched between two silicon wafers. The crystalline silicon layer is thinned down to a preferred thickness by chemical mechanical polishing (CMP). On top of this SOI wafer, a meandering strain gauge is fabricated and the stress on the membrane can be varied by heating up this heating element.

Instead of Au heating element, piezoelectric element like  $\text{Si}_3\text{N}_4$  or B-Si can be deposited/ implanted onto the membrane for determining applied pressure. Figure 20 shows our device's schematic diagram with piezoresistive (PZR) sensing element and with Au strain gauge.



**Figure 20.** Top views of circular membrane with PZR element and Top, cross-sectional and bottom view of rectangular membrane with Au on top.

## 3.2 Working Principle

We can divide the device operation into two parts: membrane operation and Wheatstone bridge operation.

### 3.2.1 Membrane's operation

In this research, MEMS membrane pressure sensors are constructed using silicon-on-insulator (SOI) wafers and there can be gold/ piezoresistive and/or piezoelectric meandering or spiral sensing element on top of it. Here, the coefficient of thermal expansion (CTE) of Si is  $2.5 \times 10^{-6}/\text{K}$  and that of silicon dioxide is  $0.55 \times 10^{-6}/\text{K}$ . As a thin SiO<sub>2</sub> layer is formed on a thick Si substrate at high temperature then cooled down and operated at room temperature, a residual stress between the layers is created due to the mismatch of CTE. Therefore, a strain of material is observed [49], [50]. Since CTE of Si is larger than SiO<sub>2</sub>, its tendency to contract is higher compared to SiO<sub>2</sub>. As these layers are bonded, a compressive stress is induced in SiO<sub>2</sub> which is responsible for the buckling of the membrane [51], [33], [52]. This strain can be found from Eq. (8),

$$\varepsilon = - \Delta\alpha (T_2 - T_1) \quad (8)$$

The membranes flex with applied pressure and bursts when the operational pressure range is exceeded. This burst pressure and its relationship with the geometry of membrane can be explained using Cabrera's equation as follows:

$$\Delta p = 4 \frac{d_M}{R_M} \sigma \sqrt{\frac{3}{2} (\sigma_0 - \sigma) \frac{1 - \nu_M}{E_M}} \quad (9)$$

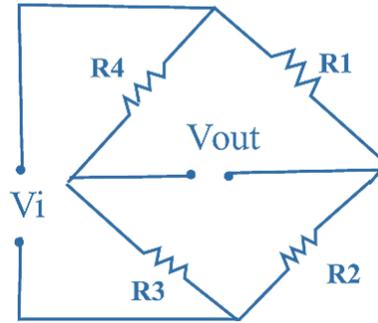
here, burst pressure ( $\Delta p$ ) is a function of membrane radius ( $R_M$ ) and thickness ( $d_M$ ). The equation shows that as the area or radius of a membrane ( $R_M$ ) is increased and thickness of the membrane is decreased, the membrane becomes robust and durable to high pressure.

### 3.2.2 *Wheatstone bridge operation*

In aqueous environment, the membrane will flex when water pressure is applied. Now, we can compare the membrane deflection with applied water pressure, or we can check the resistivity change of sensing material with applied pressure to realize it as pressure sensor. For the latter case, resistivity of the sensing material will change with membrane's deflection. Now, if we can measure the change in resistance of our device, we will be able to correlate the applied pressure with resistance change.

A popular approach is to use Wheatstone bridge circuit for measuring resistance change. Wheatstone bridge circuit (Figure 21) is the most commonly used circuit for strain measurement and determining voltage differences in electrical circuits for its high sensitivity [53]. Four resistors are connected and one of them acts as a sensing resistor. Here in our case, it will be the PZR sensing element. An input voltage is applied across two junctions that are separated by two resistors and voltage drop across the other two junctions forms the output. By measuring the voltage across the circuit, resistance change of the device can be measured.

There are three ways in to involve Wheatstone bridge configuration with the MEMS sensing devices. These are external Wheatstone bridge circuit, two-chip approach and monolithic approach [54]. The first approach is the simplest as it is easy to implement and modify. The latter two approaches allow direct Wheatstone bridge circuit integration with MEMS device. In two-chip approach, the MEMS device is mounted on a printed circuit board (PCB) where the Wheatstone bridge circuit is laid out. Electrical connection between these chips are done using wire-bonding technique. In monolithic approach, MEMS sensing device and the Wheatstone bridge circuit is fabricated on the same silicon wafer sample using MEMS technology. Therefore, the monolithic approach ensures smaller device footprint and lower noise levels [55].



**Figure 21.** The Wheatstone bridge configuration with one of the resistors element ( $R_2$ ) as variable resistor.

When strain gauges are placed in a Wheatstone bridge configuration and integrated with a pressure-sensitive membrane, a change in resistance is converted to a voltage output which is proportional to the applied pressure. Here, the change in resistivity as a result of applied pressure is called piezoresistive effect. The resistance of the sensing material is given by equation (2).

When pressure is applied,  $R_1$  and  $R_3$  are subjected to longitudinal stress and they exhibit an increase in resistance.  $R_2$  and piezoresistor  $R_4$  are subjected to tangential stress and they exhibit a decrease in resistance. The output voltage  $V_{out}$  of the Wheatstone bridge is given by [8],

$$V_{out} = V_i \left[ \frac{R_1}{(R_1 + R_2)} - \frac{R_4}{(R_3 + R_4)} \right] \quad (10)$$

Here,  $V_i$  is the input voltage to Wheatstone bridge,  $P$  is the applied pressure. The sensitivity  $S$  of a pressure sensor can be written as,

$$S = \frac{V_{\text{out}}}{V_i} \times \frac{1}{P} \text{ mV/ V/ MPa} \quad (11)$$

### 3.3 Design

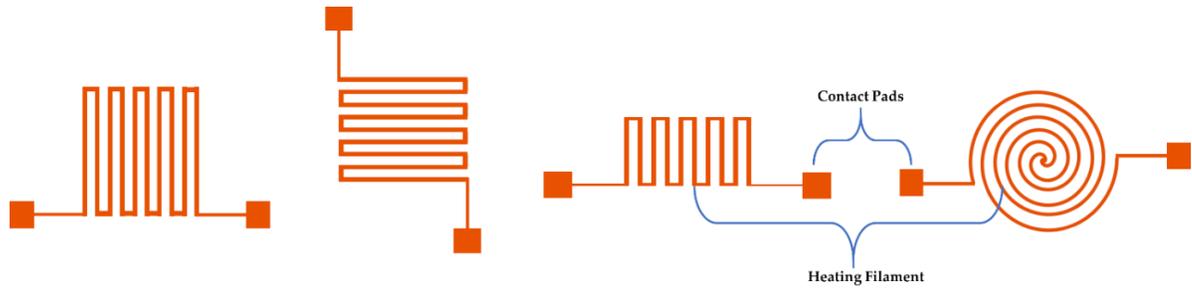
This section focuses on device design. Here, strain gauge and membrane designs are discussed. We discussed about the reasons corroborating the designs and the mask sets for fabricating the devices.

#### 3.3.1 *Strain gauge resistor design*

For our device, we are using two strain gauge resistor designs. These are rectangular gauge with sharp cornered filaments and a spiral gauge with rounded filaments (Figure 22). Dimension of the strain gauge structure changes according to the membrane's shape. On the square strain gauge resistors, we have changed filament number and spacing to ensure low voltage and high heating capability. The only drawback of this style is higher current concentration at the corners.

The second strain gauge resistor style was designed in a spiral shape for reducing current concentration at the corners [56]. Spiral resistors are composed of comparatively thinner wire than rectangular resistors and therefore have larger

spacing. Resistor's geometry affects the power requirement of the device, but the heat generated will remain almost the same [57].



**Figure 22.** Rectangular meandering and spiral strain gauge resistor designs.

Thermal transfer is inversely proportional to thermal resistance of the material. High thermal resistance results in greater thermal isolation. Thermal resistance is similar to electrical resistance and it can be expressed in the following form [56]:

$$R = \rho \frac{L}{A} \quad (12)$$

Here,  $\rho$  is the electrical resistivity,  $L$  is the length, and  $A$  is the surface area of a resistor.

The joule/ ohmic heating power or loss related to current flowing through a resistor is written as,

$$P = I^2 R \quad (13)$$

where,  $I$  is the current and  $R$  is the resistance [58].

The strain gauge resistor's resistance largely depends on its length, width, thickness, resistivity, sheet resistance, and the material's property [59]. Considering higher current concentration at the corners of square meandering resistor, its overall resistance is given as,

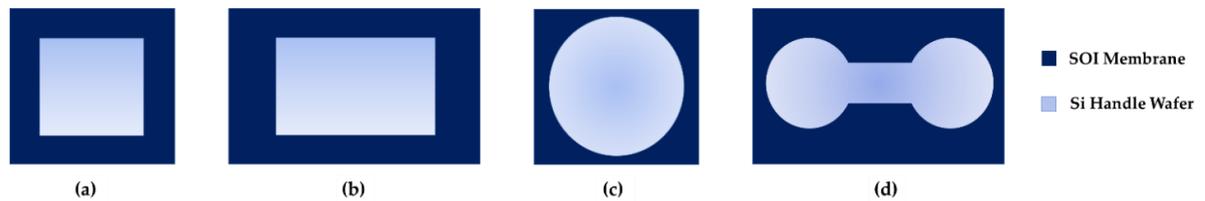
$$R = R_s(N + (K' \times N_{cb})) \quad (14)$$

where,  $R$  is the overall resistance,  $R_s$  is the sheet resistance,  $N$  is the number of subcomponent blocks in the straight sections,  $K'$  is the corner block correction factor, and  $N_{cb}$  is the number of corner blocks [59].

### 3.3.2 Membrane design

Membranes of various shape and size are fabricated to analyze geometrical effect on stiffness (Figure 34). Numerical analysis regarding this will be shown in chapter 4, section 4.1. To analyze membrane reliability (operational at high pressure up to 120 psi and above), membrane thickness was varied from 5  $\mu\text{m}$  to 30  $\mu\text{m}$ . Circular membranes diameter were varied from 0.25 mm to 8 mm and rectangular membranes edge length ranged from 0.25 mm to 7 mm. As membranes stiffness depends on both surface area and thickness, multiple combinations of thickness and area are considered in this way. Typically, square

and circular shaped membranes are fabricated to pressure sensing applications. We have designed dumbbell shaped or double cavity shaped membranes (Figure 23 (d)) which can be used for differential pressure sensing.



**Figure 23.** Membranes of various geometrical shapes; (a) square; (b) rectangular; (c) circular; (d) dumbbell.

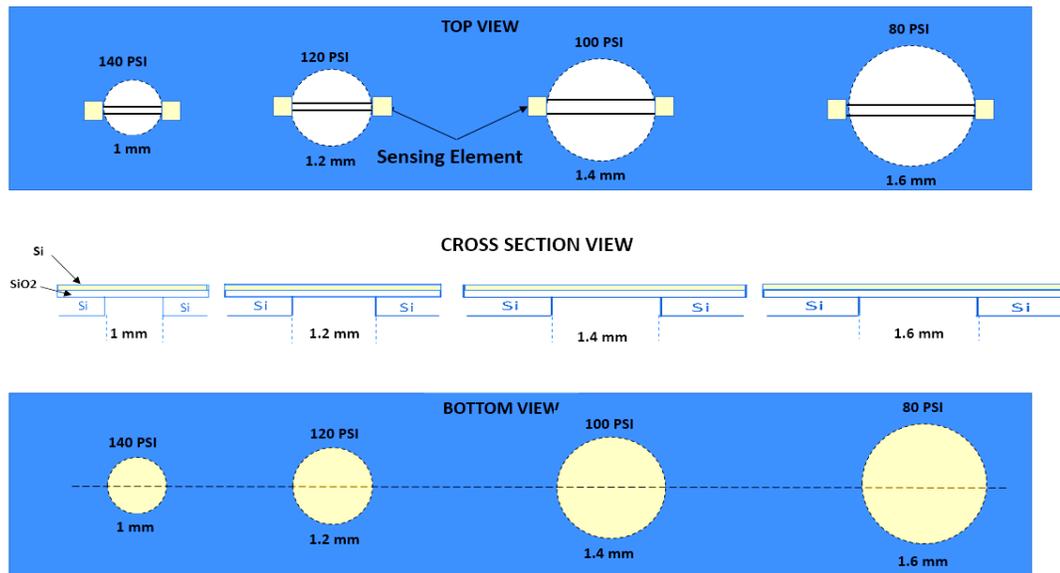
To design these membranes, Cabrera's equations for square and rectangular membranes (equation 15 and 16) were followed.

$$\text{Square Membrane:} \quad \Delta P = 66 \frac{d_M^3}{a_M^4} \frac{E_M}{1-\nu_M^2} W_0 \quad (15)$$

$$\text{Circular Membrane:} \quad \Delta P = \frac{16}{3} \frac{d_M^4}{R_M^4} \frac{E_M}{1-\nu_M^2} W_0 \quad (16)$$

where, burst pressure ( $\Delta P$ ), is a function of two key parameters: membrane radius ( $R_M$ ) and thickness ( $d_M$ ). The equation indicates that as the radius of a membrane ( $R_M$ ) is increased, the more susceptible the membrane is to burst at lower pressures with a constant membrane thickness. In this study, we proposed to fabricate multiple membranes of the same thickness yet varying diameter, onto

a single silicon wafer/coupon, for water pressure sensing and leak detection precisely to determine device failure (Figure 24)



**Figure 24.** Top, cross-sectional, and bottom views of a notional membrane coupon.

### 3.3.3 Mask design

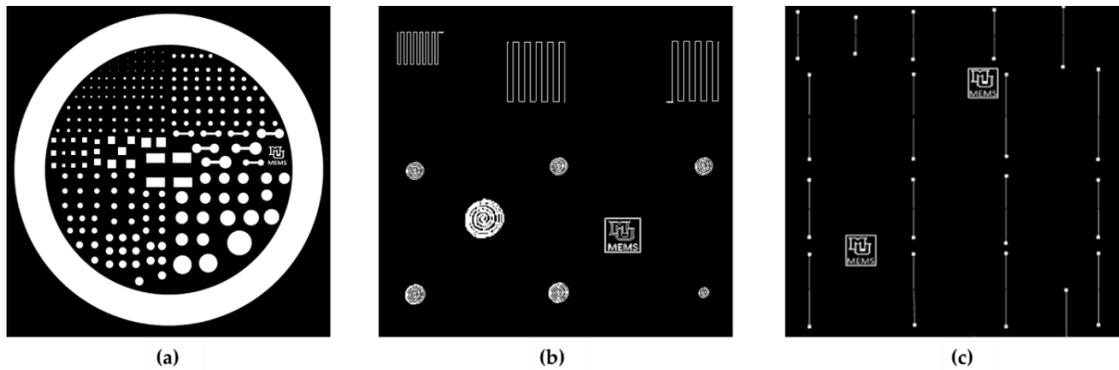
The first step of mask making is the layout. The desired patterns that will be transferred to the mask are defined using SolidWorks 2D engineering drawing documents. Our device requires total three mask sets: membrane etch mask, strain gauge resistor deposition mask, and Metal contact deposition mask. Among these, only the membrane etch mask will be used for backside processing. Other masks

will be used for frontside processing. Therefore, they require alignment marks to ensure reliable electrical connection between metal (i.e. Au) trenches and strain gauge/ PZR. Mask layouts are saved in .dxf file format for manufacturers.

Mask sets were designed for 4" wafers and 5" square mask plate. Pattern geometries of membrane etch mask and strain gauge resistor deposition mask are discussed in previous sub-sections. We used "Area Fill" under annotation for the patterns.

Membrane etch mask incorporates circular (ranging from 200  $\mu\text{m}$  – 8 mm in diameter), square, rectangular edge length ranged from 0.25 mm to 7 mm and other novel geometry etch holes to lower stress and increase yield. For the DRIE tool, we designed dead area in our mask so that there remains 10 mm wide empty region around the wafer's periphery.

The strain gauge resistor deposition mask has circular and rectangular meandering structures depending on the etch mask features. The resistors are approximately one third of the corresponding membrane in size. Another mask has metal contact pads of 150 $\mu\text{m}$  x 150 $\mu\text{m}$  and 25 $\mu\text{m}$  wide trenches. These masks have alignment marks like "+". Latter one has comparatively bigger mark to see the position of the prior one's marking. Figure 25 shows these mask layouts.



**Figure 25.** Mask Layouts for our MEMS device; (a) membrane etch mask; (b) strain gauge resistor deposition mask; (c) Metal contact deposition mask.

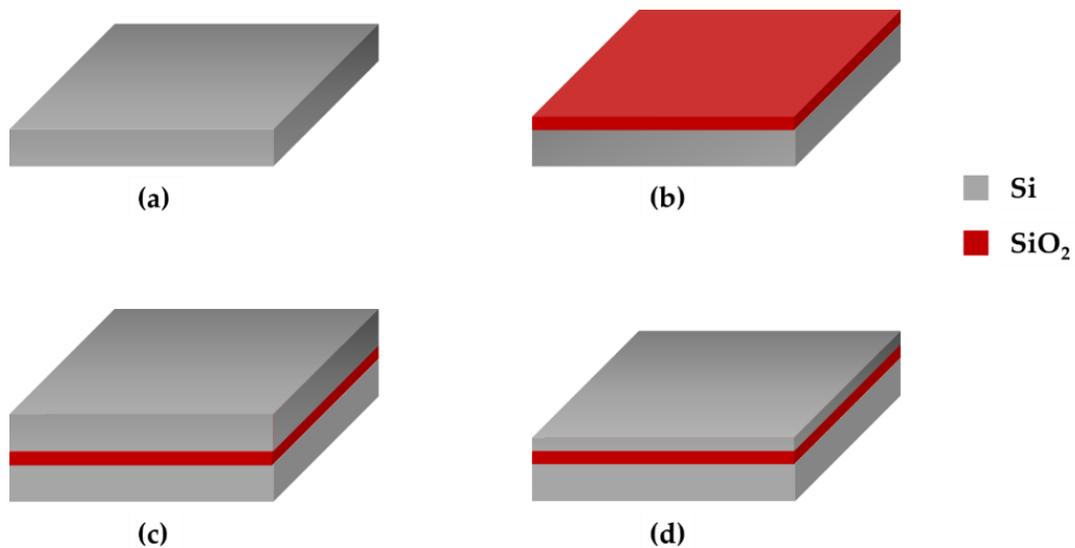
### 3.4 Device Fabrication

These microfabrication processes employ 4-inch (100) n-type double side polished SOI wafer. The device layer is  $5 \pm 1 \mu\text{m}$  and device resistance is  $2\text{-}5 \Omega\text{-cm}$ , handle wafer had thickness of  $550 \pm 10 \mu\text{m}$  and handle resistivity of  $1\text{-}10 \Omega\text{-cm}$ , the oxide layer is  $2 \pm 5\%$ . This SOI wafer was fabricated employing wafer bonding process.

#### 3.4.1 SOI wafer fabrication

SOI wafers are fabricated by a wafer bonding process. At first, an oxide layer of the preferred thickness ( $0.25 \mu\text{m} - 2 \mu\text{m}$ ) is thermally grown on a silicon wafer,

also called silicon handle wafer ( $\sim 500 \mu\text{m}$ ). Then, a second silicon wafer, called device wafer is bonded with at high temperatures ( $\sim 1100 \text{ }^\circ\text{C}$ ). The oxide layer is now sandwiched between these two silicon wafers. After completing the bonding process, silicon device layer is thinned down to the required thickness ( $\sim 5\text{-}20 \mu\text{m}$ ) by chemical mechanical polishing (CMP) [60]. Figure 26 shows the SOI wafer fabrication process step by step.

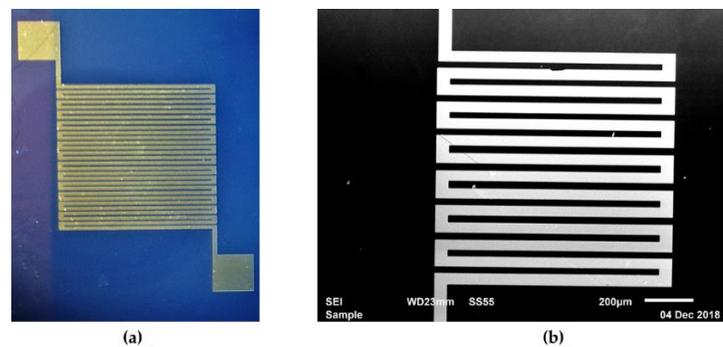


**Figure 26.** SOI wafer fabrication process. (a) silicon handle wafer ( $\sim 500 \mu\text{m}$ ); (b) a thin silicon dioxide layer ( $0.25 \mu\text{m} - 2 \mu\text{m}$ ) is grown on top of the handle wafer; (c) silicon device wafer is bonded onto the oxide layer; (d) silicon device wafer is thinned to the desired thickness ( $\sim 5\text{-}20 \mu\text{m}$ ) via chemical mechanical polishing (CMP).

### 3.4.2 Strain gauge fabrication

#### Meandering Au strain gauge:

At first, the sample was cleaned using methanol, acetone and DI water respectively and dried using pressurized nitrogen gas. The sample was spin coated for 30s at 4000 rpm to form a layer of S1818 photoresist and then soft – baked for 60s at 115 °C in hotplate. Subsequently, it was exposed to UV – radiation along with MJB-3 mask aligner and developed with 5:1 DI water to 351 developer in spin coater at 500rpm. After rinsing and drying, a 3000Å of gold layer was deposited. Beneath that, a 500Å of titanium or chromium was formed for adhesion. As the metal deposition was completed, unnecessary metals were removed by lift-off process. Acetone was used to remove the residual photoresist leaving only resistive heater on the sample [33]. Figure 27 shows microscopic and SEM images of the different Au strain gauges.



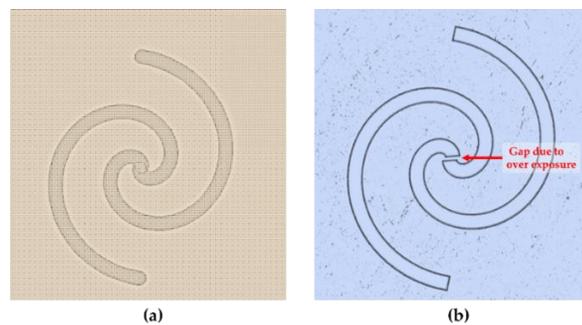
**Figure 27.** SOI membranes strain gauge image; (a) using AmScope microscope and 3-megapixel camera (b) SEM image.

**PZR strain gauge:**

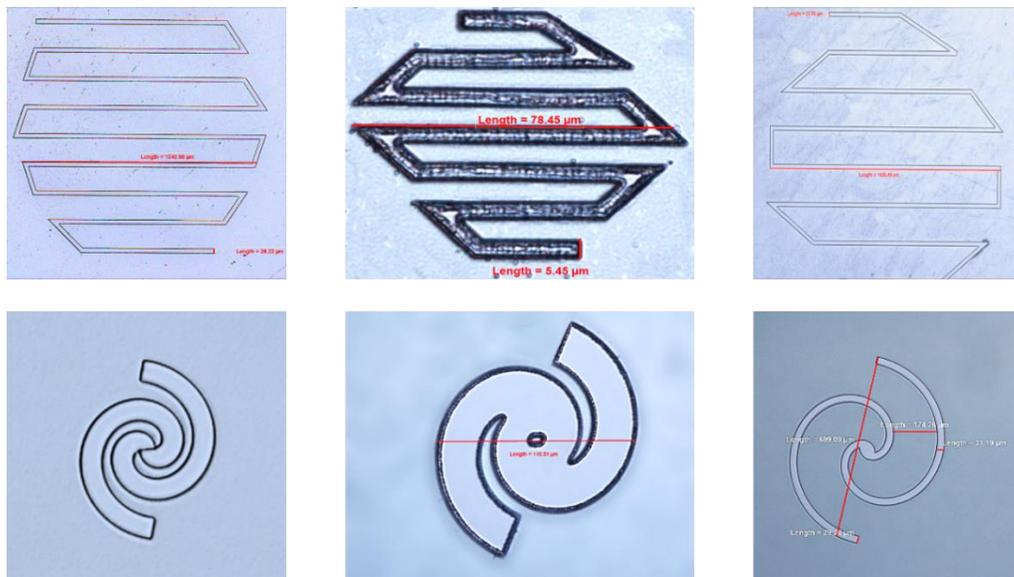
As PZR materials show better sensitivity in pressure sensing applications, we have deposited silicon nitride ( $\text{Si}_3\text{N}_4$ ) as sensing element. For better adhesion, we deposited  $\text{SiO}_2$  prior nitride deposition. We used Plasma-Therm Apex SLR HDPCVD System from PNF for oxide and nitride deposition. At first, we deposited  $1\mu\text{m}$  oxide layer as adhesion layer. Then, we deposited  $1\mu\text{m}$  nitride layer. Now, we kept it in Hexamethyldisilazane (HMDS) oven at  $120^\circ\text{C}$  for 10 minutes to form a HMDS monolayer. This will help the photoresist to ensure good photoresist adhesion. Then, we coated our sample with AZ nLOF 2020. We spin coated at 4000 rpm for 45s and softbaked it for 1 minute at  $100^\circ\text{C}$ . We transferred our patterns using Heidelberg Direct Write Lithography system at 375 nm laser ( $\sim 210\text{ mJ}/\text{cm}^2$  dose). The sample was kept on a hotplate at  $100^\circ\text{C}$  for 1 minute. The sample was developed by AZ 300 MIF developer for 1 min and then rinsed in DI water flow for at least 1 minute.

At this point, the sample was prepared for etching. We put our sample into the Plasma-Therm ICP Fluoride Etcher's load lock. After preparing the etch recipe, it took 10 minutes to etch out the unwanted nitride and oxide. To remove remaining unwanted photoresists, we used YES PLASMA ASHER for  $\text{O}_2$  Plasma Asher Descum cleaning.

We analyzed our sample wafer under Nikon Eclipse L200 Microscope to see how the patterns came out. Following figures show microscopic images of  $\text{Si}_3\text{N}_4$  pattern (Figure 28, Figure 29). We learnt that  $\text{Si}_3\text{N}_4$  deposition follows the mask patterns. However, as there was an overlap in design, it resulted in gap when over exposure occurs (Figure 28).



**Figure 28.** Gap in  $\text{Si}_3\text{N}_4$  pattern deposition due to over exposure.



**Figure 29.** Microscopic images of deposited  $\text{Si}_3\text{N}_4$  pattern.

We measured combined layer thickness of SiO<sub>2</sub> and Si<sub>3</sub>N<sub>4</sub> with Bruker Dimension Icon AFM profilometer and it was found to be ~2 $\mu$ m (Figure 30).

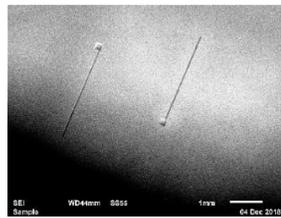


**Figure 30.** SiO<sub>2</sub> and Si<sub>3</sub>N<sub>4</sub> thickness measurement using Bruker Dimension Icon AFM profilometer.

### 3.4.3 Contact pad fabrication

To make to Au contact pads, the sample was coated with S-1818 PR initially. The sample was coated with PR at 4000 rpm spin for 30s. Then, the sample was soft baked for 60 s at 115 °C at hotplate. In mask aligner, the mask was aligned with the marking from the previous marks. After exposure, it was developed with MF 351: DI water (1:1) and using a spin/ stop/ spin/ stop method at 500 rpm for 30

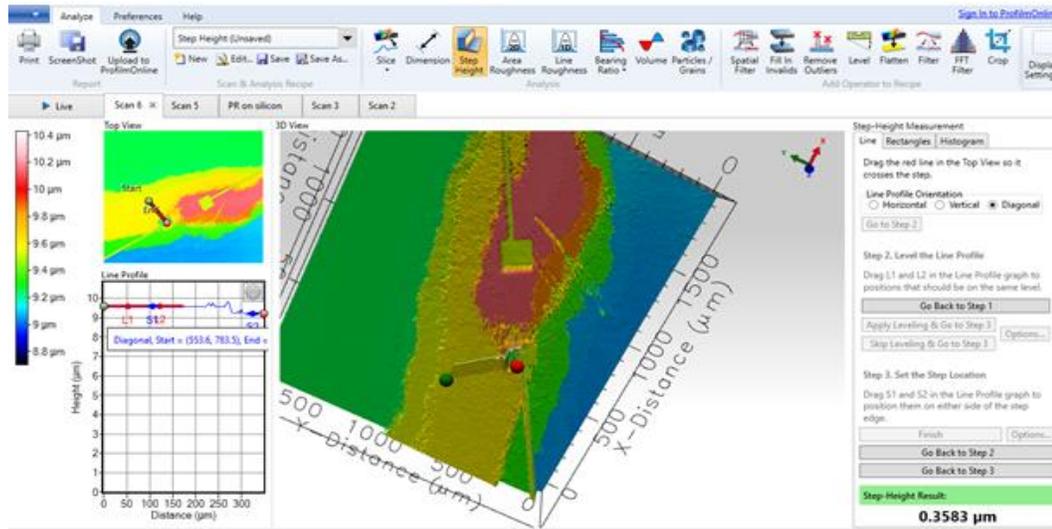
secs each time [33]. Afterwards, it was rinsed with DIW and dried with dry N<sub>2</sub>. E-beam evaporation will be done to deposit 2/100 nm Cr/Au for making the metal contact pads. For removing unwanted metal. Lift-off technique was applied. 1165 remover was kept at 90 °C temperature to heat up. In the meantime, packaging tape was used to lift-off additional metal. Then, the sample was kept in ultrasonic bath in acetone for 5 minutes. The sample was rinsed with acetone, DIW, and dry N<sub>2</sub> at 500 rpm for 30s every time. Then, the sample was dipped into heated remover for 5 minutes. Finally, it was again cleaned with acetone and dry N<sub>2</sub>. Before implementing on original device sample, the whole process was tested on bare silicon wafer to check if it works. Figure 39 shows the SEM image of that.



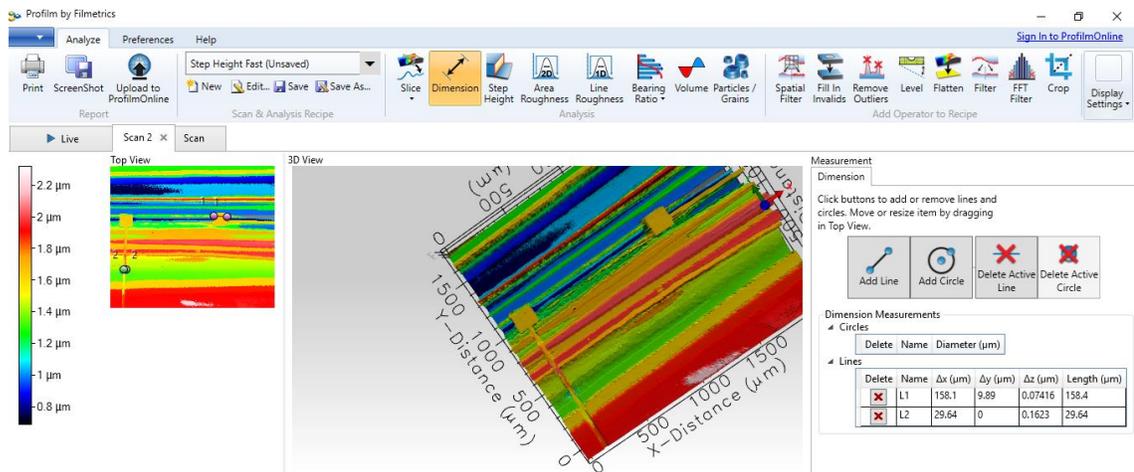
**Figure 31.** Contact pad fabrication process on a dummy wafer.

For contact pad fabrication, the wafer was coated with  $\sim 350\mu\text{m}$  thick photoresist. The contact pads and the connectors were supposed to be  $150\mu\text{m} \times 150\mu\text{m}$  and  $25\mu\text{m}$  thick, respectively. However, after developing the photoresist, we measured these dimensions and found those to be little off than how it should

be. Figure 40 and 41 below shows the photoresist thickness and contact pads dimensions measured with Filmetrics 3D profilometer.



**Figure 32.** Photoresist thickness measurement for contact pad formation.



**Figure 33.** Contact pad measurements.

Strain gauge fabrication and contact pad fabrication falls under front side processing. Figure 34 provides pictorial representation of the entire process.



### 3.4.4 Membrane fabrication

SOI wafers are used for membrane fabrication. A cavity is made in the handle wafer through backside etch up to the buried SiO<sub>2</sub> layer. We divided the membrane fabrication process into photolithography, etching, and plasma cleaning. These are discussed in the following subsections.

#### **Photolithography**

Initially, the SOI wafer was cleaned with a 30 second acetone and isopropyl alcohol (IPA) rinse, a 30 second deionized water (DIW) rinse and dried with pressurized nitrogen. Then, the wafer is coated with a thick positive or negative photoresist, compatible with the fabrication tools. We have used a positive photoresist, SPR 220 for membrane formation. A thick photoresist is needed for the DRIE process as we want deep cavities in our device. We poured SPR 220 PR onto clean wafer. Then, we spin coated it at 2000 rpm for 30 seconds to form 8 μm – 10 μm thick layer. which is enough to etch ~500 μm Si.

As pre-exposure bake, PR coated wafer is placed on a hotplate at 115 °C for 90 seconds. A positive mask or dark field mask was used as the wafer was coated with a positive photoresist (Figure 27). Generally, pre-baking results in approximately 25% decrease in the resist's thickness [61]. Then, the wafer was

exposed to UV – radiation of 365 nm using Karl Suss MA6/BA6 mask aligner. The exposure time and the exposure dose depend on the PRs thickness. Relation between exposure time and the exposure dose is expressed by the following equation:

$$\text{Exposure Dose} = \text{Flux} \times \text{Exposure Time} \quad (17)$$

According to SPR 220 Series resist datasheet, exposure dose is  $\sim 500 \text{ mJ/cm}^2$  and mask aligners mercury lamp g-line wavelength intensity is  $10 \text{ mW/cm}^2$  [62]. Therefore, we exposed our wafer for 50 seconds to achieve  $\sim 10 \mu\text{m}$  thickness.

After 30 minutes, the wafer needs to go through post-exposure step. For this, wafer was placed on hotplate at  $115^\circ\text{C}$  for 90 seconds. The wafer was then developed by 1:5 351 developer and DI water. We agitated the wafer in the developing dish and kept there for 20 minutes. While developing, we need to make sure that the wafer is not getting under or over developed to make sure that the features are not smaller or bigger than the expected size. After that, we moved it to the DI water dish. Even though there is no specific duration for that, the wafer should be kept in DI wafer for at least 4 minutes as SPR 220 is a thick photoresist.

To verify whether we achieved our desired photoresist thickness, we used Alpha-Step IQ surface profilometer to verify photoresist thickness. We measured the thickness at four location on the wafer and then took the average value. From

left to right we found thickness to be 102204 Å, 106805 Å, 106785 Å, and 102243 Å (Figure 35). The average value is 104509.25 Å or 10.45 μm. As we got our desired photoresist thickness, this sample was prepared for etching.

Another approach to fabricate membranes out of SOI membrane is to use negative photoresist. Instead of 1 SPR 220 or AZ 4620, a thick negative photoresist (i.e. SU-8) can be used for DRIE [62]. The wafer should be coated with SU-8 (2050) at 500 rpm for 5-10 seconds with acceleration of 100 rpm/s and at 2000 rpm for 30 secs with acceleration of 300 rpm/s to form a ~25 μm thick coating. For pre-exposure soft baking, the wafer should be kept on hotplate for 2 minutes at 65°C.

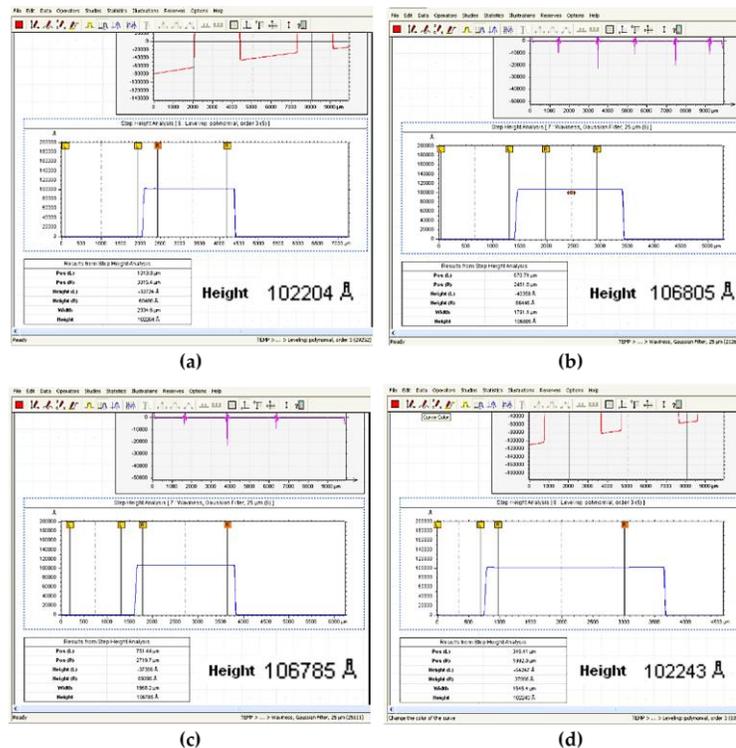
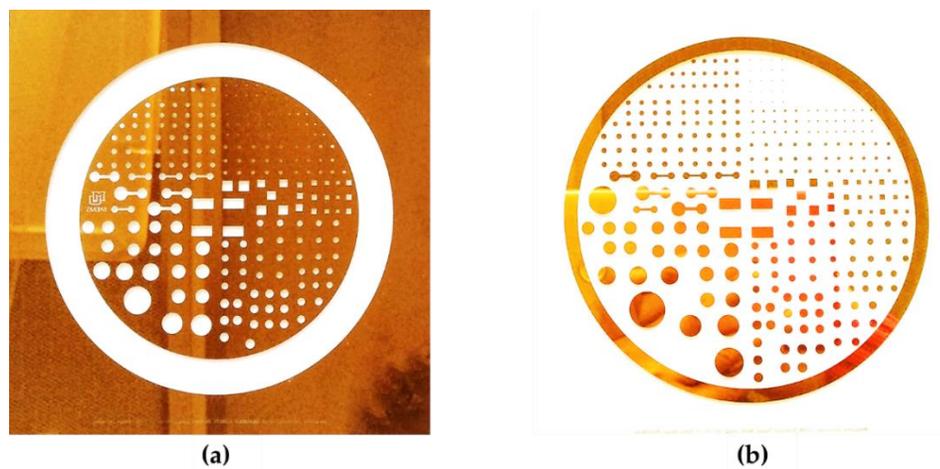


Figure 35. SPR 220 coating thickness; (a) at left end; (b), (c) at middle; (d) at right end.

Then again it was kept at 95 °C for 5 minutes for hard baking. The exposure time should be ~15 seconds to provide an exposure energy of 150-160 mJ/cm<sup>2</sup> according to the SU-8 data sheet [63]. The wafer then must go through post-exposure bake procedure which is same as pre-exposure bake. The wafer can be developed for 4-5 minute using Microchems SU-8 developer [63]. Finally, it should be rinsed in DIW and dried by dry N<sub>2</sub>.

Figure 36 shows dark field and light field masks for positive (i.e. SPR 220) and negative photoresists (i.e. SU-8), respectively.

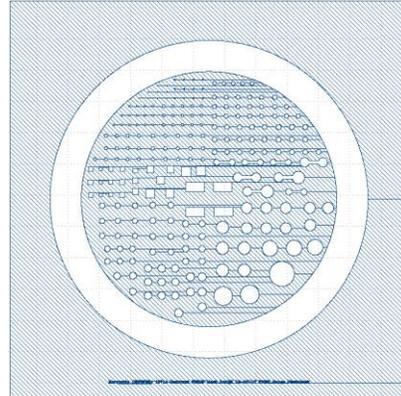


**Figure 36.** Right Reading Chrome Down (RRCD) Mask sets for DRIE; (a) Dark Field (DF) for positive photoresist (e.g.: SPR 220); (b) Light Field (LF) for negative photoresist (e.g.: SU-8).

For the last approach, we used a negative thick photoresist, AZ nLOF 2070. Before pouring the PR onto the sample wafer, we put the wafer in

Hexamethyldisilazane (HMDS) oven at 80°C to 120°C for about 10 minutes to form a HMDS monolayer. Then, we applied the photoresist and spin coated at 4000 rpm with 4000 acceleration for 45s. The wafer was soft baked at 110°C for 1 minute.

We exposed the wafer with 375 nm laser, (~210 mJ/cm<sup>2</sup> dose). In this approach, we did not use any mask as we used The Heidelberg Direct Write Lithography system. We uploaded the .dxf file of mask design to generate a K-layout so that the tool can directly write the design on the wafer (Figure 37). The tool had to write millimeter sized features and took 30 minutes to write down the patterns.



**Figure 37.** K-layout for membrane etching.

As post exposure bake, we kept the wafer on hotplate at 110°C for 1 minute. To develop the wafer, we kept it in AZ 300 MIF developer for 1 min and then rinsed in DI water flow for at least 1 minute.

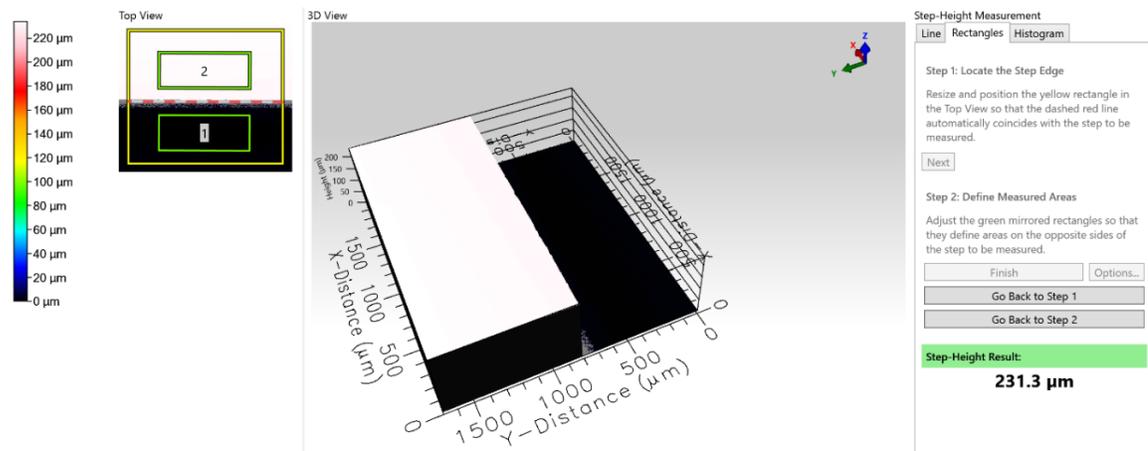
## Etching

For the second lithography approach involving SPR 220, the membranes were etched out using the Nanoscale Fabrication Center's (NFC) ETCH STS Deep Reactive Ion Si Etcher. As we etched deeper than 200  $\mu\text{m}$ , we had to attach the wafer with another dummy/ carrier wafer. Carrier wafer can be thicker than the sample wafer.

For carrier wafer mounting, we poured a small amount of PR S1827 onto carrier Si wafer. While pouring we had to make sure that there is not any PR near 10 mm of wafer's edge. Then, the sample wafer was placed on the PR. Lastly, it was baked for 10 minutes at 90°C. Another way of attaching carrier wafer is crystal bonding. Crystal bond wax 509 is a good option for that. This second approach is more reliable than the first one because it is very likely that the PR might have air bubbles trapped between the gap between two wafers. When the wafers are heated up in DRIE tool due to plasma gas, the trapped air bubbles will try to escape. This can ultimately break the sample and harm the DRIE tool as well.

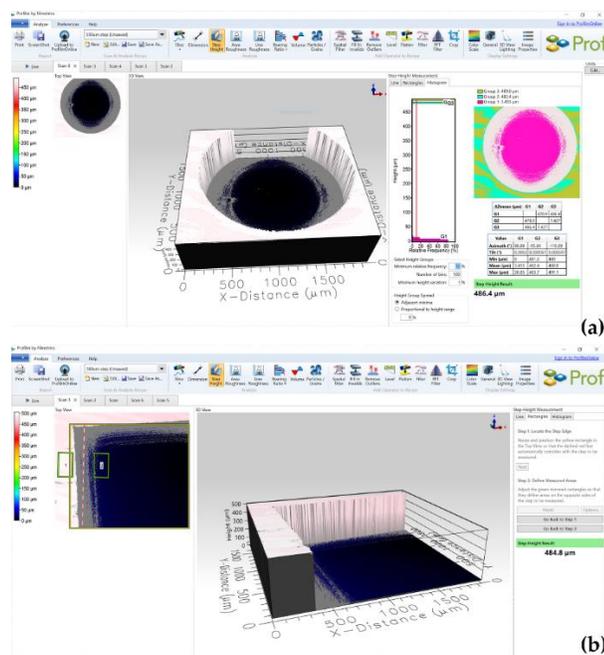
Before putting the wafer into the DRIE tool, we had to check the periphery of wafer so make sure that there is no photoresist on there and it is perfectly clean. Also, there should not be any feature within 10 mm of wafer's edge.

At this point, the sample wafer was ready to be used in DRIE tool. The wafer had to pass the helium leak up rate (He LUR) test. This rate must be  $<8.0$  mT/ min. Otherwise, it won't be processed any further. During the LUR test, we set the etch time. The etch time depends on the tools etch rate, required cavity depth, and the samples material. We needed to etch  $\sim 500\mu\text{m}$ . To find out the tools etch rate for our sample, initially we set 1 hour 55 minutes as etch time. After 2 hours, we took out the sample, removed the PR and measured the cavity depth using Filmetrics Profilm3D profilometer. The difference between cavity's surface and wafer's surface was determined by step height measurement and it was found to be  $231.3\mu\text{m}$ . This indicates that the tools etch rate is  $\sim 2.3\mu\text{m}/\text{min}$  (Figure 42).

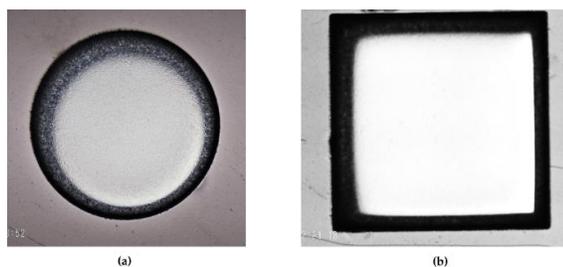


**Figure 38.** Image taken using optical profilometer after performing Deep reactive ion etching (DRIE) on SPR 220 coated wafers to verify cavity depth.

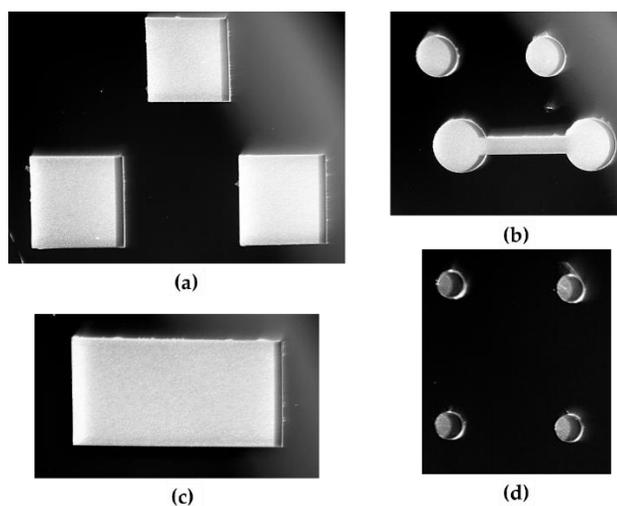
As we know the etch rate now, we again prepared a sample as before, and set the etch time 4 hours for producing the membrane. This time the membrane structure was released. Figure 39 shows our device's cavity depth. Figure 40, 41, and 42 shows microscopic images of our fabricated membranes.



**Figure 39.** Image taken using optical profilometer after completing 500 cycles of Deep reactive ion etching (DRIE) process on SPR 220 coated wafers.



**Figure 40.** Deep reactive ion etching (DRIE) is performed on SPR 220 coated wafers; (a) circular membrane; (b) square membrane.



**Figure 41.** Microscopic images of various membranes; (a) Square; (b) Circular & Dumbbell; (c) Rectangular; (c) Circular membrane.



**Figure 42.** Microscopic image of membrane cavity.

However, few smaller circular membranes were not as perfect as we expected. Etching in those portions of wafer were not good enough. These devices are located at the wafer's periphery region. So, photoresist removal from the

pattern might be insufficient over there. Figure below shows membranes that were designed to 0.2mm diameter circle.

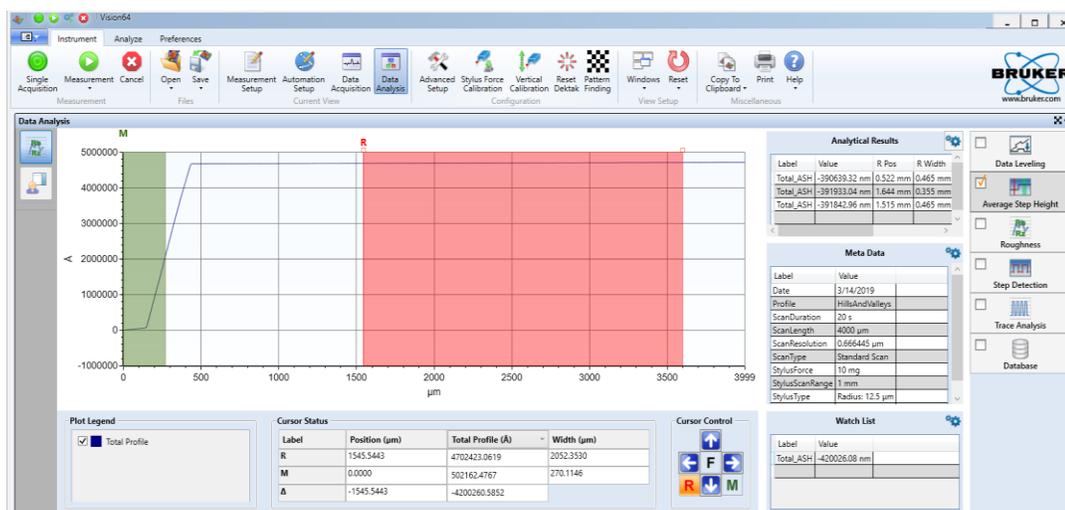


**Figure 43.** Microscopic image of imperfect devices.

For the third lithography approach (involving AZ nLOF 2070), we used The Plasma-Therm Versaline DSE (Deep Silicon Etcher) from Pritzker Nanofabrication Facility. Before putting our sample wafer onto the load lock, we mounted that to a 4-inch carrier wafer as we will etch through. There are four ways to mount the sample to the carrier wafer. These are: Fomblin oil, crystal wax, photoresist, double sided black tape. We used small amount of Fomblin oil to attach the wafers.

At this point we vented the load lock and put a dummy clean wafer. Then, we ran the O<sub>2</sub> clean recipe to plasma clean the chamber. After unloading the dummy wafer, we put our sample and carrier wafer and run 800 cycles for 80 minutes. After 800 cycles, the load lock vented automatically, and we removed our

wafers from load lock. To find the etch rate, we put our sample in Bruker Dimension Icon AFM profilometer. We figured out that we etched  $464 \mu\text{m}$  in 800 cycles. This means that the etch rate was  $\sim 5.8 \mu\text{m}/\text{min}$ .



**Figure 44.** Etch depth analysis using AFM profilometer after performing Deep reactive ion etching (DRIE) on AZ nLOF 2070 coated wafers.

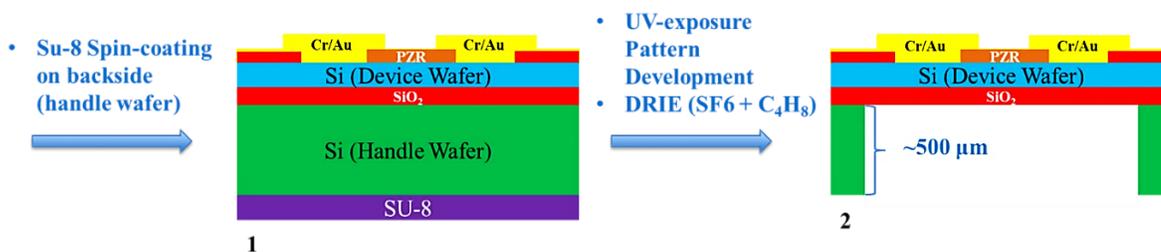
## Sample Cleaning

After etching, we followed two approaches to clean the sample. These are PR removers and plasma cleaning. We applied both procedures to clean our samples. For the first approach, we removed the remaining PR using acetone and then by Microposit remover 1165 at  $75 \text{ }^\circ\text{C}$ .

A better approach is to use O<sub>2</sub> Plasma Asher Descum cleaning. For the second approach, we used YES PLASMA ASHER from NFC. This tool runs two cycles: descum and stripping. 5 s – 15 s is enough for the prior step. The latter one requires more time and it greatly depends on PR type. However, 30 minutes is enough for any kind of PR. As SPR 220 is a thick PR and it hard to remove, we kept it in the tool for 30 minutes.

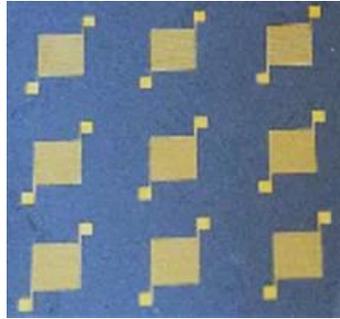
For the third approach, we placed our sample to the YES CV200 RFS Plasma Strip / Descum System and we kept the sample at 22°C with 200W, 60 sccm O<sub>2</sub> for 25 s. This recipe can remove 10-15 nm of photoresist.

As we are etching the backside (handle layer) of the SOI wafer, membrane formation can also be called as backside processing. Figure 45 explains the backside processing.



**Figure 45.** Backside processing.

Figure 46 shows complete devices within a SOI wafer.

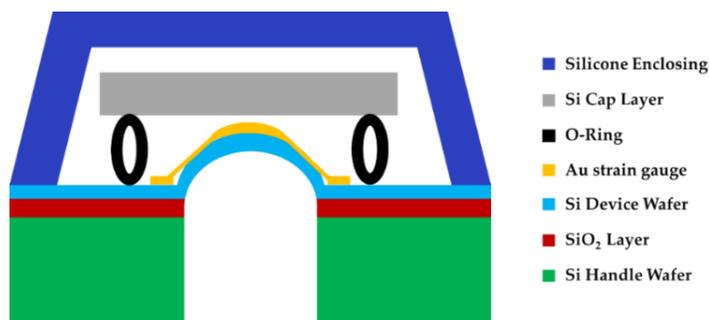


**Figure 46.** SOI wafer containing several membranes.

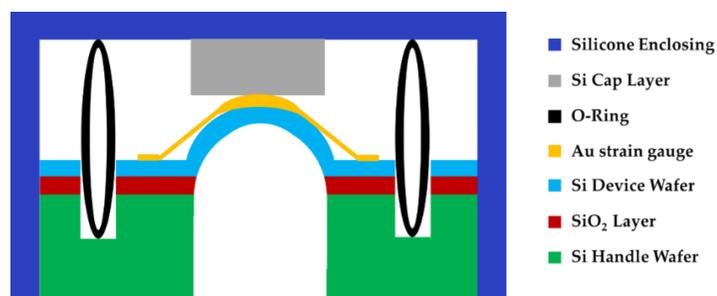
### 3.5 Waterproof Packaging

Packaging for the water environment is a very difficult problem and was studied extensively in this project. Waterproof Packaging was done in a way to avoid shorting out. Moreover, we kept the contact pads out even after packaging for additional lab testing. We have considered three novel packaging approaches as illustrated in Figures 47-49. All three approaches are simple and very low-cost. The Figure 47 approach is based on using an O-ring and a capping piece of Si. Figure 48 approach is based on inserting an O-ring into a pre-etched pair of encircling trenches around the membrane. This approach reduces cavity volume above the membrane and provides a “hard stop” to fully deflected membranes. Figure 49 is based on using a 3D printed capping box as the protective structure.

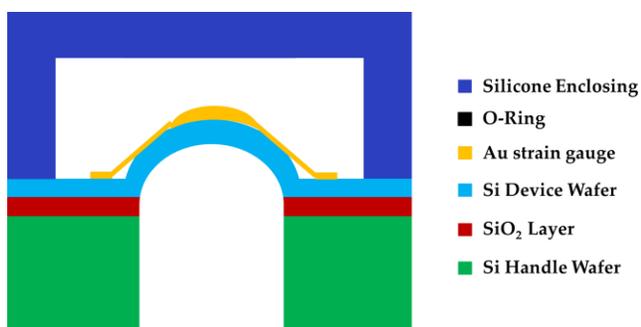
Small (4 mm x 4 mm) 3D printed box covers have been prototyped using a FlashForge Creator Pro 3D printer.



**Figure 47.** A packaged device using O-rings and a capping Si layer.



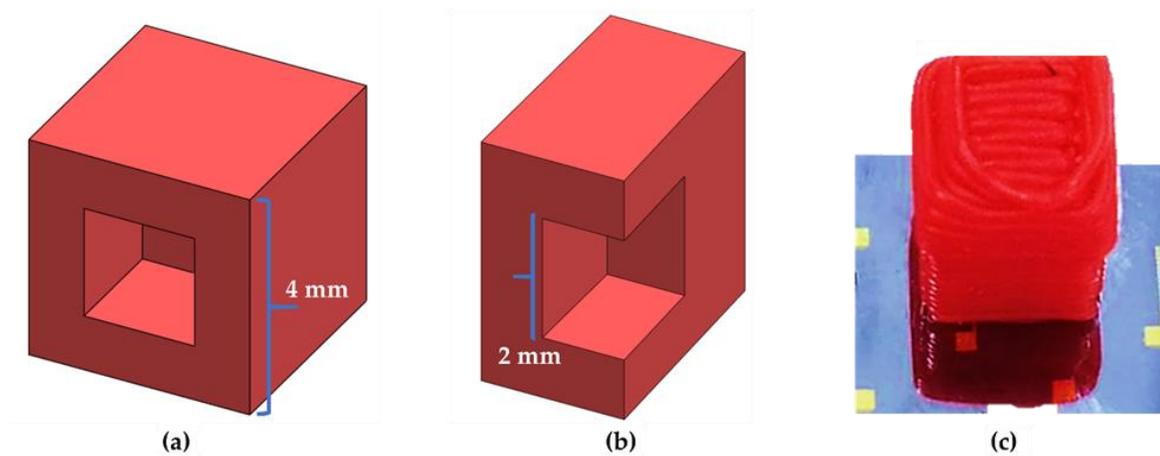
**Figure 48.** A packaged device using “embedded” O-rings and a capping Si layer.



**Figure 49.** A packaged device using a 3D printed mm-scale box that is placed on top of the membrane.

We have implemented the third approach like Figure 49 as cost-effective and reliable packaging for water environment usage. We designed a  $4 \times 4 \times 4 \text{ mm}^3$  cap using SolidWorks “parts” module. The cap has  $2 \times 2 \times 2 \text{ mm}^3$  cavity. 2 mm depth would give the membrane enough space to expand within it. After 3-D drawing in SolidWorks, we converted it to a .stl format. Then, we uploaded this .stl file to ReplicatorG – Sailfish software to generate the g-code for this. We had to set some parameters in the software based on the design. Even though 10% infill and 1 shell layer is enough for such small structure, we used 20% infill and 2 shell layers to make it waterproof. Values and parameters are shown in Table III. Beside this, we also generated a .x3g file of the design. Both of these files (i.e. g-code and .x3g file) could be used for printing the cap. Among various commercially available 3D printer filaments (i.e. PLA, Nylon, PC, etc.), we chose Acrylonitrile Butadiene Styrene (ABS) filament for its high mechanical strength and high melting point. We measured the filament’s diameter with digital calipers and put this value in ReplicatorG. In ReplicatorG, we must make sure that the object lies on the platform and the cavity should not be up or down faced. This can make the cavity’s boundaries uneven and therefore it will not seat onto the device properly. The Settings dialogue in ReplicatorG allows to change the way 3D printer will print a model [64]. The 3D printer needs to be connected with the operating computer to print the structure from g-code. However, for higher resolution, we

copied the .x3g file to a memory card dedicated for the printer and then printed the cap. The cap was 3D printed using FlashForge Creator Pro 3D printer. It took only 5 minutes to heat up the printer's nozzle and completing the printing. After printing, the cap was attached on top of the membrane using epoxy. We used Loctite Professional Liquid Super Glue to mount the cap onto the device (Figure 50). This approach is a cost effective one and it does not increase the device's mass much. Table II shows the parameters that we used for printing the cap.



**Figure 50.** (a) SolidWorks 3D model; (b) Cross sectional view of SolidWorks 3D model; (c) 3-D printed packaging cap.

TABLE II  
PRINT SETTINGS FOR GENERATING GCODE FOR THE WATERPROOF CAP

Settings	VALUE	Unit
Object Infill	20	%
Layer Height	0.08	mm
Number of shells	2	
Feed Rate	60	mm/s
Travel Feed Rate	80	mm/s
Filament Diameter	1.84	mm
Nozzle Diameter	0.4	mm
Platform Temperature	110	°C
Print Temperature	220	°C

### 3.6 Finite Element Analysis Methods

In this research, Finite Element Analysis (FEA) simulation has been done to investigate the mechanical responses of the Si membrane using SolidWorks mechanical simulation module. These FEA simulations helped us to understand the effect of membrane's geometry on its sensitivity and reliability. The parameters

involved in the simulation are membrane thickness, area and physical properties of device materials. These parameters directly affect the burst load, as well as, device sensitivity under uniform loading [43]. SolidWorks Simulation is a design analysis software and it is entirely integrated in SolidWorks [44]. This chapter discusses about Finite Element Method (FEM), Finite Element Analysis (FEA), membrane deflection/ displacement, stress, strain theories and simulation results for deflection, stress and strain for different membrane shapes with different materials at different temperature conditions. Also, we will verify if our FEA simulation results are in accord with the theories and expected results.

### *3.6.1 Finite Element Method (FEM)*

The Finite Element Method (FEM) is one of the most widely used numerical analysis tool for engineers because it is more flexible than other previous approaches. Its key advantage is that it can be applied to arbitrary shapes in any number of dimensions. Even the shapes can be made of any number of materials. Depending on the location and direction, the material properties can be non-homogeneous and/or anisotropic. It allows a wide range of common geometrical supports/ fixtures and external loads (i.e. force, pressure, torque, gravity, temperature, heat flux, etc.). The FEM offers a general method of converting

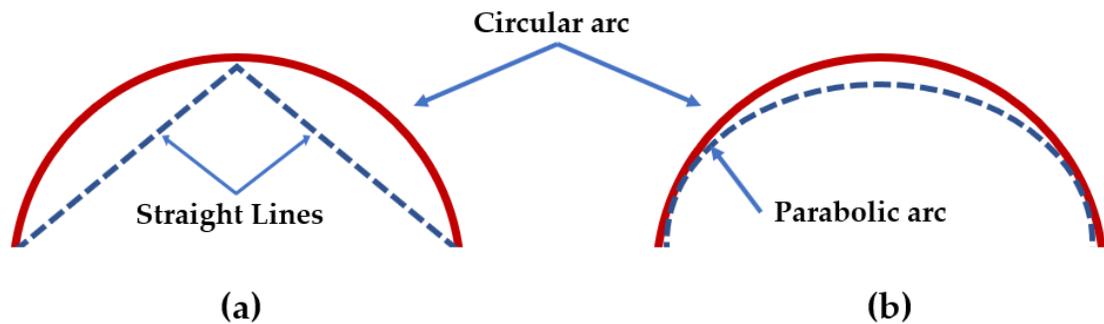
leading energy principles or leading differential equations into a matrix equation system for solving an estimated solution. Thus, nearly exact solutions for linear problems can be found very quickly. Being that done, the FEM provides additional procedures for follow up calculations like finding the solution's integral, or its derivatives at different points [45].

### 3.6.2 *Finite Element Analysis (FEA)*

When the Finite Element Method (FEM) is applied to a specific field of analysis (i.e. displacement analysis, stress analysis, strain analysis, thermal analysis, or vibration analysis) it is then called as Finite Element Analysis (FEA). This is the most popular tool for mechanical analysis. Here, several study fields are linked. For example, non-uniform temperature distribution brings non-obvious loading conditions on solid structures. Thus, it is common to conduct a thermal FEA to attain temperature results which in turn become input data for a stress FEA. Moreover, FEA can obtain input data from other tools like motion analysis systems and fluid dynamics systems [43,45].

An integral evaluation for an FEA needs a mesh. The finite element mesh result forms minimum two data sets: nodal set and element set. The nodal set is the

numbered list of all the vertices along with their spatial coordinates. The element set is the numbered set of elements along with the list of element vertex numbers to which it is connected. Usually, it is triangular mesh and tetrahedral mesh designs are used for surfaces and solids, respectively. Even though parabola segments pass through three points lying just on the boundary curve, they often convert to straight lines in the interior. This rises an unavoidable geometrical boundary error when circular or arc shapes are involved (Figure 51). The only way to mitigate is to use smaller mesh [45].



**Figure 51.** Mesh elements cannot match circular shapes; (a) Linear mesh element; (b) parabolic mesh element.

For performing FEA, we have used SolidWorks simulation module. The SolidWorks simulation module offers a wide range of linear studies including: Static, Thermal, Buckling, Drop Test, Dynamic Analysis, Fatigue, Frequency, Harmonic Analysis, Optimization, Modal Time History, Pressure Vessel Design,

Random Vibration, and Transient Thermal. We have used Static studies for our research.

### 3.6.3 *Static Studies*

Static studies allow to analyze displacements, reaction forces, strains, stresses, failure criterion, factor of safety, and error estimates. Existing loading conditions are point, line, surface, acceleration and thermal loads. This software has options to provide force, torque, gravity, bearing load and temperature as external load.

Design analysis of the membranes has been done to design better, safer, and cheaper products [43]. SolidWorks "PARTS" documents were created for setting geometrical parameters of the burst disks. The mechanical simulation module allows static analysis by which stresses, strains, displacements, and reaction forces in the model can be calculated. While keeping the faces and edges connected to substrate fixed, pressure was applied on free membrane surface. Then meshing was done where the simulation model was subdivided into many small pieces of simple shapes called elements. After giving "Run" command, stress, strain and displacement results were found. General description of the state of stress was given in a scale of von Mises stress number. It gives an overall idea about the state of stresses at a certain location [44].

### 3.6.4 Membrane deflection

According to Timoshenko *et. al*, the maximum displacement of rectangular membrane symmetrical in  $R_M$  clamped at all four edges is given by [46],

$$w_o = 0.318 l^3 \sqrt{\frac{Pa_M}{Ed_M}} \quad (18)$$

where,  $w_o$  is the maximum deflection at the center,  $P$  is the applied pressure,  $a_M$  is the membrane's length,  $E$  is Young's modulus and  $d_M$  is the membrane's thickness.

The relation between burst pressure or pressure drop at membrane surface with deflection relies on both membrane area and thickness. This relationship for square and circular membrane is given below [34]:

$$\text{Square Membrane:} \quad w_o = \frac{1}{66} \frac{a_M^4}{d_M^3} \frac{1-v_M^2}{E_M} \Delta P \quad (19)$$

$$\text{Circular Membrane:} \quad w_o = \frac{3}{16} \frac{R_M^4}{d_M^3} \frac{1-v_M^2}{E_M} \Delta P \quad (20)$$

Equation (9) and (10) indicate that membrane deflection is directly proportional to membrane's area and applied pressure. Also, it is inversely proportional to membrane's thickness.

### 3.6.5 Membrane stress

A thin membrane's stress ( $\sigma_M$ ) is comprised of two parts, the residual stress  $\sigma_o$  and the deflection stress  $\sigma_D$  [34]. Residual stress is always present even if there is no deflection and deflection stress occur due to the membrane's deflection. As deflection of thin membranes is large compared to its thickness, the central plane of the membrane expands like a balloon which results in deflection stress.  $\sigma_o$  is always positive, regardless to the direction of force but  $\sigma_D$  can be either positive (pressure at front) or negative (pressure at back). This effect seems lower when pressure is applied on the face having piezoresistors on it. For the opposite case, ballooning effect is very high [4]. Thin membrane's stress ( $\sigma_M$ ) can be expressed as [34,47],

$$\sigma_M = \sigma_o + \sigma_D \quad (21)$$

$$\text{Square Membrane:} \quad \sigma_M = 0.29 \left(1 + \frac{1.47}{0.37}\right)^3 \sqrt{\frac{p^2 a_M^2 E_M}{h^2}} \quad (22)$$

$$\text{Circular Membrane:} \quad \sigma_M = \sigma_o + \frac{2}{3} \frac{w_o^2}{R_M^2} \frac{E_M}{(1-\nu_M)} \quad (23)$$

here, square membrane's edge length  $a_M$ , circular membranes radius is  $R_M$ , thickness  $h$ , Young's modulus  $E_M$ , Poisson's ratio  $\nu_M$ , residual stress  $\sigma_o$ , and deflection at center  $w_o$ .

Deflection stress ( $\sigma_D$ ) depends on radial strain ( $\epsilon_R$ ) and tangential strain ( $\epsilon_T$ ) generated by the deflection. According to Hooke's law, the radial strain is expressed as [34],

$$\epsilon_R = \frac{1}{E_M} (\sigma_R - \nu_M \sigma_T) \quad (24)$$

Likewise, tangential strain ( $\epsilon_T$ ) is calculated as,

$$\epsilon_T = \frac{1}{E_M} (\sigma_T - \nu_M \sigma_R) \quad (25)$$

Radial strain is assumed to be constant over the entire membrane. This is satisfactory for thin membranes only because bending moments are relatively small and may be neglected in thin membranes. Therefore, strain for a thin circular membrane is expressed as,

$$\epsilon \approx \frac{2}{3} \frac{w_0^2}{R_M^2} \quad (26)$$

## 3.7 Experimental Setup

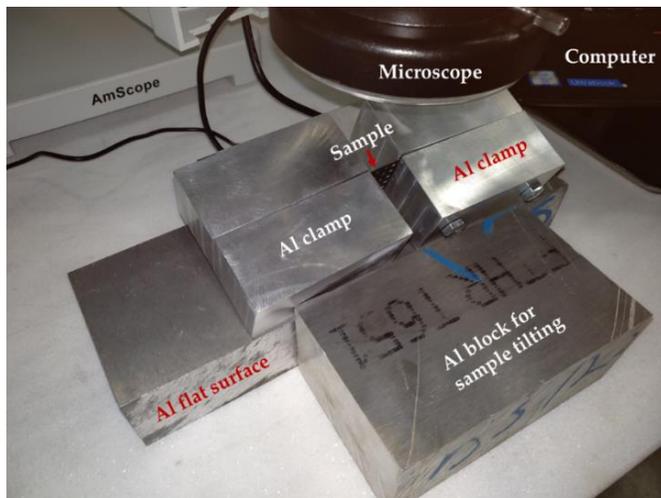
This section discusses about experimental setups for mechanical and electrical characterization of our devices.

### *3.7.1 Setup for Mechanical characterization*

For burst pressure testing involving N<sub>2</sub> gas and water, we considered two test fixture model. The first one is made of aluminum and the second one is 3D printed.

In the first approach, we took a 16 inch x 3 inch x 2.5 inch aluminum slab as horizontal smooth surface. On top of it, two 3 inch x 3 inch x 2.74 inch Al made clamps were placed. Each clamp consists of two 3 inch x 3 inch x 1.37 inch Al blocks. These blocks are connected by 2 screws of 0.2 inch diameter. For burst pressure testing, screws of the clamps are loosened, and the sample was be placed in the gap between. Screws should be tightened up to hold the sample. The sample with clamps were tilted by placing them together on different sized smaller Al blocks. This approach works well for dry N<sub>2</sub> pressure testing. Dry N<sub>2</sub> gas pressure was applied at the backside of a specific membrane/ burst disk. Above all a microscope was placed. This microscope is attached with a 3-megapixel digital

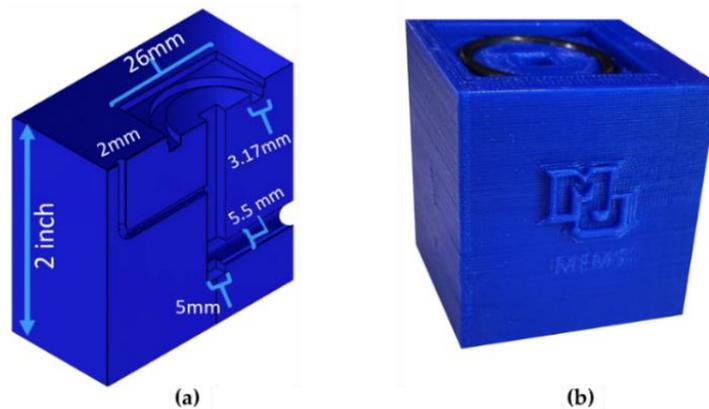
camera by which we were able to see the membrane deflection before it bursts. The camera attached with microscope is operated by AmScope software. The tilt helped us to notice the deflection clearly. An adjustable pressure regulator between the dry N<sub>2</sub> gas source and the setup is used to regulate the pressure applied to the sample. Figure 52 shows the experimental setup for this approach.



**Figure 52.** An experimental setup for holding samples in place while applying pressurized N<sub>2</sub> to the back of a membrane during deflection analysis using microscope.

A specialized test fixture for both dry N<sub>2</sub> gas and water pressure testing was designed using SolidWorks parts module. The test fixture is a 1.5 inch cubic structure with an inlet of 5.5mm and 5mm square outlet on which a single membrane/ burst disk will fit. A 2mm narrow pipe is designed to get rid of unwanted air pressure which might affect the actual result. For setting a 1 inch x 1

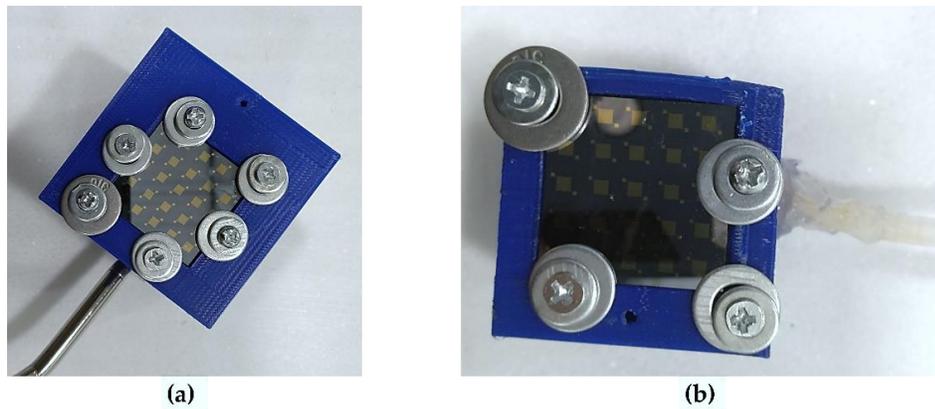
inch dice, a groove was made for fitting an O-ring of 20mm diameter and an opening of 26mm x 26mm was made. The O-ring helps the device to be seated properly. It helps to prevent gas and water leakage from the test fixture, which in turn maintains the pressure help us to determine burst pressure of the membranes/ burst disks. Washers are used to apply targeted pressure. Also, these will keep the device in place even at high pressure. Figure 53 shows the 3D printed test fixture.



**Figure 53.** (a) Cross sectional view of SolidWorks 3D model; (b) 3D printed test fixture.

The Gcode and 3D printable .x3g format of the design was generated using ReplicatorG – Sailfish software and then the test fixture was 3D printed with FlashForge Creator Pro 3D printer. Table III shows the settings used for our model. ABS filament was used to make sure that the test fixture is sturdy, waterproof and long lasting [65]. It took 2 hours and 33 minutes to print for its large size. The

filament and the parameters should be carefully selected. Otherwise, the test fixture's base will be buckled and there will be gaps which will cause gas/ water leakage. Figure 48 shows cross-sectional view of the SolidWorks model and 3D printed test fixture for this work. An adjustable pressure regulator and a minipump were used for applying  $N_2$  gas and water pressure. Figure 54 shows this experimental setup.



**Figure 54.** Burst pressure test setup with 3D printed test fixture involving (a)  $N_2$  gas; (b) water.

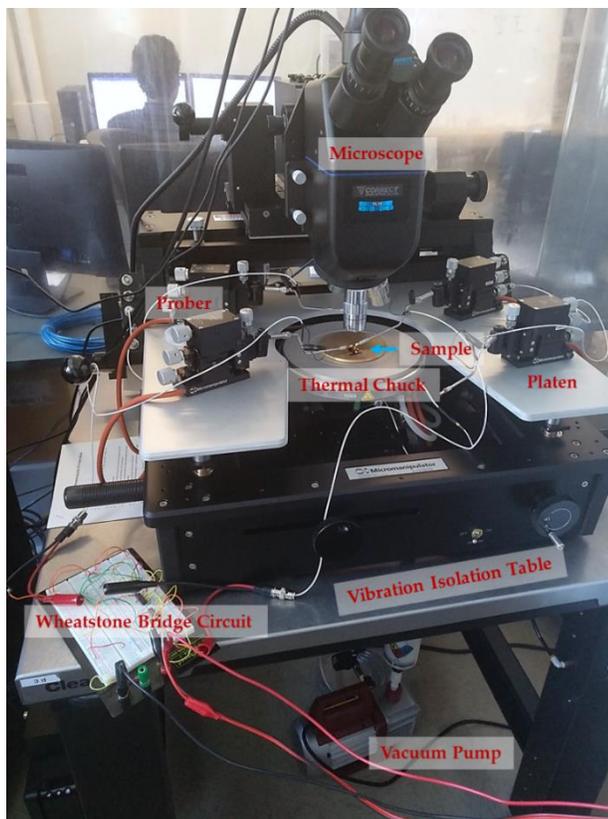
TABLE III  
PRINT SETTINGS FOR GENERATING GCODE FOR TEST FIXTURE

Settings	VALUE	Unit
Object Infill	40	%
Layer Height	0.08	mm
Number of shells	3	
Feed Rate	60	mm/s
Travel Feed Rate	180	mm/s
Filament Diameter	1.73	mm
Nozzle Diameter	0.4	mm
Platform Temperature	110	°C
Print Temperature	230	°C

### 3.7.2 Setup for Electrical characterization

To analyze membrane's behavior at elevated temperature, the sample was placed on the Micromanipulator DC probe station's thermal chuck. Temperature of the thermal stage was increased via heating module. A Wheatstone bridge circuit is connected to the probers for resistance measurement. Agilent U3606B served as multimeter and DC power supply for the Wheatstone bridge circuit. The sample and probers were held in position with vacuum pump.

The attached heat control temperature module and cooling module were utilized to set desired temperature values for chuck. C1000 Heat Exchanger is used to rapidly reduce the chuck temperature. A parameter analyzer was connected to the DC probe station's SMU-1 (sample connection) and SMU-3 (drain connection) terminals. A dedicated 15-megapixel "iCamPlus" camera and a monitor were connected to the microscope for viewing the sample. "S-Eye" application is used to control the camera and performing image measurements. A 150-Watt Fiber Optic Illuminator was incorporated for supplying enough light to see the sample through the microscope and camera. Also, a keyboard was attached with parameter analyzer for command insertion. The DC probe station was placed on a vibration isolation table. The entire system was placed in a class-100 cleanroom. Figure 55 shows this experimental setup.



**Figure 55.** Electrical testing setup.

As the membranes deflects, resistivity of the strain gauge was measured using Wheatstone bridge circuits. Wheatstone bridge circuits were built to precisely measure the resistance change for applied pressure and temperature for membranes with different geometrical features (Figure 56, 57).

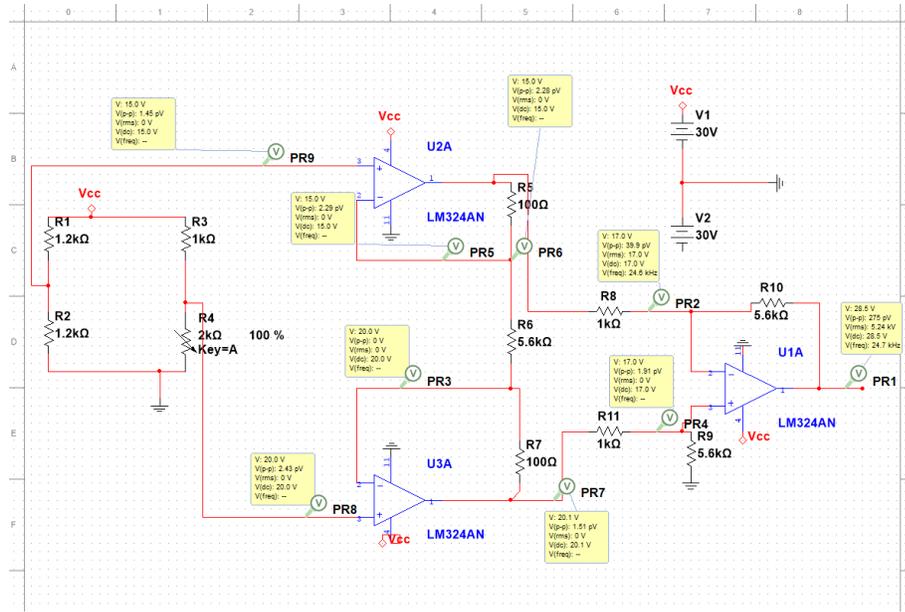


Figure 56. Wheatstone bridge circuit configuration.

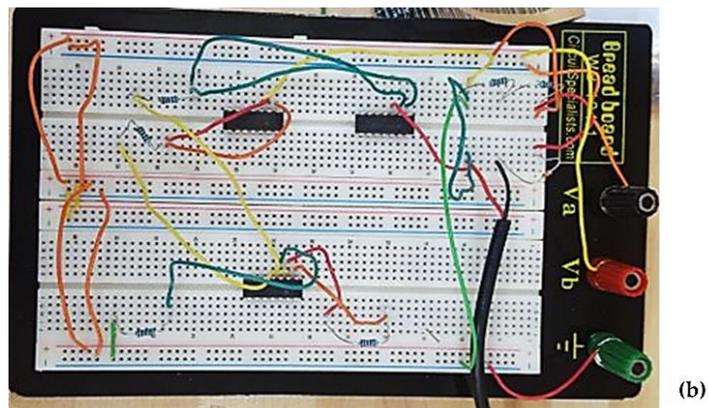
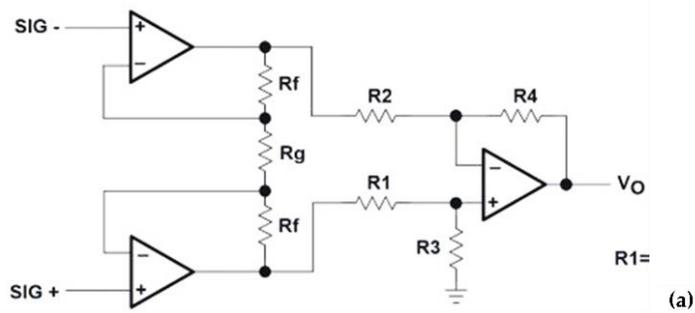
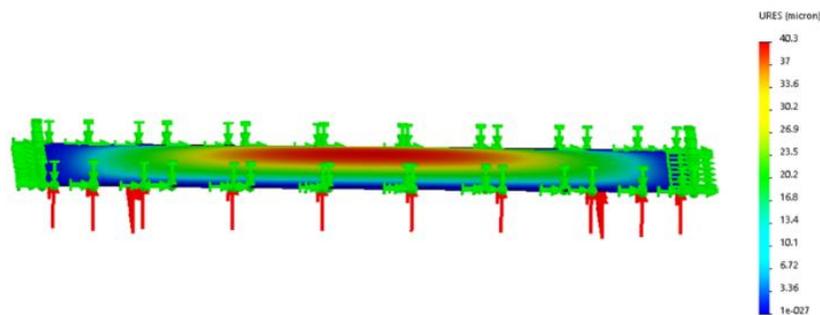


Figure 57. Wheatstone bridge circuit configuration.

## IV. Results

### 4.1 Finite Element Analysis Results

We have performed FEA for various membrane shapes (i.e. square, circular, rectangular and dumbbell). Simulations for deflection analysis were done for different shapes along with various combinations of area and thickness. Deflection was measured using optical interferometer for rectangular disks of area 1mm x 1mm, 1.5mm x 1.5mm and 2mm x 2mm with thickness 6 $\mu$ m for a pressure range 0-10 psi. These experimental results were compared to simulated results to make sure that they are in accord. Here, simulations were done for wafer of Si (100) plane. We fixed the membrane's boundary face and edges. We loaded the membrane with distributed pressure. The physical parameters are given in Table IV. Figure 58 shows fixture and pressure direction for membrane SolidWorks simulation.



**Figure 58.** Fixture and Pressure direction for Rectangular membrane.

TABLE IV  
PHYSICAL PROPERTIES OF Si (100) MEMBRANE

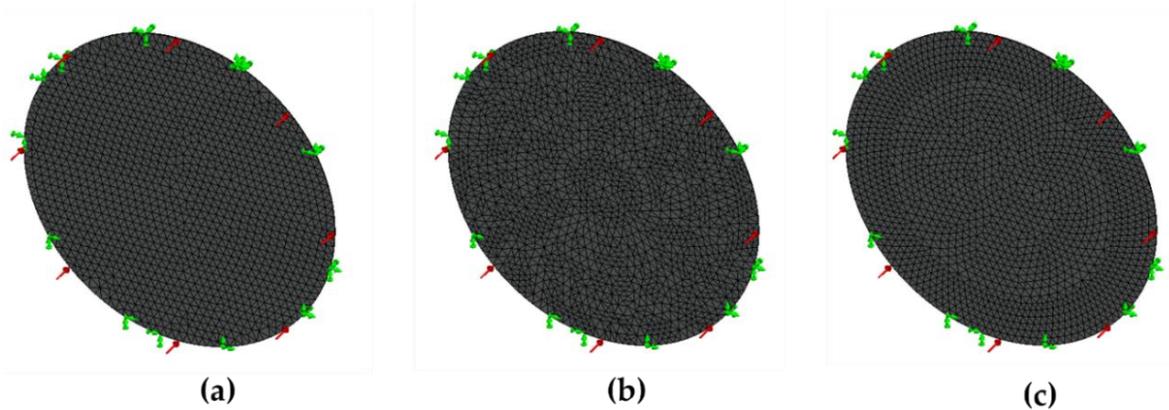
Property	Value	Unit
Elastic modulus	62	GPa
Poisson's Ratio	0.278	
Density	2.328	gcm <sup>-3</sup>
Thermal Conductivity	1.5	W/(cm*K)
Shear Modulus	64.1	GPa
Thermal Expansion Coefficient	1.44 x 10 <sup>-6</sup>	/°F
Yield Strength	0.91	

$P_{\max} = 100$  PSI, thickness  $\sim 6-30$   $\mu\text{m}$ , Area  $\sim 3 \times 3$  mm<sup>2</sup>

SolidWorks offers three types of mesh of mesh parameters: standard, curvature-based mesh and blended curvature-based mesh. We performed FEA for all three with different mesh densities (i.e. coarse, moderate, fine) to determine the differences in results. Table V shows the maximum and minimum element sizes for these three mesh densities. Figure 59 shows mesh plot for these combinations.

TABLE V  
MESH PROPERTIES Si (100) MEMBRANE

Mesh Parameter	Mesh Densities	Maximum element size (mm)	Minimum element sizes (mm)
Standard	Coarse	0.10056548 (Global Size)	0.00502827 (Tolerance)
	Moderate	0.05279688 (Global Size)	0.00263984 (Tolerance)
	Fine	0.02514137 (Global Size)	0.00125707 (Tolerance)
Curvature-based Mesh	Coarse	0.10056548	0.02514137
	Moderate	0.05028274	0.02514137
	Fine	0.02514137	0.02514137
Blended Curvature-based Mesh	Coarse	0.10056548	0.02514137
	Moderate	0.05028274	0.02514137
	Fine	0.02514137	0.02514137



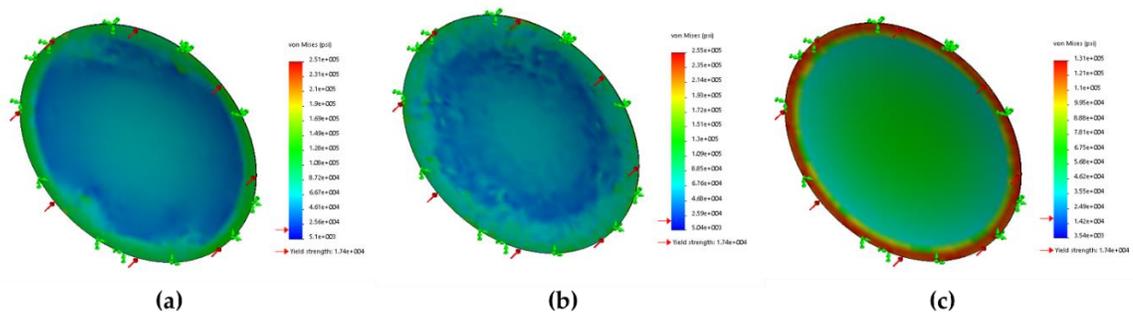
**Figure 59.** Various mesh parameters on a circular membrane for moderate mesh density; (a) Standard; (b) Curvature-based Mesh; (c) Blended Curvature-based Mesh.

From Figure 59, we can see that unlike the prior two parameters, the third one put smaller mesh elements at the maximum stress regions. Even though curvature-based mesh works good for round features, blended curvature-based mesh ensures better details and creates minimum mesh element size suitable for the geometry. We performed deflection and stress simulations for all these mesh parameter combinations to understand their effect on the results. We considered a 6  $\mu\text{m}$  thick circular membrane with 2 mm diameter. Table VI shows the deflection and stress values for the different conditions.

TABLE VI  
MAXIMUM DEFLECTION & MAXIMUM STRESS FOR VARIOUS MESH PROPERTIES

Mesh Parameter	Mesh Densities	Maximum Deflection ( $\mu\text{m}$ )	Maximum Stress ( $\mu\text{m}$ )
Standard	Coarse	68.7	$2.51 \times 10^5$
	Moderate	69.5	$1.98 \times 10^5$
	Fine	69.8	$2.33 \times 10^5$
Curvature-based Mesh	Coarse	68.5	$2.55 \times 10^5$
	Moderate	69.4	$2.13 \times 10^5$
	Fine	69.8	$2.40 \times 10^5$
Blended Curvature-based Mesh	Coarse	69	$1.31 \times 10^5$
	Moderate	69.6	$1.76 \times 10^5$
	Fine	69.8	$2.23 \times 10^5$

Table VI shows maximum deflection and maximum stress results for different mesh conditions. We noticed that deflection did not vary much for all those cases. However, maximum stress results for blended curvature-based mesh were much smaller than the other two mesh parameters. Figure 23 shows stress analysis for all three mesh parameters for coarse density. It shows that even at coarse density, blended curvature-based mesh resulted much better mesh profile than the other two. Consequently, we concluded that blended curvature-based mesh results are more accurate as here smaller and denser mesh elements are used in higher stress regions (i.e. fixed regions). Therefore, we used blended curvature-based mesh for all our simulations.

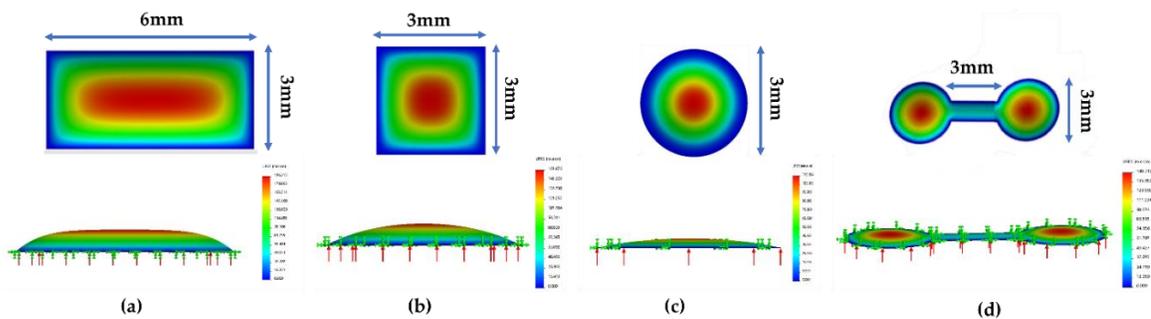


**Figure 60.** Stress analysis of a  $2\text{mm} \times 2\text{mm} \times 6\mu\text{m}$  Si membrane considering various mesh parameters and coarse mesh density; (a) Standard; (b) Curvature-based Mesh; (c) Blended Curvature-based Mesh.

#### 4.1.1 Effect of shape on membrane's deflection

To understand how membranes shape affects its sensitivity, we considered various shapes like circular, square, dumbbell and rectangular shaped membranes.

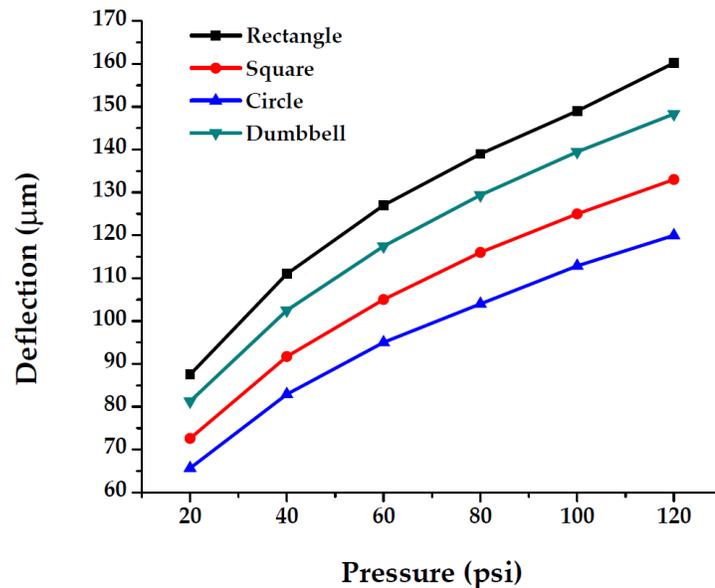
We did FEA simulation studies for observing maximum deflection at 0-120 psi pressure on 3mmx3mmx6 $\mu$ m square membrane, 3mmx6mmx6 $\mu$ m rectangular membrane, circular membrane of 3mm diameter with 6 $\mu$ m thickness, and dumbbell shape membrane with 3mm diameter having 3 mm distance between the arcs. Figure 61 shows deflection analysis of these membranes.



**Figure 61.** FEA for determining maximum deflection of membranes having various shapes and sizes.

Figure 62 shows the maximum deflection results for these membrane geometries. Maximum deflection of rectangular, square, circular and dumbbell

shaped membranes at 120 psi are 160.21 $\mu\text{m}$ , 133 $\mu\text{m}$ , 119.98 $\mu\text{m}$ , and 148.312 $\mu\text{m}$ . The results indicate that rectangular membranes are more sensitive to pressure than other shapes. Dumbbell shape is also a good candidate for pressure sensitive membrane. However, we need to keep a balance between membranes sensitivity and robustness to use it for a wide pressure range. Therefore, membrane's stress analysis is also important.

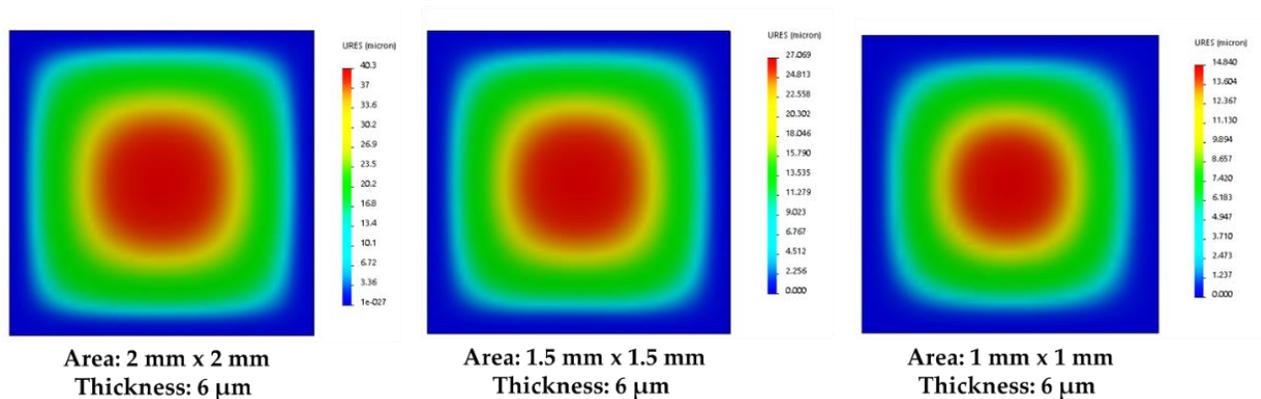


**Figure 62.** Effect of shape on membrane's deflection.

#### 4.1.2 Effect of size on membrane's deflection

To analyze the effect of membrane's size on its performance, we have considered square membranes of 1mm x 1mm, 1.5mm x 1.5mm and 2mm x 2mm

with thickness  $6\mu\text{m}$  for SolidWorks simulations. For rectangular membranes of each size, pressure was applied from backwards. Figure 63 shows maximum deflection for each membrane.

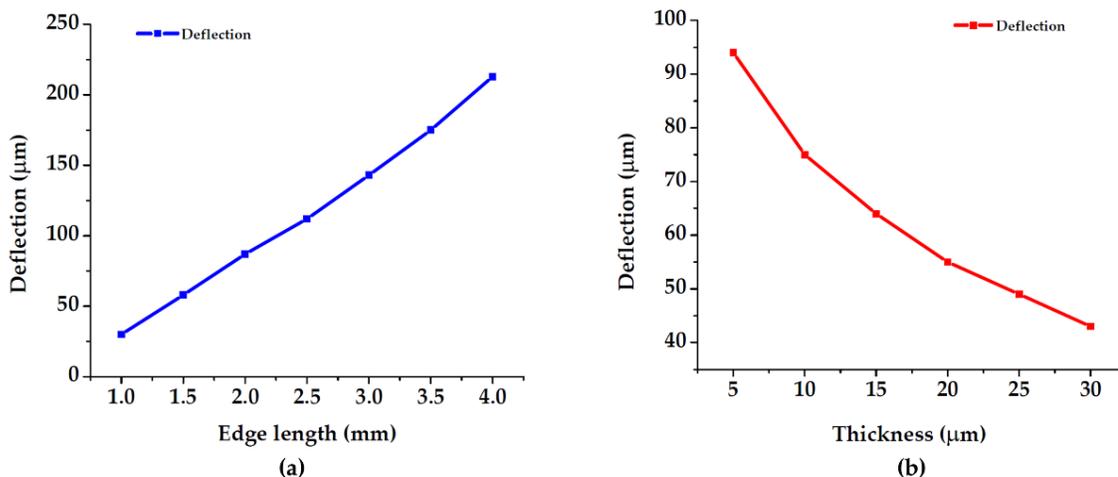


**Figure 63.** Deflection analysis of square membranes with different edge lengths.

Our devices are produced to finely operate between a pressure range of 0 – 120 psi. Therefore, we have simulated for 100 psi pressure to see the how the deflection depends on membrane area and membrane thickness. For this, we have kept membrane thickness  $8\mu\text{m}$  and varied the edge length from 1mm to 4mm. The minimum deflection was  $30.2\mu\text{m}$  for 1mm edge length and maximum deflection was found to be  $215\mu\text{m}$  for edge length of 4mm.

Then, membrane's thickness was varied from  $5\mu\text{m}$  –  $30\mu\text{m}$  keeping the edge length 2 mm. For this, the minimum deflection was  $43.2\mu\text{m}$  for  $30\mu\text{m}$  thickness

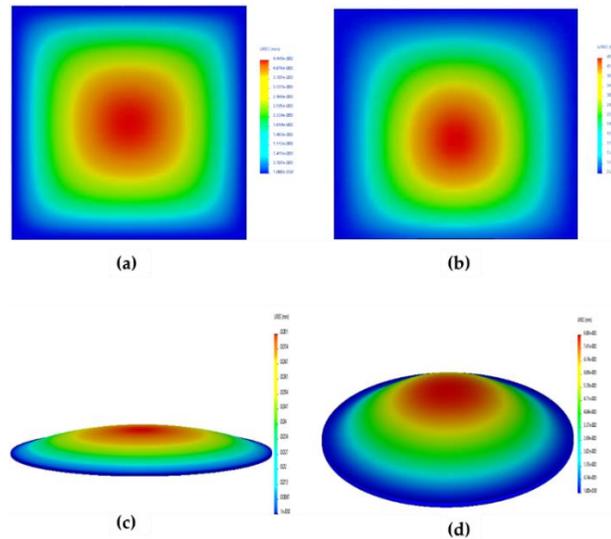
and maximum deflection was found to be 94  $\mu\text{m}$  for 5 mm thickness (Figure 64). Thus, we can say that the maximum deflection increases with the area and decreases with the thickness. Membrane stiffness increases for greater thickness, but this will reduce the sensitivity of it.



**Figure 64.** Deflection as a function of membrane edge length and thickness; (a) edge length versus deflection; (b) thickness versus deflection.

Since deflection is a coefficient of area and thickness, there are several sets of area and thickness for which similar deflection results can be found. Thus, the operational pressure range can be modulated by changing the geometry of the burst disks. In FEA simulations, we found that at 100 psi, deflection was found to be  $\sim 45 \mu\text{m}$  for square membranes edge of 3mm and thickness was  $30 \mu\text{m}$  also for 2.2mm and thickness was  $42 \mu\text{m}$  as well (Figure 65 a, Figure 65 b). For circular burst

disk membranes, at 100psi, deflection was  $\sim 81\mu\text{m}$  for 1.7mm diameter, 7  $\mu\text{m}$  thickness and it is same for 3mm diameter, 30 $\mu\text{m}$  thickness (Figure 65 c, Figure 65 d).



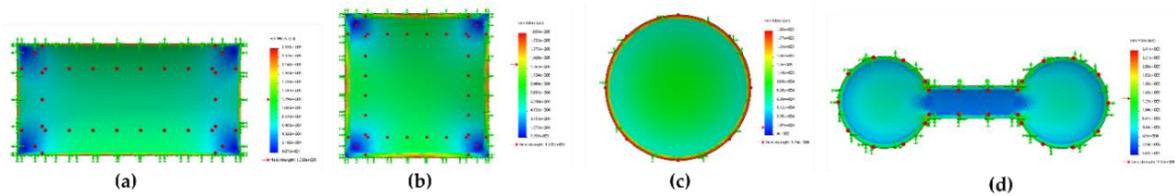
**Figure 65.** Deflection of square membrane burst disks; (a) edge 3mm and thickness 30 $\mu\text{m}$ ; (b) edge 2.2mm and thickness 42 $\mu\text{m}$ ; Deflection of circular membrane burst disks; (c) diameter 1.7mm and thickness 7 $\mu\text{m}$ ; (d) diameter 3mm and thickness 30 $\mu\text{m}$ .

#### 4.1.3 Effect of shape on membrane's stress

To understand how membranes shape affects its reliability, we did stress analysis for circular, square, dumbbell and rectangular shaped membranes.

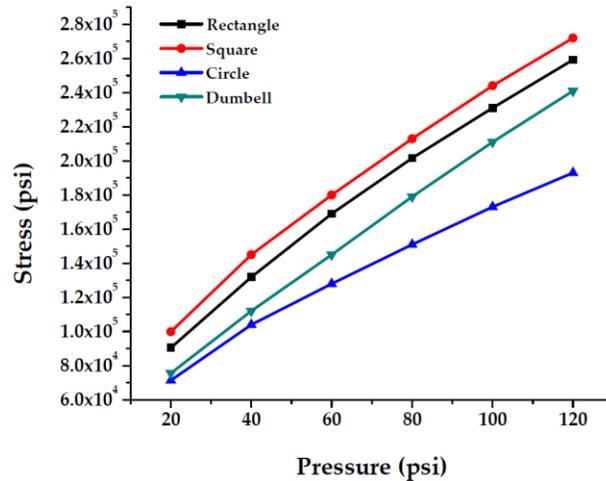
We did FEA simulation studies for observing maximum stress at 0-120 psi pressure on 3mmx3mmx6 $\mu\text{m}$  square membrane, 3mmx6mmx6 $\mu\text{m}$  rectangular membrane, circular membrane of 3 mm diameter with 6 $\mu\text{m}$  thickness and

dumbbell shape membrane with 3 mm diameter having 3 mm distance between the arcs. Figure 66 shows stress analysis of these membranes.



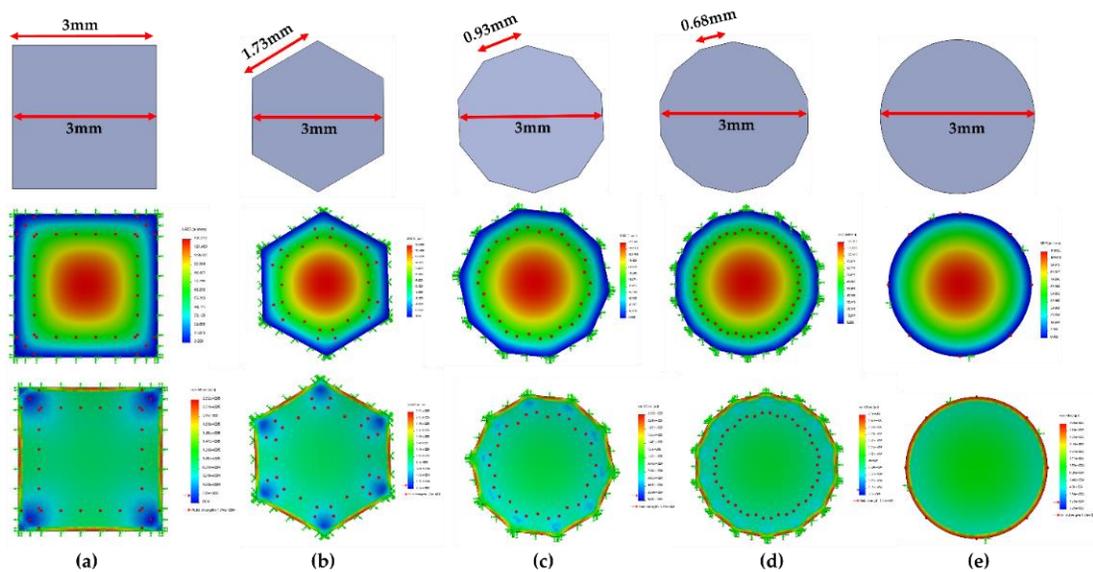
**Figure 66.** FEA for determining maximum stress of membranes having various shapes and sizes.

Figure 67 shows the maximum stress results for these membrane geometries. Maximum stress of rectangular, square, circular and dumbbell shaped membranes at 120 psi are  $2.592 \times 10^5$  psi,  $2.72 \times 10^5$  psi,  $1.93 \times 10^5$  psi, and  $2.41 \times 10^5$  psi.

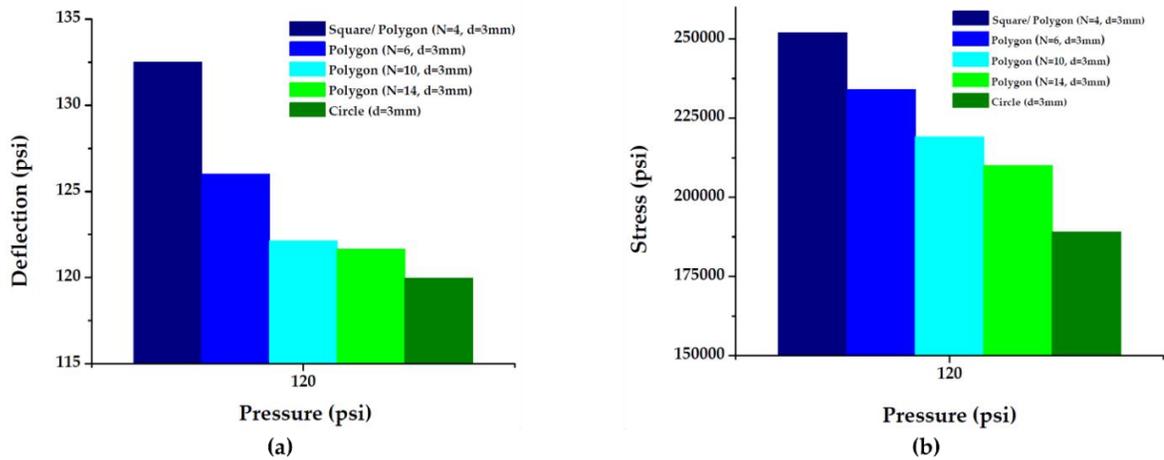


**Figure 67.** Effect of shape on membrane's deflection.

The results indicate that rectangular membranes tend to show higher stress at the boundaries at any pressure compared to other shapes. On the other hand, stress is found to be much lower in circular shape as it is free from corners. To clarify this, we did simulation for square, polygons, and circle and compared the stress and deflection results. Figure 68 and Figure 69 shows deflection and stress analysis results.



**Figure 68.** FEA for comparing maximum deflection and maximum stress of polygons (i.e.  $N=4, 6, 10,$  and  $14$ ) and circle.

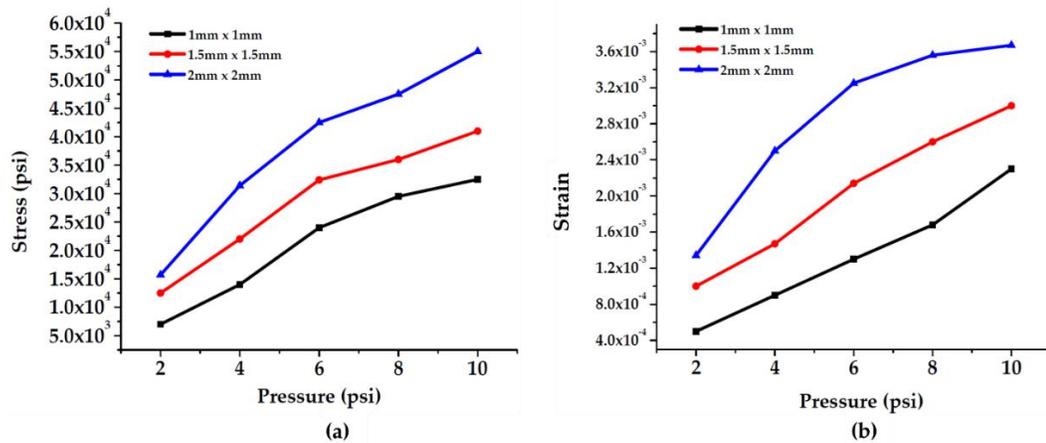


**Figure 69.** FEA analysis for determining effect of corners in membrane, (a) deflection analysis, and; (b) stress analysis.

Figure 69 reflects that stress decreases when the membrane shape comes closer to circular shape. For higher stress, the burst pressure decreases. Therefore, membranes tend to face burst failure more easily. But both deflection and stress tend to get lower for polygons with more edges. Higher deflection ensures higher sensitivity, but higher stress leads to lower longevity. Therefore, we need to keep a balance between membranes sensitivity and robustness to use it for a wide pressure range.

#### 4.1.4 Effect of size on membrane's stress

For pressure range of 2 – 10 psi, stress and strain were calculated using FEA for the same geometries of membranes. From the simulations it was found that stress and strain have proportional relationship with pressure. Besides, for a certain pressure, stress and strain are higher for larger membranes (Figure 70).

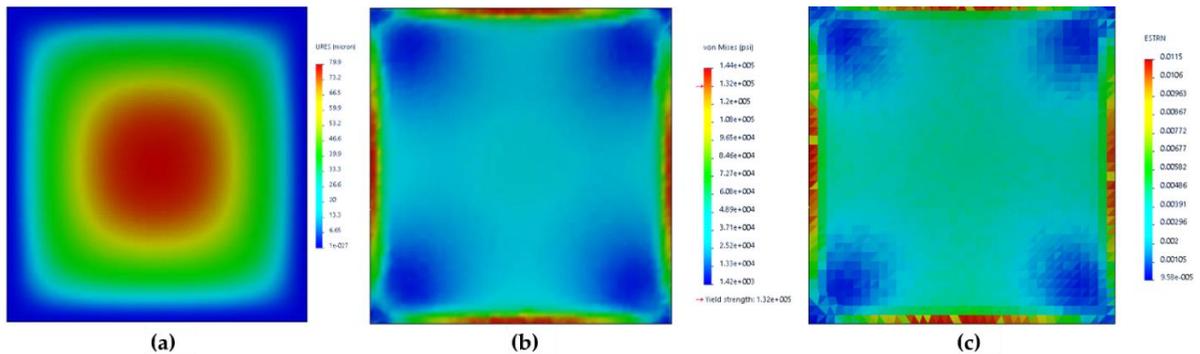


**Figure 70.** Finite Element Analysis for (a) Stress versus pressure; (b) Strain versus pressure as a function of membrane area and thickness.

#### 4.1.5 FEA for Si membranes w/ and w/out $Si_3N_4$

In this work, membrane's robustness and performance were estimated from deflection, stress and strain analysis. For example, robustness of burst disk

of 2mm x 2mm and thickness 8 $\mu$ m was estimated for 0-120 psi pressure range (Figure 71). From FEA, maximum deflection was found to be 80 $\mu$ m, maximum stress  $1.44 \times 10^5$  and equivalent strain was 0.0115. Since we are applying pressure at membrane's back, maximum deflection is found in its center. Also, four edges surrounding the membrane is fixed. Therefore, when pressure hits, majority of stress and strain is seen near those edges (Figure 71).



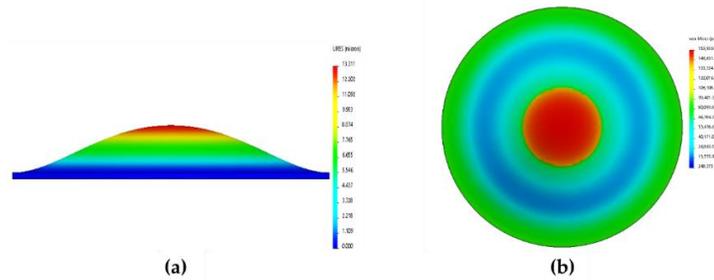
**Figure 71.** FEA for burst disk of 2 mm x 2 mm and thickness 8  $\mu$ m; (a) Deflection; (b) Stress; (c) Strain.

Besides, FEA were done for membranes with  $\text{Si}_3\text{N}_4$  atop. Deflection, stress and strain were analyzed. Figure 71 shows the deflection, stress and strain results for a membrane with 2mm diameter. Sensing element covered around one third portion of it. At 120 psi, simulations were done for 7 $\mu$ m thick membranes of 0.25mm to 8mm in diameter. The size of the sensing element changed accordingly.

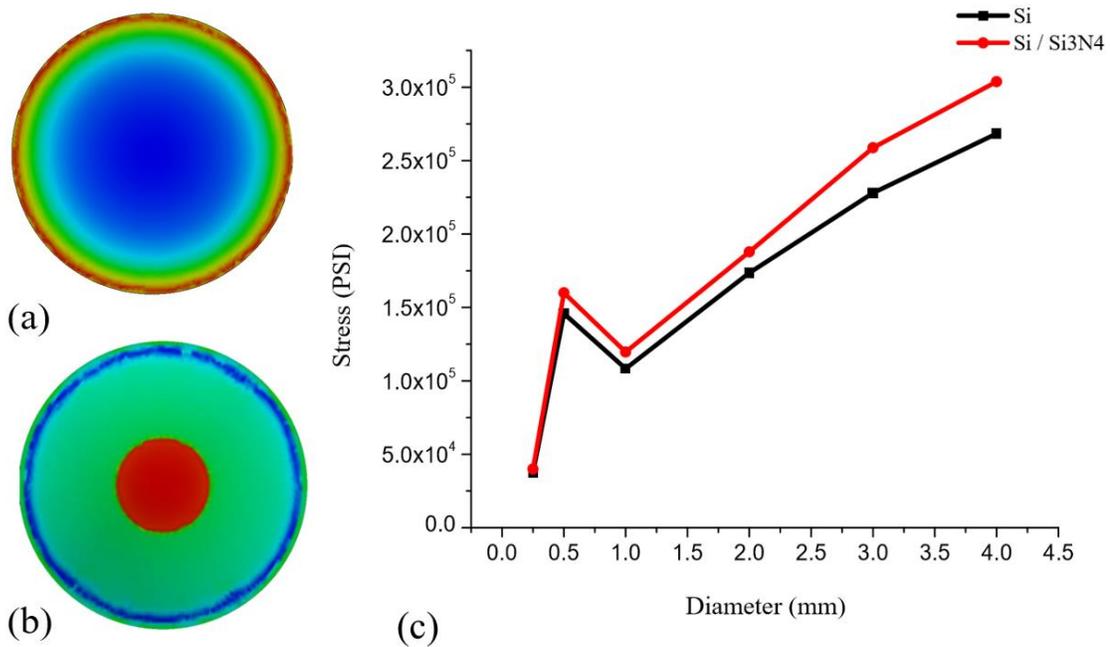
Unlike simple silicon burst disks, here the maximum stress is seen at the center due to the high sensitivity of  $\text{Si}_3\text{N}_4$  (Figure 72). Also, it indicates that we need to deposit a thin  $\text{SiO}_2$  screening layer before depositing  $\text{Si}_3\text{N}_4$  because for surface passivation because direct  $\text{Si}_3\text{N}_4$  deposition can produce high stress at the interface [48]. Deflection changed radically in every increment of diameter. In all cases, the deflection is higher than the thickness. For this reason, there is an additional stretching stress along with membrane bending stress and therefore, ballooning effect is observed. This effect seems lower when pressure is applied on the face having piezoresistors on it. For the opposite case, ballooning effect is very high. In our FEA simulations, pressure is applied at the opposite face.

Simulation were done for Si membranes having  $\text{Si}_3\text{N}_4$  atop for determining deflection, stress and strain (Figure 72). Unlike Si membranes, the results have shown high stress and strain around the periphery and at the center as well. For both cases, stress on the membrane were compared for different diameter values (Figure 73 (c)). We could see that stress on membrane increases when we apply different material on Si. We can see that stress at the Si/  $\text{Si}_3\text{N}_4$  interface is very high. Therefore, we need to keep in mind that direct  $\text{Si}_3\text{N}_4$  deposition can produce high stress at the interface. To pacify this stress, a screening layer should be introduced.  $\text{SiO}_2$  is widely used as screening layer for such devices.  $\text{Si}_3\text{N}_4/\text{SiO}_2/\text{Si}$  stacks can

allow good surface passivation. Besides, such stacks show improved thermal stability due to hydrogen in the nitride layer, in the form of N-H and Si-H bonds.



**Figure 72.** FEA for determining (a) deflection; (b) stress of burst disks having  $\text{Si}_3\text{N}_4$ .



**Figure 73.** (a) Stress on Si membrane; (b) Stress on Si membrane having  $\text{Si}_3\text{N}_4$  atop; (c) Stress versus diameter w/out and w/  $\text{Si}_3\text{N}_4$ .

## 4.2 Experimental Results

This chapter provides the results of mechanical and electrical testing of the membrane devices. The primary measurement of these devices was the burst failure as it is correlated to pressure applied to the back of the membrane and increasing temperature. Besides, thermal stress was increased to analyze the sensitivity of these membranes.

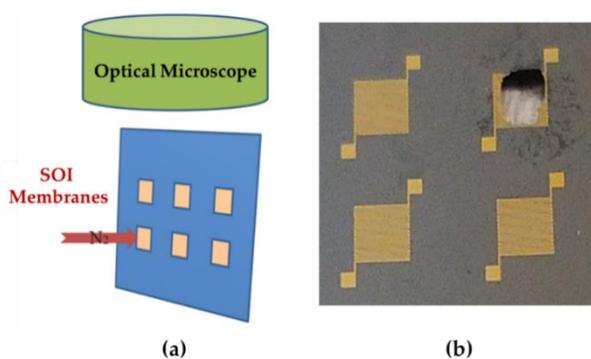
### 4.2.1 *Burst Failure Testing*

The pre-packaged sensors were tested by flowing dry nitrogen and water to verify the burst pressure estimate from FEA. This test provided information about the maximum pressure the burst disks/ membranes can tolerate prior to the burst failure mechanism. The deflection (or applied pressure) versus change in resistance was obtained using an integrated Wheatstone bridge circuit. The bridge circuit converts strain induced resistance changes to voltage outputs [66, 67].

Multiple membranes of various edge lengths and thicknesses were tested. Depending on water pressure and membranes' surface area, certain membranes will burst, and others will not be affected. This distinction, between burst and intact membranes, will reveal a precise pressure. For a certain thickness, the larger

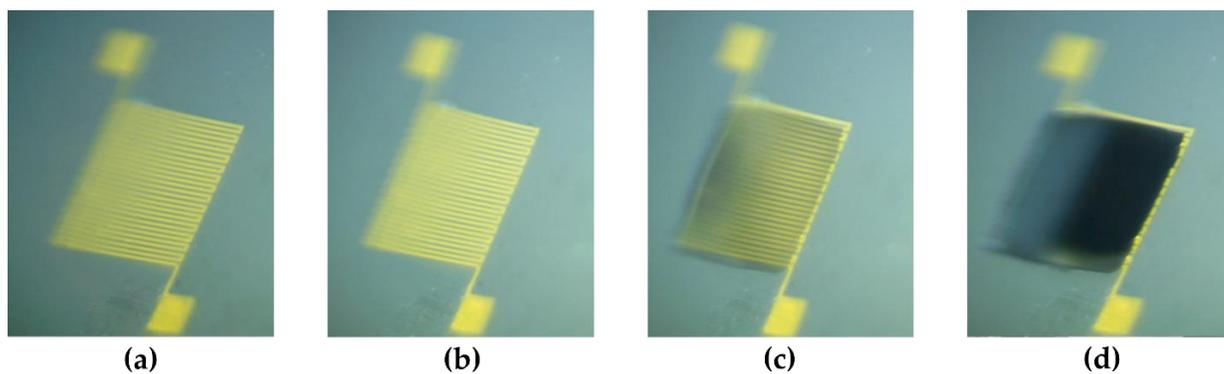
the membrane area, the flimsier it becomes. This allows the membrane to burst at lower pressures. For example, if this sensing coupon was set to measure water pressure using the membranes depicted in Figure 74, and only the 1.4mm and 1.6mm membranes would rupture resulting in a pressure range of 80 to 100 psi.

We did N<sub>2</sub> gas flow testing for membranes of 2mm x 2mm area and 6μm thickness, 2mm x 2mm area and 30μm thickness and for 1.5mm x 1.5mm area and 6μm thickness. N<sub>2</sub> gas flow was increased from 0 psi to 120 psi. N<sub>2</sub> gas was applied on several membranes of each type. For burst disk of 2mm x 2mm area and 6 μm thickness, burst failure happened at ~90 psi gas flow (Figure 76). Burst disks of other two types were working fine even after 90 psi. So, even though the thickness was same, disk of 1.5 mm edge length shown better rigidity. On the other hand, stiffness improved for burst disk of 2mm x 2mm area when thickness increased from 6μm to 30μm. These two membranes failed for 120 psi pressure. The results indicate that smaller and thicker membranes have comparatively higher rigidity than larger and thinner membranes.

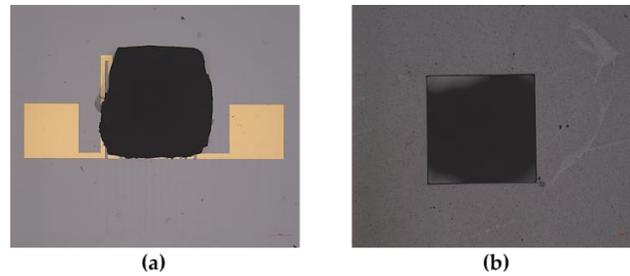


**Figure 74.** Dry  $N_2$  gas flow testing; (a) schematic diagram of setup; (b) burst disk of 2 mm x 2 mm area and 6  $\mu\text{m}$  thickness at ~80 psi.

Figure 75 shows membrane deflection and eventually membrane burst failure at elevated  $N_2$  gas pressure. Test setup mentioned at subsection 3.7.1 is used for this experiment.



**Figure 75.** Dry  $N_2$  gas flow testing on 2 mm x 2 mm area and 30  $\mu\text{m}$  thickness; (a) at 20 psi; (b) at 40 psi; (c) at 80 psi; (d) at 120 psi.



**Figure 76.** Failed membrane due to  $N_2$  gas testing on 1.5 mm x 1.5 mm area and 6  $\mu\text{m}$  thickness; (a) frontside; (b) backside.

A micro-pump was used for applying water pressure on the membrane. Water flow of the pump was increased from 0.05 – 0.5 ml/min. When water hits the membrane, it flexes, and this deforms the strain gauge attached onto the membrane. This leads to resistivity change. Thus, to characterize the membrane deflection, strain gauge's resistance change was measured. Setup for water testing is shown in Figure 77.



**Figure 77.** Setup for water flow testing.

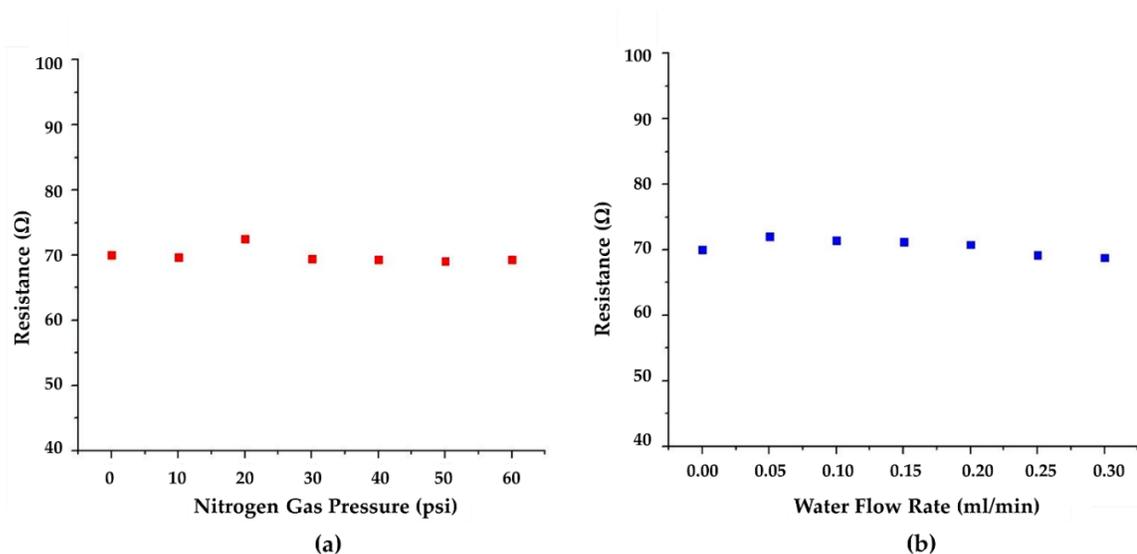
During N<sub>2</sub> and water testing, the Au strain gauge was used to measure resistance changes versus applied pressure or water flow rate. Stable resistance was found for both experiments. The results are shown in Table VII and Figure 78. We were expecting the resistance to rise with increasing pressure.

TABLE VII  
RESISTANCE CHANGE OF THE STRAIN GAUGE

N <sub>2</sub> flow Pressure (psi)	Resistance (Ω)	Water flow rate (ml/min)	Resistance (Ω)
0	70	0	70
10	69.7	0.05	72.1
20	72.5	0.10	71.5
30	69.5	0.15	71.2
40	69.3	0.20	70.8
50	69.1	0.25	69.2
60	69.3	0.30	68.8

Table VII and Figure 78 shows side by side comparison of experimental results for N<sub>2</sub> gas flow and water flow test. For these experiments, a 2mm x 2mm x 6μm sample was used. The results from Table V indicate that the pressure might leak during the experiment for which the resistance did not change much. This also implies that different test setup for N<sub>2</sub> testing can help to collect better data. For water pressure testing, we have noticed that water starts to leak when it fills the test fixture's inner portion even after holding the sample on O-ring with

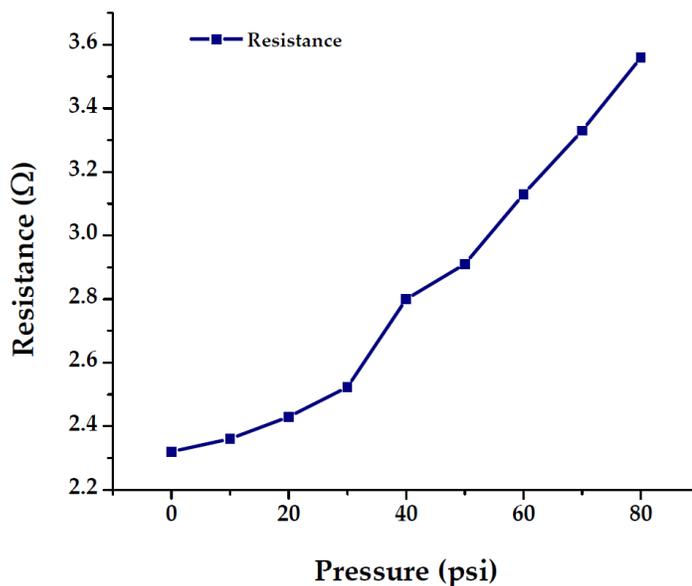
washer (Figure 54 b). An improved test fixture will help to hold the water pressure till the targeted membrane bursts. Also, a pressure sensor can be attached to measure the applied water pressure on the membrane via minipump to verify the accuracy of our device.



**Figure 78.** Resistance change of strain gauge; (a)  $N_2$  gas pressure versus Resistance; (b) Water flow versus Resistance.

Experimental setup showed in Figure 48 was utilized for analyzing  $N_2$  gas induced burst pressure testing on a  $2\text{mm} \times 2\text{mm} \times 6\mu\text{m}$  sample. We increased pressure from 0 psi to 80 psi. As a result, resistance rose from 2.34  $\Omega$  to 3.65  $\Omega$ . This time we got desired results as the device resistance increased proportionally with

the applied pressure. We tested other devices from the same sample as the results were similar. Figure 79 depicts the experimental data.



**Figure 79.** Resistance of the strain gauge increased for higher N<sub>2</sub> pressure.

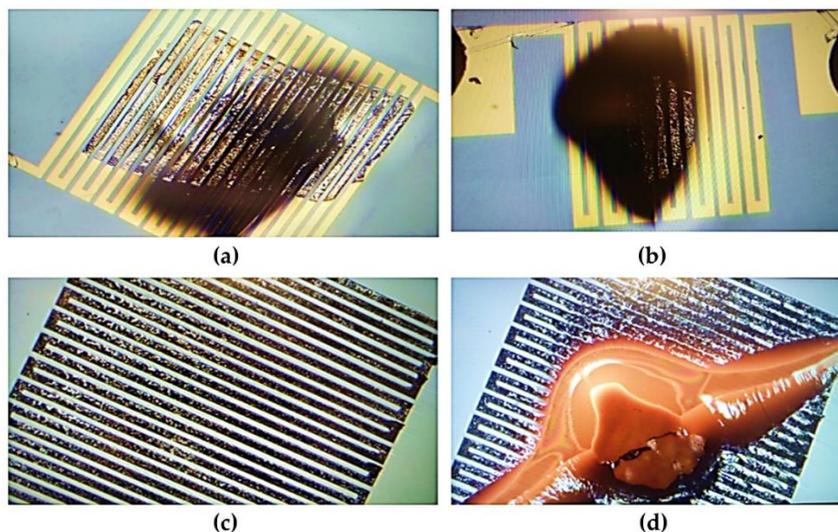
#### 4.2.2 Thermal Testing

Thermal testing pursued to understand the thermal characteristics of the membrane's resistive heater. This will also help us to tune membrane stiffness by heating up. The device was characterized by applying thermal loads using both DC voltage (applied to the Au strain gauge) and a probe-station thermal chuck. The strain gauge Joule heated the membrane with increasing DC voltage and the

strain gauge resistance change was measured using a Wheatstone bridge circuit to reduce unwanted noise.

### Joule Heating:

DC voltage was applied across the strain gauge for stiffness tuning. As current flows across the strain gauge, temperature rises. Current flow increases for higher voltage and leads to device failure after reaching a certain voltage due to excessive heat generation. We took three devices with different geometries (i.e.  $2\text{mm} \times 2\text{mm} \times 6\mu\text{m}$ ,  $2\text{mm} \times 2\text{mm} \times 30\mu\text{m}$ , and  $1.5\text{mm} \times 1.5\text{mm} \times 6\mu\text{m}$ ) to characterize the strain gauge. Figure 80 shows the membranes before and after burst Joule heating induced failure. Experimental results are shown in Table VIII.



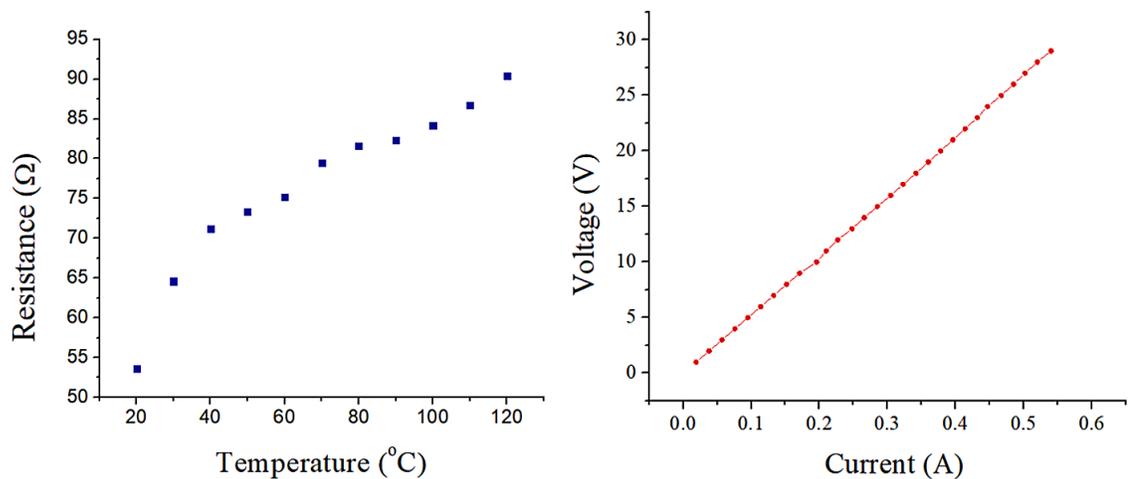
**Figure 80.** Burnt membranes due to DC voltage; (a) burnt  $2\text{ mm} \times 2\text{ mm}$  area,  $6\ \mu\text{m}$  thick membrane; (b) burnt  $1.5\text{ mm} \times 1.5\text{ mm}$  area,  $6\ \mu\text{m}$  thick membrane; (c) burnt  $2\text{ mm} \times 2\text{ mm}$  area,  $30\ \mu\text{m}$  thick membrane; (d) burst  $2\text{ mm} \times 2\text{ mm}$  area,  $30\ \mu\text{m}$  thick membrane.

TABLE VIII  
RESISTANCE CHANGE OF THE STRAIN GAUGE

Edge Length (mm)	Thickness ( $\mu\text{m}$ )	Burning/ Melting Voltage (V)	Burst Voltage (V)
2	6	24	27
2	30	15	22
1.5	6	11	15

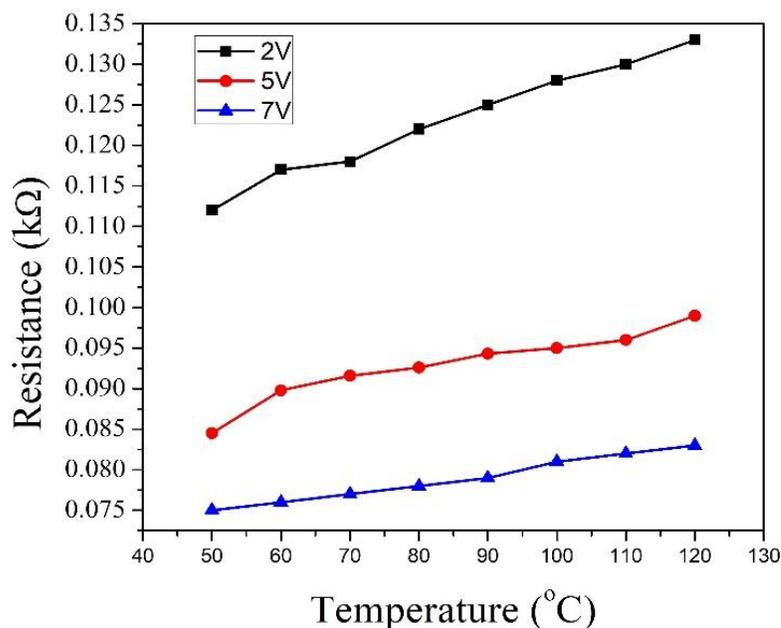
### Heating via Thermal Stage:

The burst disk of 2 mm x 2 mm area and 6  $\mu\text{m}$  thickness were placed on thermal heating stage. We measured resistance while increasing temperature of the hot chuck. Also, voltage was measured for applied current. Figure 81 shows relation of temperature and resistance and I-V characteristic curve at room temperature.



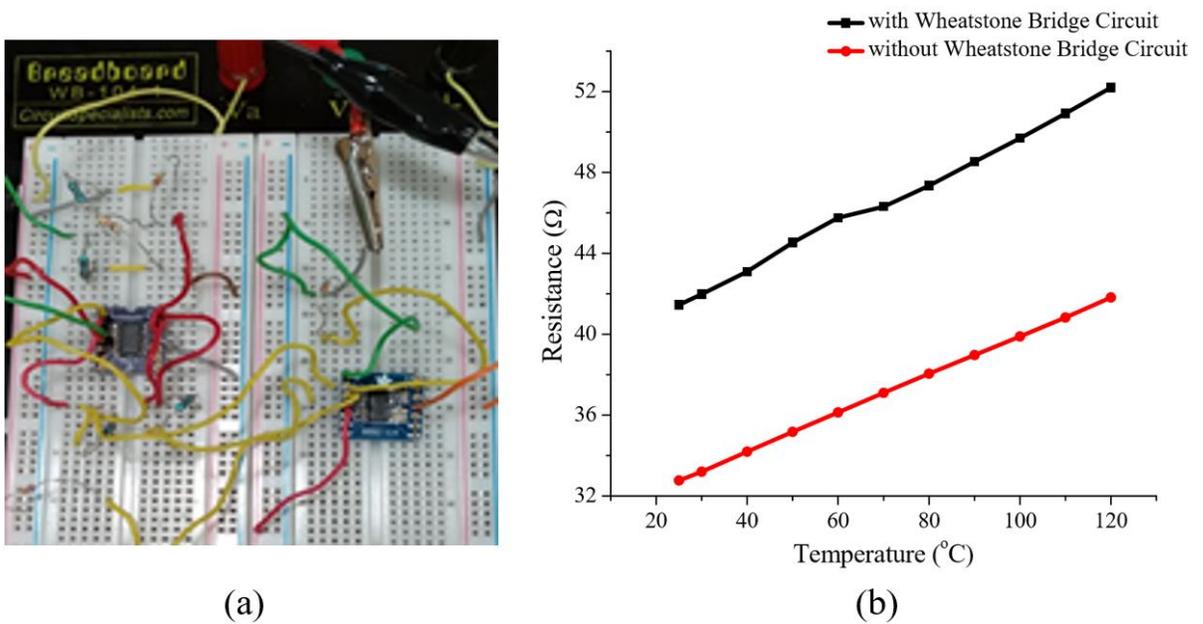
**Figure 81.** Thermal and electrical characterization of burst disk of 2mm x 2mm area and 6 $\mu\text{m}$  thickness; (a) Temperature versus Resistance; (b) I-V characteristic curve.

In addition, resistance of the strain gauge was measured while applying different sweeping voltage via parameter analyzer. Temperature was varied from 25°C – 120°C using heating module and thermal heating stage (Figure 82 only shows resistance variation for temperature 50°C – 120°C). We saw that resistance of the strain gauge lowered for higher sweep voltage. Besides, higher temperature led to higher resistance for 2V, 5V, and 7V. The slopes of the graphs represent coefficient of thermal expansion (CTE) [34]. The CTE is positive as we used a gold strain gauge here (Figure 82).



**Figure 82.** Resistance versus Temperature curves for constant voltages.

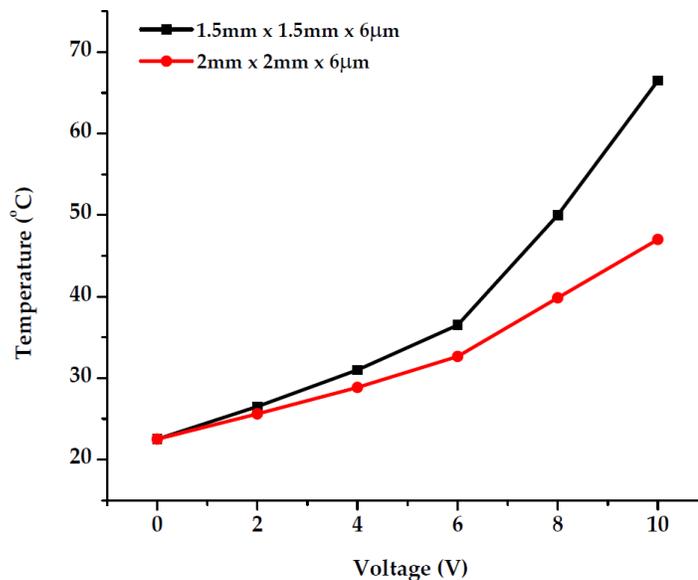
An external Wheatstone bridge has been used to measure resistance change of the Au strain gauge. Resistance of strain gauge was increased by increasing applied N<sub>2</sub> pressure from 0 psi – 80 psi and by increasing temperature from 0°C – 120°C. The results were compared with the results that we got without using the Wheatstone bridge circuit. Even though the results were much better than before, but not good enough as it cannot eliminate unwanted noise properly (Figure 83). For this reason, integrated Wheatstone bridge is needed to acquire accurate data.



**Figure 83.** (a) Wheatstone bridge circuit configuration; (b) Comparing Temperature versus Resistance of strain gage w/ and w/out Wheatstone bridge.

### Heater Temperature:

We measured temperature of different devices (i.e., 1.5mm and 2mm) by applying different voltages through the strain gauge. Smaller devices tend to heat up and eventually fail faster than the bigger devices. As from TABLE VI we got to know that 1.5mm devices burn at 11V, we applied 0V-10V to the devices and measured their temperature using a digital thermometer. The digital thermometer's result was fluctuating, and Figure 84 shows an illustration of our data after several attempts.

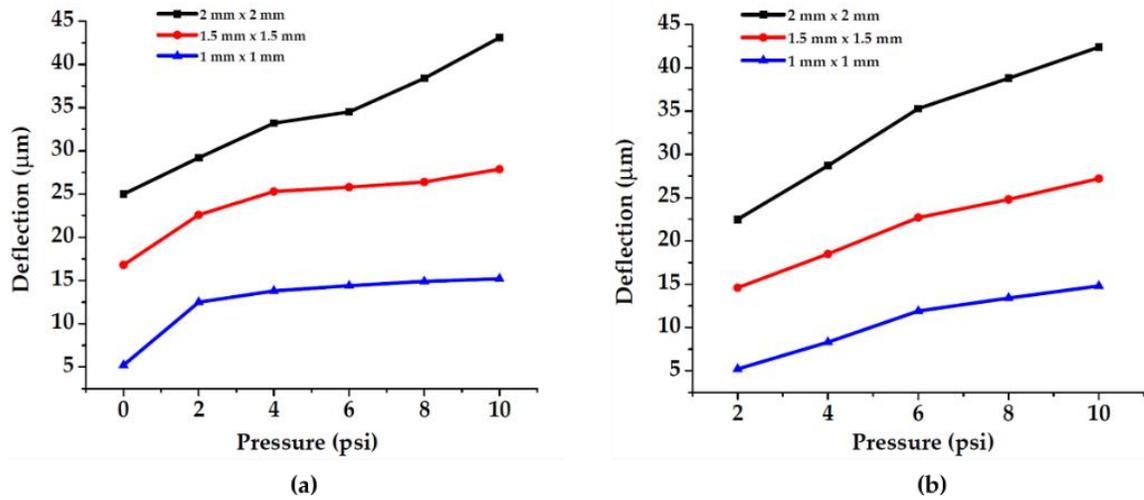


**Figure 84.** Applied voltage versus device temperature; generated due to Joule heating.

## V. Analysis

### 5.1 Simulated versus measured data

Figure 85 compares experimental and SolidWorks simulation data results of membrane deflection versus applied pressure side by side. From both experimental and simulated results, maximum deflection was found to be  $\sim 15\mu\text{m}$ ,  $\sim 28\mu\text{m}$ , and  $\sim 43\mu\text{m}$ . Hence, we can justify our model and conclude that the results match closely. We noticed that the membrane's deflection depends on membrane's length or surface area and its thickness. We noticed higher membrane deflection when we increased the membrane's area but kept the thickness constant for a certain applied pressure. This means that for a specific thickness, larger membranes tend to provide greater deflection. The reason behind this is that same pressure can cause larger stress on a membrane when its area is increased.



**Figure 85.** Deflection versus applied pressure plot as a function of membrane diameter and thickness; (a) experimental result; (b) simulated result.

Based on the FEA and measured results, Table IX Summarizes the relation between membrane area and thickness with maximum stress and maximum deflection for any specific applied pressure.

TABLE IX  
APPLIED PRESSURE VERSUS MAXIMUM DEFLECTION & MAXIMUM STRESS

	Maximum Stress	Maximum Deflection
Membrane Area $\uparrow$	$\downarrow$	$\uparrow$
Membrane Thickness $\uparrow$	$\uparrow$	$\downarrow$

## 5.2 Effect of Joule heating

We introduced Joule heating by applying DC voltage across the strain gauge. We saw that at a certain voltage, smaller devices showed higher temperature. This is because, the smaller length of the resistor allows higher current flow. As a result, higher power dissipates in the strain gauge which causes higher temperatures for the same applied voltage [33].

Resistances of these strain gauges depend on their size. By applying the same voltage to each device, we noticed that smaller the membrane, lesser voltage is required to heat it up. From the results of Table VI, we saw that it took lesser voltage to burn a thin membrane compared to a thicker membrane. Table X Summarizes the relation between membrane area and thickness with maximum stress and maximum deflection for any specific applied voltage induced heating.

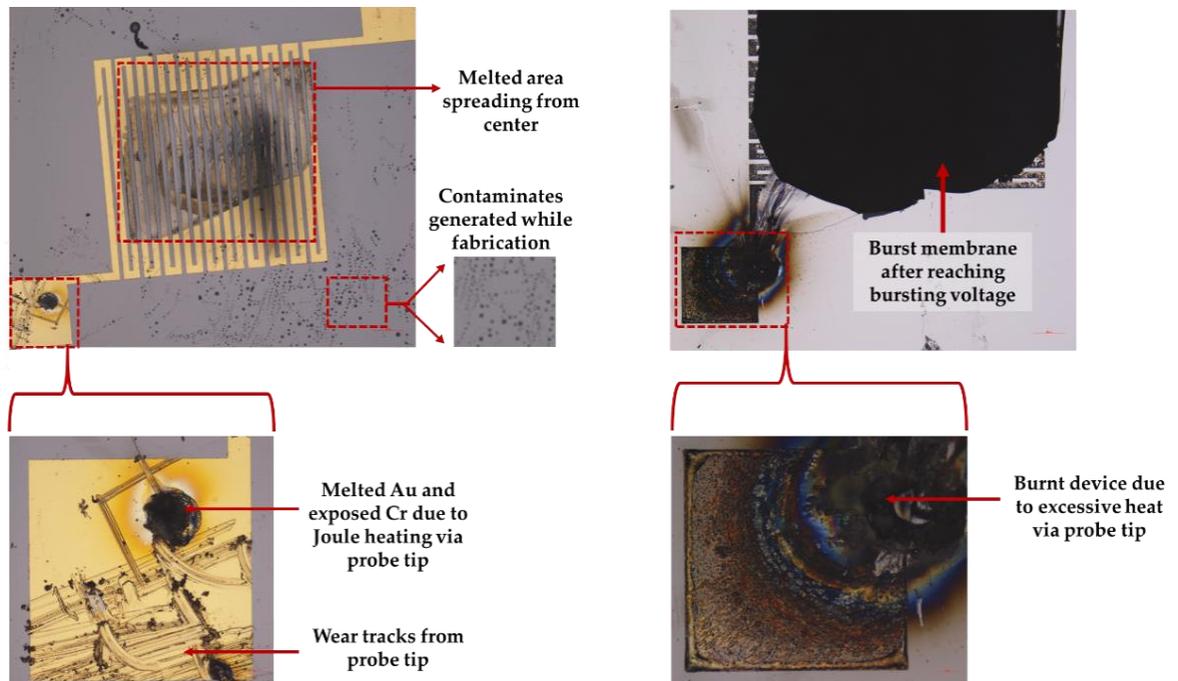
TABLE X  
APPLIED TEMPERATURE VERSUS MAXIMUM DEFLECTION & MAXIMUM STRESS

	Maximum Stress	Maximum Deflection
Membrane Area ↑	↓	↑
Membrane Thickness ↑	↑	↓

## 5.3 Postmortem analysis of failed devices

### 5.3.1 *Failure during thermal experiment*

This section discusses the strain gauge behavior while performing Joule heating tests. Mainly, we wanted to figure out the reasons behind their failure. The gold meandering resistors failed after a certain applied voltage (TABLE VI). The failure is not likely caused by the high current crowd at sharp corners as the resistors did not fail near the corner regions. Instead, the failure was caused by overall Joule heating. Another interesting fact is that smaller Au strain gauges melted faster than the bigger ones. This effect is known as melting-point depression [68]. As peak temperature is found to be at the center of the device, the Au strain gauge located near the center melts first. Starting from the center, the melted portion creeps outward until it covers the entire device. Zeiss AXIO Motorized Microscope was used to take images for observing the failed strain gauges and contact pads (Figure 86).

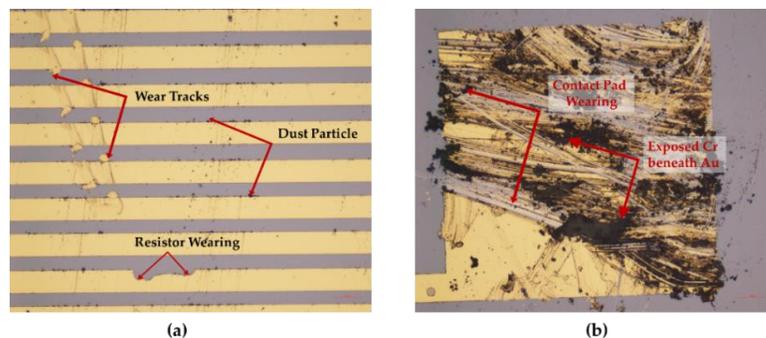


**Figure 86.** Microscopic images showing melted and burnt portions of several failed devices.

### 5.3.2 Failure due to contact wear

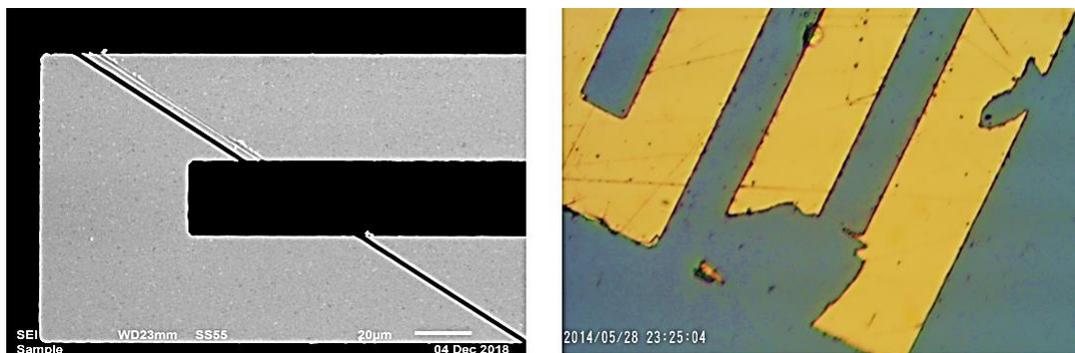
The choice of contact metal very important to design a MEMS device. Among the candidates for contact metal, gold (Au) is the most common metal because of its unique properties. the main reason behind using gold is its incomparable corrosion resistance. Au is least susceptible to oxidation and thus it can prevent rust. Although Au is expensive, its excellent electrical and thermal conductivity guarantee low contact resistance [69]. According to Hanno and

Hosaka, gold has a lower contact resistance in air than silver (Ag) or palladium (Pd) [70]. However, the ideal contact material should have minimum resistivity but maximum hardness. These parameters depend on the design and operation of a specific device. Low contact resistance material means low insertion loss of the contact and higher hardness ensures higher wear resistance and lower adhesion forces at the contact region. The alloying should be such that the wear resistance material should be increased without an increasing the contact resistance [71]. The only issue that can affect the contact performance is Au's high adherence [72]. Besides, Au is prone to contact wear which can affect the device performance [73]. After testing the device, it is very common to leave wear tracks on the contact pads. Figure 87 illustrates the micro wear tracks on a gold meandering resistance and on a contact pad surface.



**Figure 87.** Microscopic image illustrating Au wear due to probe tips; (a) Au strain gauge resistor; (b) Au contact pad.

Dust particles and contaminations accumulate near the rough wear tracks which leads to high and erratic contact resistance. For instance, in a coupon consisting several 2mm x 2mm area, 6 $\mu$ m thick devices, resistance varied from ~2.4 $\Omega$  – 5 $\Omega$ . Devices which are frequently used for testing tends to show higher resistance compared to the newer devices. Since a very thin film of Au is deposited, sometimes Au is absent in some locations. Images taken with AmScope microscope and SEM images were used to find out interruption in Au meandering strain gage (Figure 88). This happens during device fabrication. Similar event can occur while testing the device. Probe tips and dust can leave tiny wear tracks which can scratch out Au from strain gage, causing open circuit. This leads to the failure of the entire device.



**Figure 88.** SEM and Microscopic image of showing absence of Au in Au strain gauge, resulting open circuit.

## VI. Conclusions and Recommendations

This chapter will summarize the findings of this research. The accomplishments of this research will be specified and explained in a brief. In addition, the chapter discusses the recommendations for improving device performance, testing procedures, and applications. Following this, the chapter also focuses on possible directions for future research in this field.

A tunable water pressure sensor was designed, fabricated and characterized. It was found that the membrane sensitivity and stiffness can be modified by altering its geometrical properties (area, shape and thickness). Hence, it is possible to modify the device performance depending on the targeted application. The mechanical stiffness of our MEMS membrane found to be extremely robust and tunable with a thermal stimulus [33]. In this research, membrane shape, thickness and area are used in concert to target specific stiffness values that will result in targeted operational pressure ranges of approximately 0-120 psi. We focused on the difficult challenges of 1) device packaging for the water environment, 2) improved piezoresistive (PZR) sensitivity, 3) improved membrane fabrication, and 4) material improvements. We came up with cheap and effective 3D printed waterproof capping. For better sensitivity, we deposited silicon nitride; however, we are yet to characterize the device performance with it.

Beside water pressure measurement, this device can act as water leak detection burst disk. In devices such as pressure sensors, microvalves and micropumps, membranes can be subjected to immense pressure that causes them to fail or burst [34]. Once the membrane bursts, the device will stop functioning, but this event can be used to indicate the precise pressure level that malfunction occurred. Our microelectromechanical systems (MEMS) membrane arrays will be used to determine pressure values by bursting. The membrane(s) bursting will indicate that water pressure is too high and that there is leakage. Such failure events will be used to detect leakages in household appliances, ranging from automatic sinks to dishwashers. For example, existing burst membranes range from 3mm to 19mm in diameter, with maximum pressure levels ranging from 15psi to 1,000 psi [74]. Burst disks can be used to simultaneously detect leaks, as well as, precisely measure or sense water pressure.

In appliances such as automatic sinks, automatic toilets, washing machines and dishwashers, diaphragm valves control the water flow and water pressure systematically. In these appliances, burst disks can be used as a warning device or gatekeeper which leads to the disabling of a diaphragm valve once there is leakage. The appliance can then be repaired, and the sensor can be replaced. Also, the burst disk will have the dual purpose as an actuator. By manipulating the

thickness and diameter of the membranes, and by adding a resistor to the top of the membrane, the device will act as a pump that directs water flow.

Apart from its multifunctionality, the primary advantage of our device is its high reliability, and extremely low-cost stemming from batch fabrication used in MEMS. For example, a single 6" SOI wafer can result in over 2,200 unpackaged devices costing approximately \$1 per device. For comparison, a typical low-cost sensor ranges between \$1 and \$5 and a typical burst disk, leak detector sensor costs between \$125-\$450 each.

## Appendix A.

### A-1 Process Follower for Piezoresistive material deposition

Init.	Silicon Nitride Strain Gauge Fabrication Process Follower	Notes	Date & Time
1	<b>INSPECT WAFER:</b>  <input type="checkbox"/> Note any defects		
2	<b>SOLVENT CLEAN WAFER:</b>  <input type="checkbox"/> 20 sec acetone rinse <input type="checkbox"/> 20 sec methanol rinse <input type="checkbox"/> 20 sec isopropyl rinse <input type="checkbox"/> Dry with nitrogen at 500 rpm <input type="checkbox"/> Dry wafer with nitrogen on clean texwipes <input type="checkbox"/> 1 min 65°C hot plate bake <input type="checkbox"/> 1 min 95°C hot plate bake <input type="checkbox"/> Dry wafer with nitrogen on clean texwipes		
3	<b>SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub> DEPOSITION:</b>  <input type="checkbox"/> Place a dummy clean wafer and run the O <sub>2</sub> clean recipe in Plasma-Therm Apex SLR HDPCVD tool <input type="checkbox"/> Run the precondition recipe <input type="checkbox"/> Vent and replace the dummy wafer with the sample <input type="checkbox"/> Run the recipe for 1µm SiO <sub>2</sub> deposition in Plasma-Therm Apex SLR HDPCVD tool <input type="checkbox"/> Run the recipe for 1µm Si <sub>3</sub> N <sub>4</sub> deposition in Plasma-Therm Apex SLR HDPCVD tool <input type="checkbox"/> Unload the wafer		
5	<b>HMDS DEPOSITION:</b>  <input type="checkbox"/> Keep it in Hexamethyldisilazane (HMDS) oven at 120°C for 10 minutes		
6	<b>APPLY AZ nLOF 2020:</b>  <input type="checkbox"/> Drop AZ nLOF 2020 over the wafer <input type="checkbox"/> Ensure that the wafer is completely covered to the edges <input type="checkbox"/> Spin coat it for 45 sec at 4000 rpm <input type="checkbox"/> Softbake for 1 minute at 100 °C		
7	<b>EXPOSE AZ nLOF 2020:</b>		

	<ul style="list-style-type: none"> <li><input type="checkbox"/> Open the mask design filr (i.e. .dxf file or .gds file) to K-Layout or Layout editor to make any change</li> <li><input type="checkbox"/> Insert the wafer size and mask design files to Heidelberg MLA150 Direct Write Lithographer</li> <li><input type="checkbox"/> Load the wafer in the tool</li> <li><input type="checkbox"/> Select 375 nm laser wavelength and put 210 mJ/cm<sup>2</sup> as dose</li> <li><input type="checkbox"/> Hit the expose button in MLA software interface</li> <li><input type="checkbox"/> Unload the wafer</li> </ul>		
8	<p><b>DEVELOP:</b></p> <ul style="list-style-type: none"> <li><input type="checkbox"/> Take enough AZ 300 MIF developer and agitate the wafer in it for 1 min</li> <li><input type="checkbox"/> Rinse with DI H<sub>2</sub>O.</li> <li><input type="checkbox"/> Dry with nitrogen.</li> </ul>		
9	<p><b>FLUORINE ICP ETCHING:</b></p> <ul style="list-style-type: none"> <li><input type="checkbox"/> Run the plasma O<sub>2</sub> clean recipe in Inductively Coupled Plasma (ICP) etching tool</li> <li><input type="checkbox"/> Run the etch recipe for etching 1μm Si<sub>3</sub>N<sub>4</sub></li> <li><input type="checkbox"/> Run the etch recipe for etching 1μm SiO<sub>2</sub></li> <li><input type="checkbox"/> Vent and take out the sample</li> </ul>		
10	<p><b>WAFER CLEANING:</b></p> <ul style="list-style-type: none"> <li><input type="checkbox"/> Clean the sample with acetone, IPA and DI water</li> <li><input type="checkbox"/> Put the sample in YES CV200RFS Plasma Asher to clean photoresist residuals</li> <li><input type="checkbox"/> Vent and take out the sample when the recipe finishes</li> <li><input type="checkbox"/> Run recipe 1 in the tool to remove ~15nm thick PR</li> <li><input type="checkbox"/> Take out the wafer when recipe ends</li> </ul>		

## A-2 Process Follower for metal trench & contact pads deposition

Init.	Au Strain Gauge/ Contact Pad Fabrication Process Follower	Notes	Date & Time
1	<b>INSPECT WAFER:</b> Note any defects		
2	<b>SETUP:</b> <ul style="list-style-type: none"> <li><input type="checkbox"/> Start MJB3 to step 4, wait till suss power shows 275W</li> <li><input type="checkbox"/> Start DUV system, needs 10 min to warm up</li> </ul>		
3	<b>SOLVENT CLEAN WAFER:</b> <ul style="list-style-type: none"> <li><input type="checkbox"/> 20 sec acetone rinse</li> <li><input type="checkbox"/> 20 sec methanol rinse</li> <li><input type="checkbox"/> 20 sec isopropyl rinse</li> <li><input type="checkbox"/> Dry with nitrogen at 500 rpm</li> <li><input type="checkbox"/> Dry wafer with nitrogen on clean texwipes</li> <li><input type="checkbox"/> 1 min 65°C hot plate bake</li> <li><input type="checkbox"/> 1 min 95°C hot plate bake</li>   <li><input type="checkbox"/> Dry wafer with nitrogen on clean texwipes</li> </ul>		
4	<b>APPLY SF11:</b> <ul style="list-style-type: none"> <li><input type="checkbox"/> Dropper SF11 over sample</li> <li><input type="checkbox"/> Ensure sample is completely covered to the edges</li> <li><input type="checkbox"/> 4 sec 500 rpm</li> <li><input type="checkbox"/> 30 sec 4000 rpm</li> <li><input type="checkbox"/> 3 min 110°C hot plate bake</li> </ul>		
5	<b>S1818 COAT:</b> <ul style="list-style-type: none"> <li><input type="checkbox"/> Dropper 1818 over sample</li> <li><input type="checkbox"/> Ensure sample is completely covered to the edges</li> <li><input type="checkbox"/> 4 sec 500 rpm</li> <li><input type="checkbox"/> 30 sec 4000 rpm</li> <li><input type="checkbox"/> 3 min 110°C hot plate bake</li> </ul>		
6	<b>EXPOSE S1818:</b> <ul style="list-style-type: none"> <li><input type="checkbox"/> Finish setting up MJB3</li> <li><input type="checkbox"/> Clean Mask (ensure cap is on the spinner)</li> <li><input type="checkbox"/> Put mask on the holder</li> <li><input type="checkbox"/> Carefully raise stage to see height, adjust appropriately</li> </ul>		

	<ul style="list-style-type: none"> <li><input type="checkbox"/> Center sample within one-inch window for alignment. Use the resistor mask.</li> <li><input type="checkbox"/> 8 sec expose, may need longer depends on thickness. SU-8 manual lists the amount of energy necessary to fully expose.</li> </ul>		
7	<p><b>S1818 DEVELOP:</b></p> <ul style="list-style-type: none"> <li><input type="checkbox"/> 45 sec develop with 351 DI Water [1:5] developer</li> <li><input type="checkbox"/> 30 sec rinse with DI</li> <li><input type="checkbox"/> Dry with N<sub>2</sub> on clean texwipes</li> </ul>		
8	<p><b>EXPOSE SF11:</b></p> <ul style="list-style-type: none"> <li><input type="checkbox"/> 200 sec flood expose, may need longer, depends on thickness.</li> </ul>		
9	<p><b>DEVELOP:</b></p> <ul style="list-style-type: none"> <li><input type="checkbox"/> Partially fill small container with SAL 101 developer.</li> <li><input type="checkbox"/> Submerge and agitate the sample in developer for 1 minute.</li> </ul>		
10	<p><b>EVAPORATE Ti/Au:</b></p> <ul style="list-style-type: none"> <li><input type="checkbox"/> Need 500A of Ti and 3000A of Au deposited on top side of sample.</li> <li><input type="checkbox"/> Follow backside etch process after evaporation and before release.</li> </ul>		
11	<p><b>RELEASE:</b></p> <ul style="list-style-type: none"> <li><input type="checkbox"/> Fill beaker with ¼ inch of 1165 stripping agent.</li> <li><input type="checkbox"/> 120°C heat on hot plate until liquid reaches 90°C, cover with foil.</li> <li><input type="checkbox"/> 20 min sample soak in acetone.</li> <li><input type="checkbox"/> Submerge sample in developer for 10 minutes.</li> <li><input type="checkbox"/> Rinse sample and dry with nitrogen.</li> </ul>		

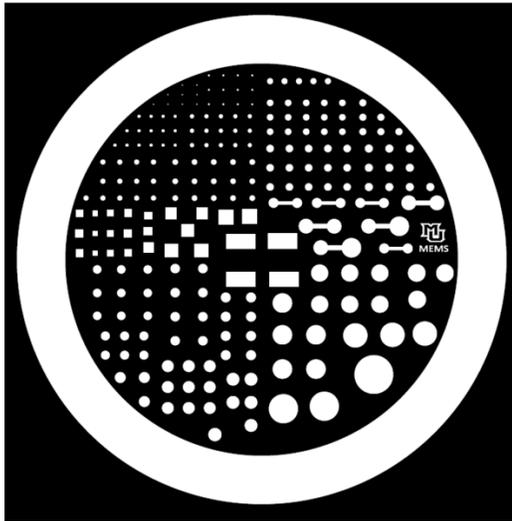
### A-3 Process Follower for membrane formation

Init.	Membrane Fabrication Process Follower	Notes	Date & Time
1	<b>INSPECT WAFER:</b>  Note any defects		
2	<b>SOLVENT CLEAN WAFER:</b> <ul style="list-style-type: none"> <li><input type="checkbox"/> 30 sec acetone rinse</li> <li><input type="checkbox"/> 30 sec isopropyl rinse</li> <li><input type="checkbox"/> 30 sec DI water rinse</li> <li><input type="checkbox"/> Dry with nitrogen at 500 rpm</li> <li><input type="checkbox"/> Dry wafer with nitrogen on clean texwipes</li> </ul>		
3	<b>SPR 220 COAT:</b> <ul style="list-style-type: none"> <li><input type="checkbox"/> Dropper SPR 220 over sample</li> <li><input type="checkbox"/> Ensure sample is completely covered to the edges</li> <li><input type="checkbox"/> 30 sec 2000 rpm</li> <li><input type="checkbox"/> Keep it on hotplate for 90s at 115°C for pre-exposure bake</li> </ul>		
4	<b>EXPOSE SPR 220:</b> <ul style="list-style-type: none"> <li><input type="checkbox"/> Finish setting up Karl Suss MA6/BA6 mask aligner</li> <li><input type="checkbox"/> Clean Mask (ensure cap is on the spinner)</li> <li><input type="checkbox"/> Put mask on the holder</li> <li><input type="checkbox"/> Carefully raise stage to see height, adjust appropriately</li> <li><input type="checkbox"/> Center sample</li> <li><input type="checkbox"/> 50s expose with 500mJ/cm<sup>2</sup> dose and 375nm wavelength</li> <li><input type="checkbox"/> Keep the wafer in room temperature for 30 minutes</li> <li><input type="checkbox"/> Place the wafer on hotplate at 115°C for 90 seconds for post-exposure bake</li> </ul>		
5	<b>DEVELOP SPR 220:</b> <ul style="list-style-type: none"> <li><input type="checkbox"/> Pour 1:5 351 developer in developing dish</li> <li><input type="checkbox"/> Agitate the wafer in developing dish</li> <li><input type="checkbox"/> Keep the wafer in developing dish for 20 minutes</li> <li><input type="checkbox"/> Agitate the wafer before moving it into DI water dish</li> </ul>		

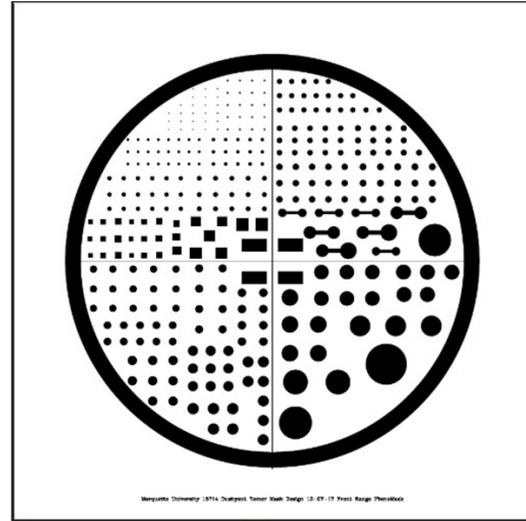
	<ul style="list-style-type: none"> <li><input type="checkbox"/> Rinse it in DI water</li> <li><input type="checkbox"/> Dry it using dry N<sub>2</sub></li> </ul>		
6	<p><b>Carrier Wafer Mounting:</b></p> <ul style="list-style-type: none"> <li><input type="checkbox"/> Dip pointed shaped cotton swabs into fomblin oil</li> <li><input type="checkbox"/> Dab the swab on a 4" carrier wafer</li> <li><input type="checkbox"/> Mount the sample wafer on the carrier wafer</li> </ul>		
7	<p><b>DEEP SILICON ETCHING:</b></p> <ul style="list-style-type: none"> <li><input type="checkbox"/> Run O<sub>2</sub> clean recipe on the Plasma-Therm Versaline DSE (Deep Silicon Etcher)</li> <li><input type="checkbox"/> Put the sample wafer attached with carrier wafer into the loadlock</li> <li><input type="checkbox"/> Run DSE etch recipe for 400 cycles</li> <li><input type="checkbox"/> Bring out the wafers when the process finishes</li> </ul>		
8	<p><b>WAFER CLEANING:</b></p> <ul style="list-style-type: none"> <li><input type="checkbox"/> Clean the sample with acetone, IPA and DI water</li> <li><input type="checkbox"/> Put the sample in YES CV200RFS Plasma Asher to clean photoresist residuals</li> <li><input type="checkbox"/> Vent and take out the sample when the recipe finishes</li> <li><input type="checkbox"/> Run recipe 1 in the tool to remove ~15nm thick PR</li> <li><input type="checkbox"/> Take out the wafer when recipe ends</li> </ul>		

# Appendix B.

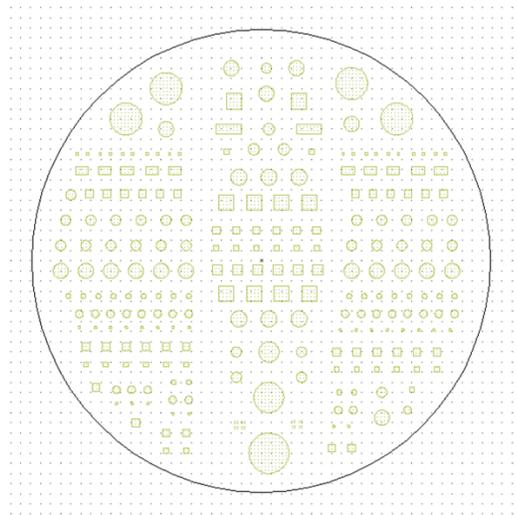
## B-1 Membrane mask sets



(a)



(b)



(c)

Figure B-1. Membrane mask sets

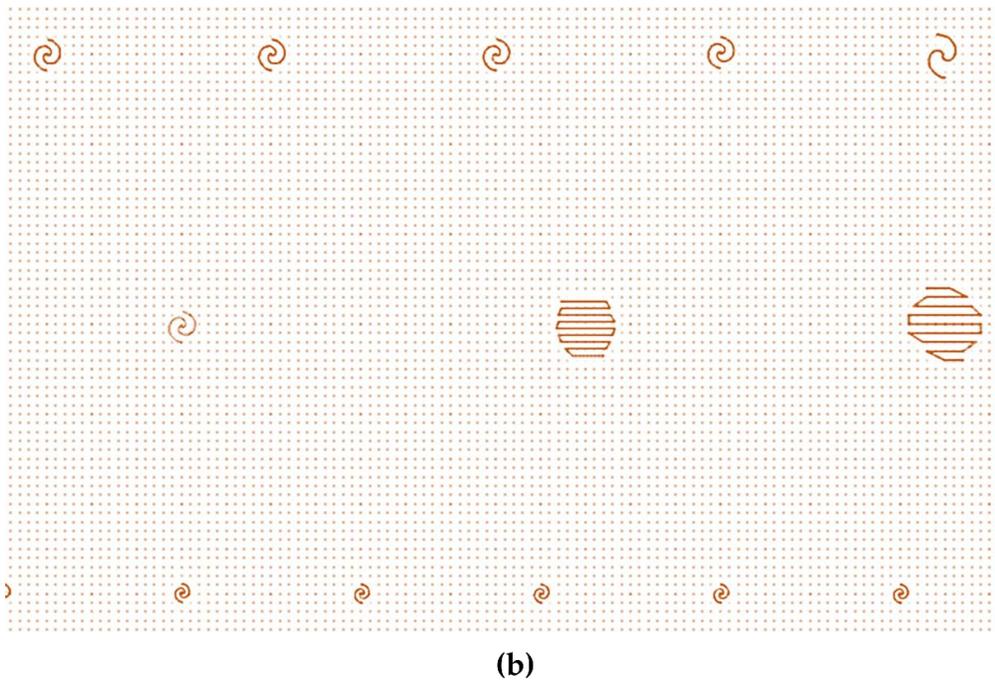
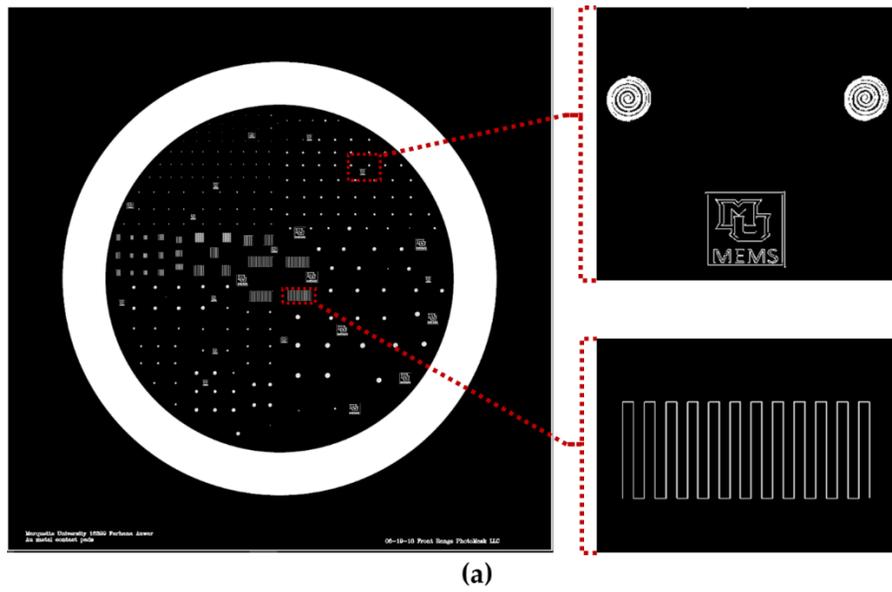
Figure B-1 shows mask patterns for membrane (0.25mm-8mm in diameter/ edge length) fabrication

(a) This membrane etch mask was designed in SolidWorks design module. The black and white portions refer to chrome and transparent, respectively. This polarity is suitable for positive photoresists (i.e.: SPR 220). 10 mm empty space was kept around the mask for DRIE tool at NFC.

(b) In this mask, the black and white portions refer to chrome and transparent, respectively. This polarity is suitable for negative photoresists (i.e.: AZ-nLof 2070)). We kept 5mm empty space around the mask for DRIE tool at PNF. This mask was designed in SolidWorks as well.

(c) This mask was designed in Layout editor and we made it according to the requirements of DRIE tool at PNF.

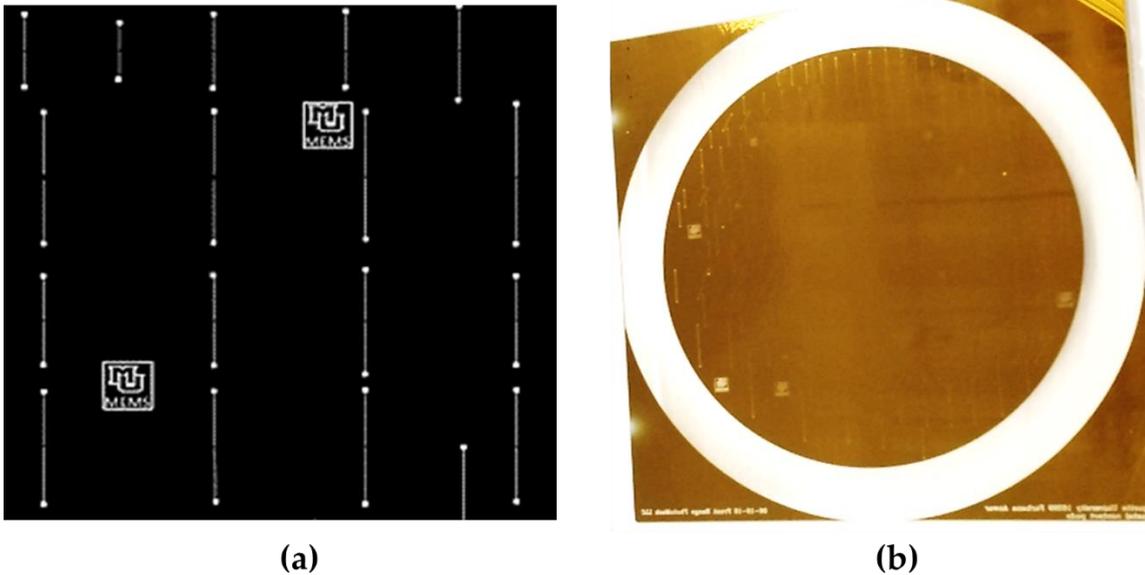
## B-2 Piezoresistive pattern mask sets



**Figure B-2.** Mask pattern for piezoresistive element deposition.

- (a) This mask was designed in SolidWorks design module. However, there is no option to draw Archimedean spirals, we had to draw spirals by connecting arcs. Thus, the patterns are not uniform. The linewidth of the patterns is only  $1\mu\text{m}$  here;
- (b) This mask was designed in Layout editor. It allowed us to draw Archimedean spirals.

### B-3 Mask for metal trench & contact pads



**Figure B-3.** (a) Mask designed using SolidWorks design module; (b) Dark field mask compatible with positive photoresist.

## Appendix C.

### C-1 YES-58TA Vacuum Bake/HMDS Vapor Prime and Image Reversal System



**Figure C-1.** YES-58TA Vacuum Bake/HMDS Vapor Prime and Image Reversal System.

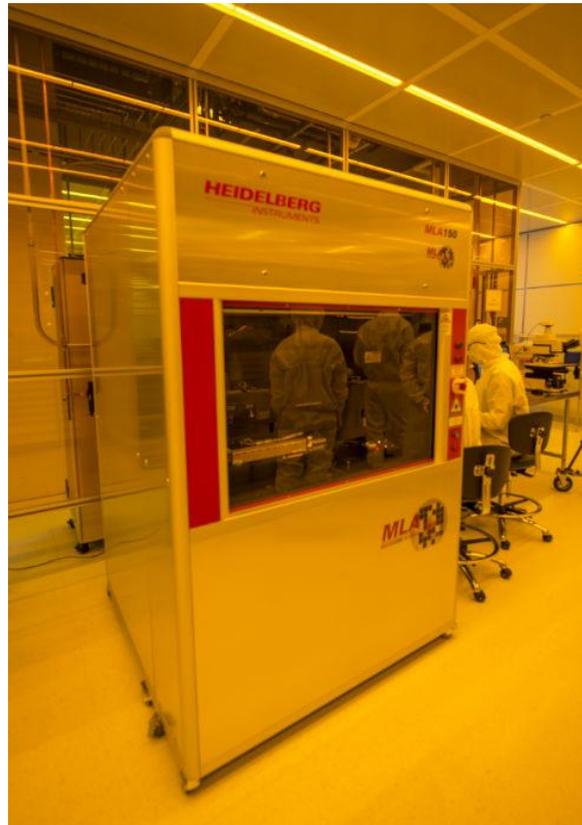
Figure shows HMDS oven tool at University of Chicago, The Pritzker Nanofabrication Facility. We used this tool to make a HMDS monolayer on our samples so that photoresists adhere better on the sample.

## C-2 Solvent Hood



**Figure C-2.** Solvent hood at the University of Wisconsin-Madison, The Nanoscale Fabrication Center (NFC) used for photolithography and cleaning.

### C-3 Heidelberg MLA150 Direct Write Lithographer



**Figure C-3.** Heidelberg MLA150 Direct Write Lithographer

Figure shows Direct Write Lithographer tool from University of Chicago, The Pritzker Nanofabrication Facility. It used for making 4" photomasks and pattern transferring (without photomask) during photolithography.

## C-4 Suss MA6 Lithography Aligner



**Figure C-4.** Suss MA6 Lithography Aligner

MA6/BA6 at the University of Wisconsin-Madison, The Nanoscale Fabrication Center (NFC). It was used for exposing photoresist. Exposure time depends on the photoresist's type and thickness.

## C-5 STS Deep Reactive Ion Si Etcher



**Figure C-5.** STS Deep Reactive Ion Si Etcher at the University of Wisconsin-Madison, The Nanoscale Fabrication Center (NFC). For our recipe, the Si etch rate was  $\sim 2.31$   $\mu\text{m}/\text{min}$ .

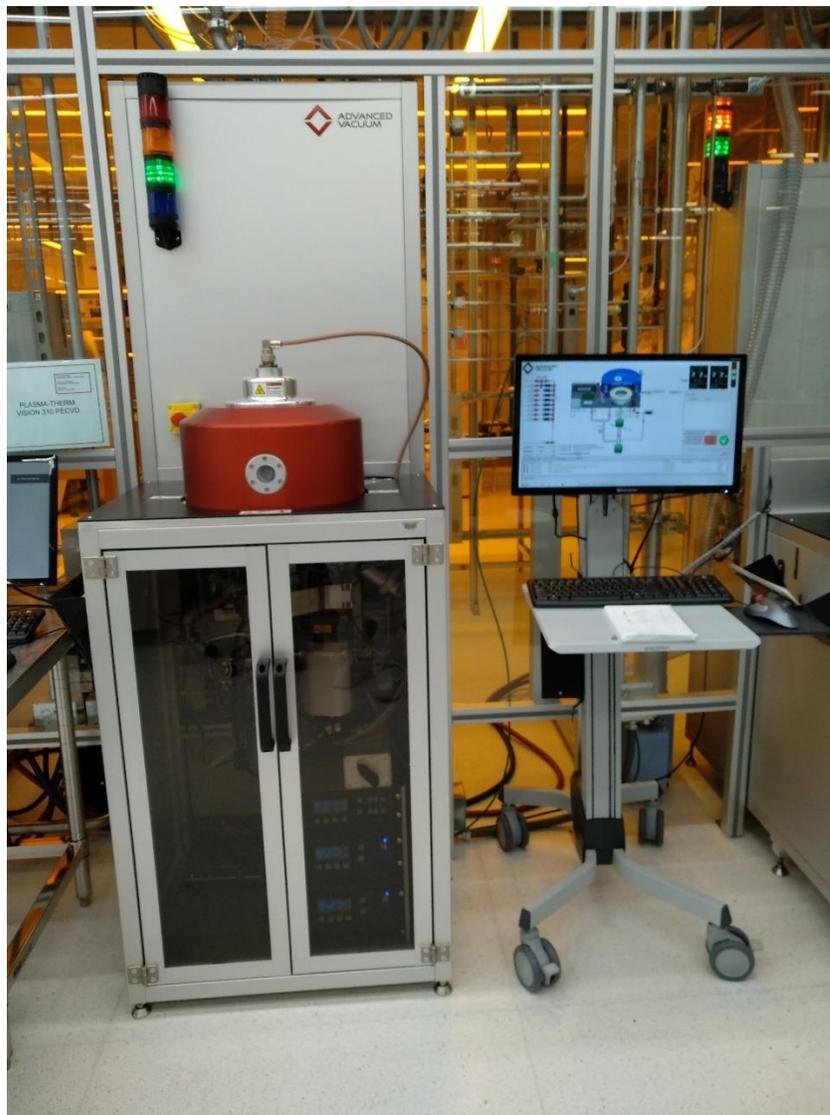
## C-6 Plasma-Therm Versaline Deep Si RIE



**Figure C-6.** Plasma-Therm Versaline Deep Si RIE.

Figure shows DRIE tool from University of Chicago, The Pritzker Nanofabrication Facility. For our recipe, the Si etch rate was  $\sim 8 \mu\text{m}/\text{min}$ .

## C-7 Plasma-Therm Vision 310 PECVD



**Figure C-7.** Plasma-Therm Vision 310 PECVD.

Figure shows PECVD tool at University of Chicago, The Pritzker Nanofabrication Facility. We used it for deposition silicon oxide and silicon nitride layer. Due to low plasma density, it is usually kept at high temperature ( $>300\text{ }^{\circ}\text{C}$ ).

## C-8 Plasma-Therm Apex SLR HDPCVD



**Figure C-8.** Plasma-Therm Apex SLR HDPCVD.

Figure shows HDPCVD tool at University of Chicago, The Pritzker Nanofabrication Facility. We used this tool for depositing silicon oxide and silicon nitride layer on most of our samples as it gave better result.

## C-9 Plasma-Therm ICP Fluoride Etch



**Figure C-9.** Plasma-Therm ICP Fluoride Etch at University of Chicago, The Pritzker Nanofabrication Facility. We etched out silicon nitride and silicon oxide layer to get our desired pattern.

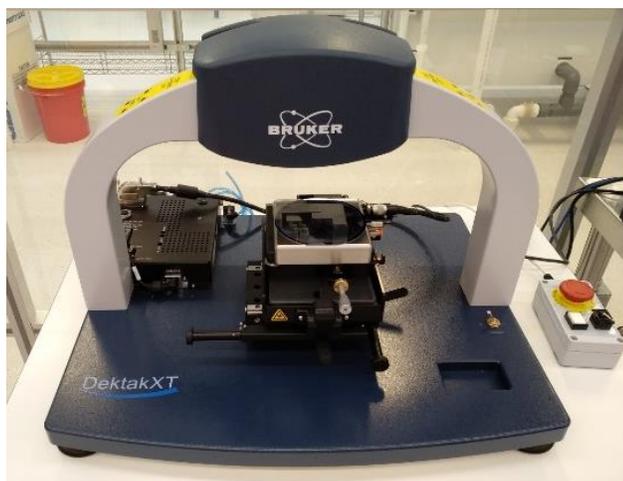
## C-10 YES G1000 Plasma Cleaning System



**Figure C-10.** YES G1000 Plasma Cleaning System.

Figure shows plasma asher tool at University of Chicago, The Pritzker Nanofabrication Facility. We utilized this tool for plasma cleaning our samples at the end of our completing fabrication process.

### C-11 Bruker DektakXT® stylus profiler



**Figure C-11.** Bruker DektakXT® stylus profilometer.

Figure shows stylus profilometer at University of Chicago, The Pritzker Nanofabrication Facility. We estimated etch rate and cavity depth of our membrane by this tool.

### C-12 KLA-Tencor P-7 Surface Profilometer



**Figure C-12.** KLA-Tencor P-7 Surface Profilometer.

Figure shows surface profilometer from our lab. We use this tool to measure thickness of thin layers ( $<300 \mu\text{m}$ ).

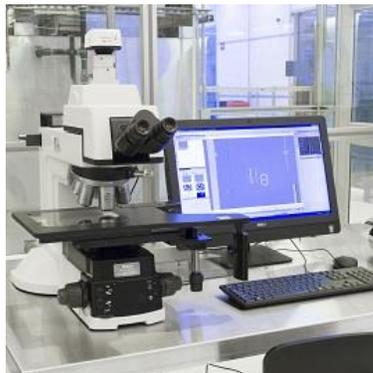
### C-13 Zeiss AXIO Motorized Microscope



**Figure C-13.** Zeiss AXIO Motorized Microscope.

We used this microscope for analyzing our fabricated devices.

### C-14 Nikon Eclipse L200 Microscope



**Figure C-14.** Nikon Eclipse L200 Microscope.

Along with the previous one, we used this microscope from University of Chicago, The Pritzker Nanofabrication Facility to analyze the patterns and to roughly estimate photoresist thickness.

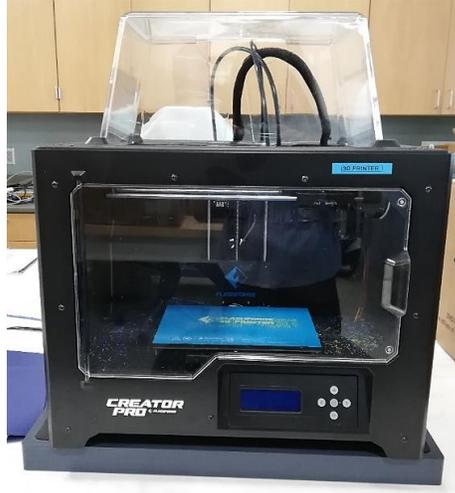
### C-15 Filmetrics 3D profilometer



**Figure C-15.** Filmetrics 3D profilometer.

This optical profilometer was utilized to precisely measure the cavity depth of membranes.

## C-16 Flashforge USA Creator Pro FDM Dual Extrusion 3D Printer



**Figure C-16.** Flashforge USA Creator Pro FDM Dual Extrusion 3D Printer.

We used our 3D printer for making our waterproof capping and test fixtures. We put this on seated on a vibration isolator to keep precision.

## C-17 Micromanipulator DC probe station & HP Parameter analyzer



**Figure C-17.** DC probe station & Parameter analyzer.

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