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Ramin Katebi
Marquette University

Jiangbiao He
General Electric Corporation

Nathan Weise
Marquette University, nathan.weise@marquette.edu

Investigation of Fault-Tolerant Capabilities in an Advanced Three-Level Active T-Type Converter

Ramin Katebi
Department of Electrical and Computer Engineering, Marquette University, Milwaukee, WI
Jiangbiao He
GE Global Research, Niskayuna, NY
Nathan Weise
Department of Electrical and Computer Engineering, Marquette University, Milwaukee, WI

Abstract:

A novel fault-tolerant three-level power converter topology, named advanced three-level active T-Type (A_3L-ATT) converter, is introduced to increase the reliability of multilevel power converters used in safety-critical applications. This new fault-tolerant multilevel power converter is derived from the conventional T-Type converter topology. The topology has significantly improved the fault-tolerant capability under any open circuit or certain short-circuit faults in the semiconductor devices. In addition, under healthy condition, the redundant

phase leg can be utilized to share overload current with other main legs, which enhances the overload capability of the converter. The conduction losses in the original outer devices can be reduced by sharing the load current with the redundant leg. Moreover, unlike other existing fault-tolerant power converters in the literature, full output voltages can be always obtained in this proposed A_3L-ATT converter during fault-tolerant operation. A 13.5-kW ATT-A_3L converter prototype was developed and constructed using silicon carbide MOSFETs. Simulation and experimental results were obtained to substantiate the theoretical claims of this new fault-tolerant power converter.

SECTION I. Introduction

In safety-critical applications, fault tolerance and resilience of power electronic converters are paramount. For multilevel power converters, the probability of device failures is escalated because of the increased part count and system complexity. Although the larger number of switches in a converter leads to a more sophisticated control scheme, the application of fault-tolerant power converters can be justified in safety-critical missions where the continuous operating availability of power converters is given higher priority. These applications include the emerging more electric aircrafts (MEAs), uninterruptible power supplies (UPSs), high-power medical instruments, and renewable energy conversion for grid applications, electric vehicle (EV), hybrid vehicle, and the like.

After the introduction of three-level T-Type and I-Type neutral point clamp (NPC) converters in 1981 [1], different fault-tolerant solutions and circuit topologies have been introduced in the literature to improve the reliability of the three-level converters [2]–[3][4][5][6][7][8][9][10][11]. The fault-tolerant capability of the conventional T-Type inverter has been investigated in [2]. However, the output voltage and linear operating range have to be significantly reduced during fault-tolerant operation modes such as an open-circuit fault in the outer switches. In certain safety-critical applications, such as the aforementioned MEA, EV, and UPS, where the rated output power is crucial, the derated output voltage and power may not be allowable. Two other fault-tolerant T-Type inverter topologies with redundant phase legs were reported in [3] and [4] and can tolerate any open-circuit and short-circuit switching faults. However, the redundant leg is not leveraged in normal operation and is just reserved for the faulty condition. Furthermore, there are many redundant devices kept constant on during normal operation, which obviously causes additional device losses and decreases the converter efficiency. Another fault-tolerant three-phase four-leg T-Type converter topology was recently reported in [5]. This topology can tolerate any open-circuit and certain short-circuit power semiconductor faults. However, as clarified in [5], this converter cannot tolerate a short-circuit fault that could occur in the outer switches of the converter. Similar investigations were also carried out on fault-tolerant I-Type NPC converters [6]–[7][8]. One of the earliest studies on the fault-tolerant operation of three-level I-Type NPC converters was presented in [6], in which the fault-tolerant capability of the converter was implemented based on the inherent redundancy of the switching states. This proposed fault-tolerant solution does not require any redundant converter legs or devices. However, as pointed out by the authors in [6], this solution requires a significant derating in the output voltages of the converter. Reference [7] indicates that the active NPC (ANPC) converter can tolerate any open-circuit faults without a fourth leg, but the ANPC converter is still not immune to all short-circuit faults. Moreover, for some of the proposed fault-tolerant operation in [7], this ANPC converter has to be operated with a derated modulation index resulting in lower maximum output voltage. In [8], a redundant resonant leg is added to a three-phase I-Type NPC converter. In normal operation, the resonant leg is used to balance the oscillation of the NP voltage and improve the converter efficiency. Under faulty condition, this resonant leg will be used to tolerate switching faults in semiconductor devices. However, in addition to the resonant leg, many thyristors and contactors are required to obtain fault-tolerant capability, leading to considerable increase in the system cost and additional device losses.

A novel topology based on the conventional T-Type converter was introduced in [12] and is named "Diode-Free T-Type Three-Level Converter." Accordingly, a fault-tolerant power converter topology based on this diode-free T-Type converter, was introduced as "Active T-Type Three-Level Converter" in [9]. The topology introduced in [9] utilizes two additional active switches and two bidirectional triod thyristors for each phase leg to improve the fault-tolerant capability. The ATT converter has fault-tolerant capability against open-circuit faults, while the problem with short-circuit faults remains unsolved.

Another fault-tolerant converter, namely, A_3L-ANPC converter, is introduced in [10]. The A_3L-ANPC converter has the ability to share the load current with the fault tolerant leg to increase the overload capability of the converter [11]. The A_3L-ANPC converter is superior to the other mentioned topologies in terms of fault tolerance and overload capability.

In this paper, a novel fault-tolerant three-level power converter topology, named "Advanced Three-Level Active T-Type (A_3L-ATT) Converter," will be introduced. The contributions of this paper are as follows: a novel fault-tolerant multilevel converter is introduced, all the open-circuit and certain short-circuit faults are survivable, current sharing capability in normal operation increases the overall converter efficiency and overload capability, and finally proper pulsewidth modulation (PWM) scheme selection for maximizing the current sharing duration is presented. The remaining content of this paper is organized as follows. The operating principle of this proposed A_3L-ATT converter under normal operation is introduced in Section II. The current sharing capability of the proposed A_3L-ATT converter under various PWM strategies is discussed in Section III. The fault-tolerant operation under open-circuit and short-circuit switching faults will be presented in Sections IV and V, respectively. Comprehensive comparison including efficiency, output power, weight, physical volume, and fault-tolerant capability between the proposed A_3L-ATT inverter and the conventional T-Type inverter is simulated and discussed in Section VI. Experimental verification based on a 13.5-kW A_3L-ATT inverter prototype is presented in Section VII. Finally, the conclusions are drawn in Section VIII.

SECTION II. Normal Operating Principle of the Proposed A_3L-ATT Inverter

The circuit topology of the proposed A_3L-ATT converter is shown in Fig. 1. The A_3L-ATT converter has a redundant leg connected between the virtual NP (VNP) and the NP. The presence of the redundant leg provides the A_3L-ATT topology the ability to tolerate all the open-circuit and short-circuit faults. The switches of the redundant leg are sized to be the same as the three main phase legs. The system is developed to use four identical phase modules consisting of three phase legs and one redundant leg, for easy fabrication and packaging.

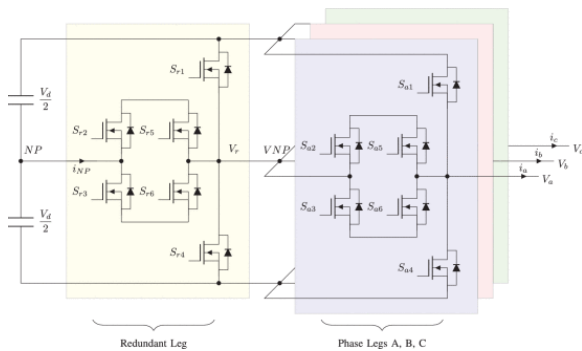Fig. 1. Proposed three-phase A_3L-ATT converter topology.

All the possible switching states of the A_3L-ATT converter are given in Table I. Here, the three switching states, "P," "O," and "N," refer to positive voltage, zero voltage, and negative voltage of the output of each inverter phase leg. Under normal operation, the redundant leg outputs an O state so that the VNP is always connected to

the NP. The current that flows between the VNP and the NP is known as the NP current i_{NP} . To reduce the conduction losses in the redundant leg, all the middle switching devices (S_{r2} , S_{r3}, S_{r5}, and S_{r6}) in the NP current path are turned ON at the O state. The available switching states in normal operation are P_O, O, and N_O and are depicted in Table I (red). Note that in these three states, the VNP is always connected to the NP. The converter can be modulated as a regular three-level converter with three voltage levels available per phase because the VNP is always connected to the NP. Table I also contains other switching states such as P_{sh}, P_s, N_s, and N_{sh}, but these are reserved for additional capabilities such as current sharing mode which will be discussed in Section III. The signals P_{sh}, P_s, P_O N_{sh}, N_s, N_o, and O are tied to a color scheme. In order to produce an output voltage vector at a given time, one can only use switching state types of the same color. That is because of the fact that the switching status of the redundant leg will conflict (creating dc bus short-circuit faults) between two different colors, if the same coloring scheme is not used. The details of these additional switching combinations are discussed in Section III.

TABLE I Switching States of the A₃L-ATT Converter With Color Scheme

Switching State	Type	Switching Status											
		Phase Leg ($x = a, b$, or c)						Redundant Leg					
		S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{r1}	S_{r2}	S_{r3}	S_{r4}	S_{r5}	S_{r6}
p	P_{sh}	1	1	1	0	1	1	1	0	0	0	0	0
	P_s	1	0	1	0	1	0	0	0	0	1	0	0
	P_o	1	0	1	0	1	0	0	1	1	0	1	1
O	O	0	1	1	0	1	1	0	1	1	0	1	1
N	N_{sh}	0	1	0	1	0	1	0	0	0	1	0	0
	N_s	0	1	0	1	0	1	1	0	0	0	0	0
	N_o	0	1	0	1	0	1	0	1	1	0	1	1

SECTION III. Current Sharing Capability

Overload capability is an important factor to be considered during the design of power converters in many applications, such as UPS, EV, servo drives, and the like. Thanks to the redundant leg in the proposed A₃L-ATT converter, the overload current capability can be significantly improved and the conduction losses can be reduced. Specifically, the redundant leg can be used to provide parallel conduction paths for the load currents in phase legs a, b, and c. For example, Fig. 2(a) is showing a current sharing scenario where the redundant leg is sharing the load current with Phase-A leg. The Phase-A leg is producing a P state at the output while simultaneously the redundant leg is also producing a P state at the output. The output of the redundant leg is connected to the load through phase leg a. Assuming the on-state resistance of the silicon carbide (SiC) MOSFETs used in the topology as R, the current sharing paths will provide a parallel path with the on-state resistance of 3R. The equivalent resistance between the dc bus and the output will decrease to 0.75R which is a 25% reduction in conduction losses. The conduction losses can be reduced further by turning ON the second sharing path shown in Fig. 2(b) (blue). The equivalent resistance between the dc bus and the output will decrease to 0.66R which is a 33% reduction in conduction losses while producing the P or N state at the output. The A₃L-ATT converter has superior current sharing capability than the A₃L-ANPC converter [11] because of the total equivalent resistance when outputting P or N state. Current sharing capability cannot be used while any one of the phase legs a, b, or c is in the O state, because turning ON S_{r1} or S_{r4} will lead to a shoot-through fault in the dc bus.
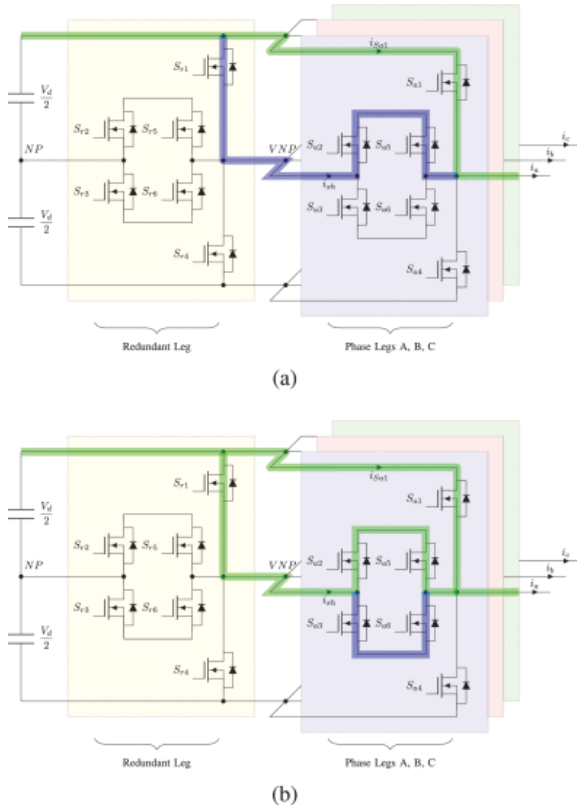
Fig. 2. Proposed current sharing strategy under normal operation. (a) Current sharing with one path. (b) Current sharing with two paths.

The switching states of the converter are categorized with colors as given in Table I. The group of red states represents the normal operation mode with no current sharing. The group of blue states enables current sharing mode for the phase legs that are outputting a P state. Finally, the group of yellow states implement current sharing mode for the phase legs that are outputting an N state. All the phase legs must use a switching state from the same color group simultaneously in order to avoid a shoot-though fault in the dc bus.

As an example, considering a case that the phase leg a is outputting a P state and the phase legs b and c are outputting an N state, current sharing is possible if P_{sh} is selected for the phase leg a and N_s is chosen for the phase legs b and c. Note that the chosen states are from the same color group in Table I. Current sharing capability is highly dependant on the modulation scheme which is used to control the converter. In Sections III-A–III-D the current sharing characteristics of different modulation schemes are discussed. The basic principle of the various PWM schemes that are going to be discussed is presented in [13].

A. Current Sharing in Sine-PWM-PD Scheme

Equation (1) shows the three sinusoidal duty ratios for the three-phase inverter with the Sine-PWM-potential difference (PD) modulation strategy [13]

$$
\begin{aligned}
d_a &= m\cos(\omega t) \\
d_b &= m\cos(\omega t - 2\pi/3) \quad (1) \\
d_c &= m\cos(\omega t - 4\pi/3).
\end{aligned}
$$

The modulation index m controls the magnitude of the inverter output voltages and ω sets the output angular frequency. Current sharing is only possible when all the three phase legs output either P or N states. In other words, none of the phase legs can output an O state during current sharing mode. In order to determine when current sharing is possible, one additional duty ratio is calculated and given in (2)

$$d_{s-\text{sine}-\text{pd}} = max(|d_a|, |d_b|, |d_c|) + min(|d_a|, |d_b|, |d_c|) - 1. \,(2)$$

Current sharing in the Sine-PWM-PD scheme is possible when $d_\text{s-sine-pd}$ is greater than zero. Fig. 3 shows the possible intersections of $d_\text{s-sine-pd}$ (blue) and zero (gray) at different angles and modulation indices. The duty ratio $d_\text{s-sine-pd}$ is plotted 10 times starting with a modulation index of $m = 0.1$ up to a modulation index of $m = 1$ in steps of 0.1. The line thickness is representative of the value changes of the modulation index. For example, starting at $m = 0.1$, the line is at its thinnest, and as m increases the thickness increases. Note that current sharing is not possible for modulation indices below 0.66. According to (3), the current sharing capability of the converter is enabled if $d_\text{s-sine-pd}$ is greater than zero and the sharing duration (d_share) is equal to $d_\text{s-sine-pd}$. Otherwise, if $d_\text{s-sine-pd}$ is less than zero, the converter cannot share current and d_share will be equal to zero. Note that current sharing is not possible for modulation indices below 0.66 because modulation indices below 0.66 will result in $d_\text{s-sine-pd}$ smaller than zero, as given in (3)

$$d_\text{share} = \begin{cases} d_\text{s-sine-pd}, & \text{if } d_\text{s-sine-pd} > 0 \\ 0, & \text{if } d_\text{s-sine-pd} \leq 0. \end{cases} \,(3)$$

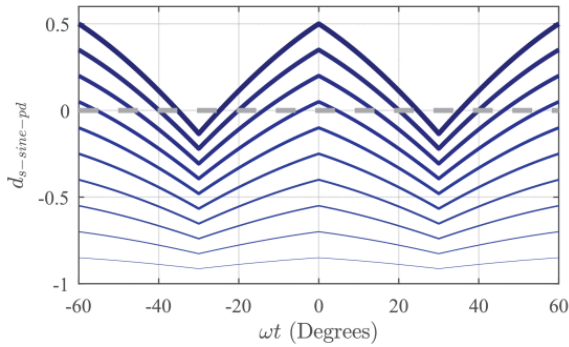
Fig. 3. Current sharing duty ratio $d_\text{s-sine-pd}$ (blue) in the Sine-PWM-PD modulation scheme.

Fig. 4(a) shows the output voltages of each phase leg including the redundant leg. In addition, the triangular carrier signals (shown in thin brown traces), duty ratios, and switching combinations are shown. Assuming a modulation index $m = 0.9$ and $\omega t = 10°$, the duty ratio $d_\text{s-sine-pd}$ is calculated to be 0.1941. Since the duty cycle is greater than zero, the current sharing is enabled and $d_\text{share}=0.1941$. Accordingly, the selected phase leg can share the load current with the redundant leg for a duty ratio of 19.41% of that specific switching cycle. Recalling that sharing current with Phase-A leg is associated with the switching states in Table I (blue). Note that in Fig. 4(a), the load current in Phase-A leg is shared with the redundant leg and the sharing duration, shown in blue, is approximately 19.41%.
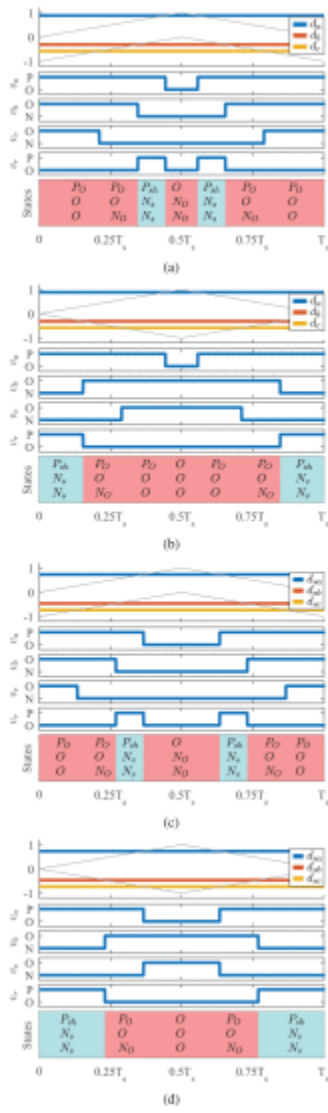
Fig. 4. Current sharing duration in a switching cycle under various sine pulsewidth modulation (SPWM) schemes, $m = 0.9$ and $\theta = 10°$. (a) Sine-PWM-PD. (b) Sine-PWM-POD. (c) SFO-PWM-PD. (d) SFO-PWM-POD.

Fig. 5(a) shows the possible current sharing ratios d_{share} over a range of modulation indices and ωt. The range of ωt is from $-30°$ to $30°$ because it repeats every $60°$ and the range of the modulation index changes from 0 to 1. It is observed that sharing is not possible for modulation indices below 0.66. Maximum current sharing duty ratio of 50% is obtained at $m = 1$ and $\omega t = 0°$.
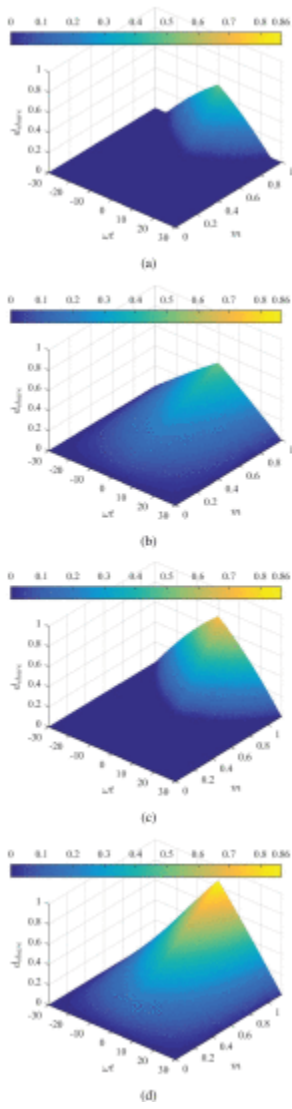
Fig. 5. Current sharing capability of the proposed A$_3$L-ATT inverter for various SPWM strategies. (a) Sine-PWM-PD. (b) Sine-PWM-POD. (c) SFO-PWM-PD. (d) SFO-PWM-POD.

It should be noted that the first quarter cycle in Fig. 4(a) is producing P_O, O, and O states for the three phases which belong to one color scheme in Table I. The third time interval in Fig. 4(a) is outputting P_{sh}, N_s, and N_s state which belong to the blue color scheme shown in Table I.

B. Current Sharing in Sine-PWM-POD Scheme

The modulation of the Sine-PWM-para-operational device (POD) scheme [13] uses the same three duty ratios as the Sine-PWM-PD scheme, but the carrier signal is shifted by 180° as shown in Fig. 4(b) (i.e., the thin brown traces). Unlike the Sine-PWM-PD scheme, current sharing is always possible for the Sine-PWM-POD scheme. The duty ratio of the current sharing over a switching cycle is shown in (4)

$$d_{\text{share}} = min(|d_a|, |d_b|, |d_c|). \ (4)$$

The calculated sharing duty ratio for the modulation index $m = 0.9$ and the $\omega t = 10°$ is 0.3078. In other words, the load current in any phase leg can be shared with the redundant leg for 30.78% of that specific switching cycle. Fig. 5(b) shows the possible current sharing duty ratio over a switching cycle. Obviously, the current

sharing region is possible over the whole range of modulation indices in comparison with the Sine-PWM-PD scheme, but the maximum sharing duration cannot exceed 50%.

C. Current Sharing in SFO-PWM-PD Scheme

The three duty ratios for the three-phase inverter with the switching frequency optimal (SFO)-PWM-PD scheme [13] are given in (5) and (6)

$$
\begin{aligned}
d_{\text{inj}} &= 0.5[max(d_a, d_b, d_c) + min(d_a, d_b, d_c)] \\
d_{\text{sa}} &= d_a - d_{\text{inj}} \\
d_{\text{sb}} &= d_b - d_{\text{inj}} \\
d_{\text{sc}} &= d_v - d_{\text{inj}}.
\end{aligned}
\qquad \text{(5) (6)}
$$

Similar to the Sine-PWM-PD switching strategy, the current sharing is possible when $d_{s-\text{sfo-pd}}$ is greater than zero, as given in (7). The sharing duty ratio (d_{share}) is equal to $d_{s-\text{sfo-pd}}$ when current sharing is possible, as shown in (8)

$$
d_{s-\text{sfo-pd}} = max(|d_{\text{sa}}|, |d_{\text{sb}}|, |d_{\text{sc}}|) + min(|d_{\text{sa}}|, |d_{\text{sb}}|, |d_{\text{sc}}|) - 1
$$

$$
d_{\text{share}} = \begin{cases} d_{s-\text{sfo-pd}}, \text{if } d_{s-\text{sfo-pd}} > 0 \\ 0, \text{if } d_{s-\text{sfo-pd}} \leq 0. \end{cases}
\qquad \text{(7) (8)}
$$

Fig. 4(c) illustrates the carrier signals, duty ratios, and the switching combinations used for the SFO-PWM-PD scheme. Assuming a modulation index $m = 0.9$ and $\omega t = 10°$, the calculated current sharing duty ratio is 0.1941. This indicates that sharing the load current with the redundant leg is possible for 19.41% of that specific switching cycle. Unlike the Sine-PWM-PD scheme, the maximum modulation index is not fixed at 1 and can be increased to 1.1547. Assuming the same maximum output voltage for the Sine-PWM-PD and the SFO-PWM-PD schemes, the modulation indices are calculated to be $m = 0.9$ and $m = 1.0392$, respectively. The calculated current sharing duty ratios are d_{share}=0.1941 and d_{share}=0.3788, respectively. Obviously, for generating the same output voltage, the SFO-PWM-PD has larger current sharing duty ratio in comparison with the Sine-PWM-PD scheme. This means that the SFO-PWM-PD scheme has higher dc bus voltage utilization. Therefore, if both modulation schemes were designed such that they had the same maximum output voltage; the SFO-PWM-PD scheme would have higher sharing capability.

Fig. 5(c) shows the current sharing duty ratio for all modulation indices and ωt. Note that the maximum current sharing duty ratio over a switching cycle is 0.725 in this modulation scheme which happens at $m = 1.1547$ and $\omega t = 0°$.

D. Current Sharing in SFO-PWM-POD Scheme

In the SFO-PWM-POD modulation scheme, the same three reference voltages are used as the SFO-PWM-PD scheme, but the lower carrier signal is shifted by 180°, as shown in Fig. 4(d) (brown traces). In this modulation scheme, current sharing is always possible and the current sharing duty ratio is given in (9)

$$
d_{\text{share}} = min(|d_{\text{sa}}|, |d_{\text{sb}}|, |d_{\text{sc}}|). \text{ (9)}
$$

Assuming the modulation index $m = 0.9$ and $\omega t = 10°$, the sharing duty ratio is calculated to be 0.4617. The load current can be shared for 46.17% of the switching cycle. Considering having the same voltage at the output for the Sine-PWM-POD and the SFO-PWM-POD schemes, the modulation indices are calculated to be $m = 0.9$ and $m = 1.0392$, respectively. The calculated current sharing duty ratios are d_{share}=0.3078 and d_{share}=0.5284, respectively, which verifies the superiority of the SFO-PWM-POD scheme.

Fig. 5(d) shows the possible current sharing duty ratio over a switching cycle with the SFO-PWM-POD scheme for all modulation indices and ωt. Note that the SFO-PWM-POD scheme possesses the best current sharing duty ratios for all operating conditions in comparison with the aforementioned three PWM modulation schemes. The maximum current sharing duty ratio is 0.8625 and is achieved at $m = 1.1547$ and $\omega t = 0°$ in this modulation scheme. A comparison between these four modulation schemes in Fig. 5 illustrates that the SFO-PWM-POD scheme will provide larger current sharing duty ratio than other modulation schemes, leading to better overall performance of the proposed converter.

SECTION IV. Fault-Tolerant Operation for Open-Circuit Faults

In this section, the open-circuit faults of the power semiconductors that could occur to the proposed A₃L-ATT converter are investigated. Since the fault-tolerant strategies for open-circuit faults in Phase-B and C legs will be approached the same way as the Phase-A leg, open-circuit faults in the Phase-A leg will only be considered here. In addition, open-circuit faults in switches S_{a4}, S_{a3}, and S_{a6} are the dual of open-circuit faults in switch S_{a1}, S_{a2}, and S_{a5}, consequently, open-circuit faults of the latter will not be discussed here. Fault scenarios in the redundant leg switches S_{r4}, S_{r3}, and S_{r6} are the same as switches S_{r1}, S_{r2}, and S_{r5}, therefore, they are not going to be investigated in this section. In the following subsections, the individual fault scenarios will be discussed and appropriate recovery strategies will be introduced.

A. Open Circuit in S_{a1}

An open-circuit fault in S_{a1} will result in losing the P state in the Phase-A leg. To reclaim the P state, the switches S_{r2}, S_{r3}, S_{r5}, and S_{r6} of the redundant leg are turned OFF to disconnect the VNP from NP. Turning ON switch S_{r1} will reconfigure the P state path through the converter as shown in Fig. 6. Although turning ON the switch S_{r1} will recover the lost P state but the converter loses the ability to output an O state. In this case, the converter has the ability to output P and N states. Hence, it performs as a two-level converter with full modulation index.
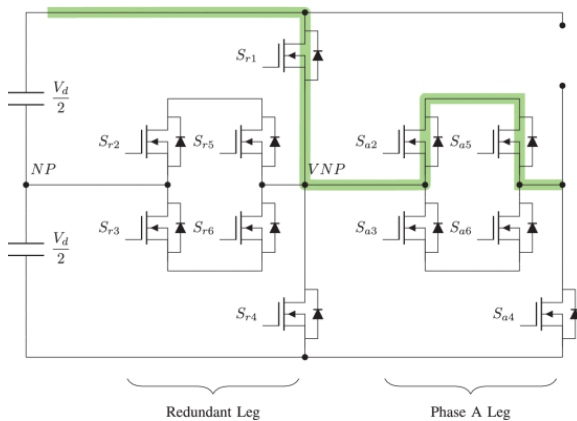

Fig. 6. Fault-tolerant operation for an open-circuit switch fault in S_{a1} at State P.

B. Open Circuit in S_{a2}

An open-circuit fault in S_{a2} will not cause any severe issues in the converter. Due to such a fault, the converter loses one of the parallel conduction paths at the O state which will result in a slight increase of conduction losses. Therefore, the converter can still operate three-phase three-level output voltages with full modulation index.

C. Open Circuit in S_{a5}

An open-circuit fault in S_{a5} causes similar consequences as the open-circuit fault in S_{a2}. The converter losses a parallel conduction path for the O state and can still generate three-level voltages with full modulation index.

D. Open Circuit in S_{r1}

An open-circuit fault in S_{r1} of the redundant leg eliminates the possibility to share current with other main phase legs at the P output state. However, the normal operation is unaffected and the converter can still produce three-phase three-level voltages at full modulation index.

E. Open Circuit in S_{r2}

An open-circuit fault in S_{r2} results in the loss of a parallel conduction path that connect the VNP to NP. The normal operation of the converter is unaffected and the converter experiences slightly more conduction loss in the NP current path.

F. Open Circuit in S_{r5}

Open-circuit fault in S_{r5} has the same effect as the open-circuit fault in S_{r2} . Therefore, the converter can maintain the three-level operation and full modulation index at the cost of slightly increased conduction loss.

# SECTION V. Fault-Tolerant Operation for Short-Circuit Faults

Short-circuit faults of one device at a time are considered in this section. The short-circuit fault scenarios are divided up between the three phase legs a, b, and c and the redundant leg. The short-circuit faults that appear in Phase-A leg are handled exactly the same as a short-circuit fault in Phase-B and Phase-C legs. Therefore, only the short-circuit faults in the Phase-A leg are considered here. Furthermore, short-circuit faults in S_{a1}, S_{a2}, and S_{a5} have dual fault scenarios in switches S_{a4}, S_{a3}, and S_{a6}, and thus the dual fault scenarios are not covered here. Finally, in the redundant leg, the short-circuit fault scenarios in switches S_{r1}, S_{r2}, and S_{r5} are covered. Considering the circuit symmetry, these switches have dual-fault scenarios with switches S_{r4}, S_{r3}, and S_{r6} will not be repeated.

A. Short Circuit in S_{a1}

Fig. 7(a) shows the A₃L-ATT converter with a short-circuit fault in S_{a1}. Turning ON the switches S_{a2}, S_{a3}, S_{a5}, and S_{a6} to output an O state will cause a short circuit of the upper dc bus capacitors. Fig. 7(b) shows the A₃L-ATT converter with a short-circuit fault in S_{a1} trying to produce an N state. Turning ON the S_{a4} to output state N will also cause a short circuit of the whole dc bus. The result of the short circuit in switch S_{a1} is the loss of states O and N at the output of Phase-A. The loss of O and N states results in a reduced modulation index and reduced output power.
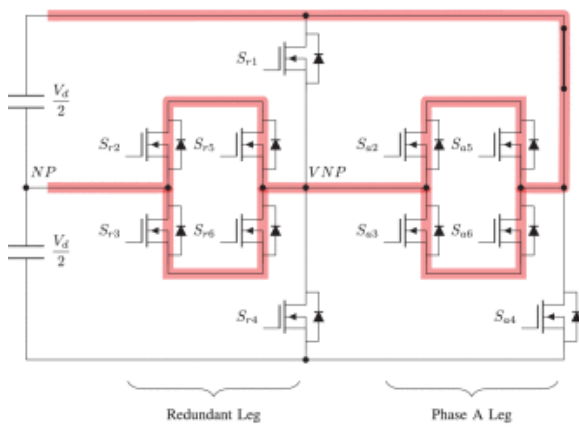
(a)
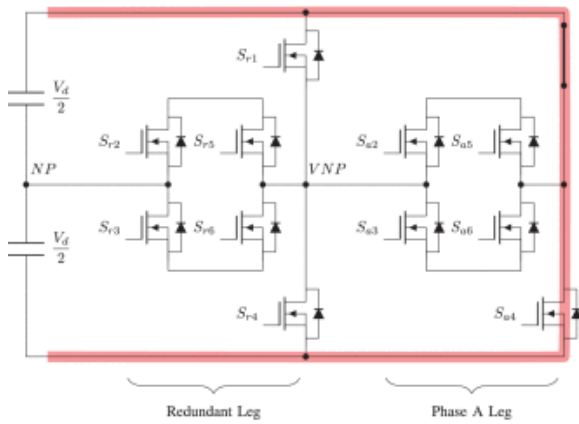
(b)

Fig. 7. Demonstration of potential short-circuit paths while having a short-circuit fault in S_{a1}. (a) Short-circuit fault in S_{a1} at State O. (b) Short-circuit fault in S_{a1} at State N.

B. Short Circuit in S_{a2}

Considering that in normal operation, the VNP is connected to NP through the redundant leg, a short-circuit fault in S_{a2} will cause a short circuit of the upper dc bus capacitors if the converter outputs any of the P states. As shown in Fig. 8(a), turning ON S_{a1} in order to have one of the P states will cause a short circuit of the upper dc bus capacitors. The solution is to disconnect the VNP from the NP. In this case, the converter regains the ability to output a P state in the faulty phase leg, but disconnecting the VNP from the NP makes it impossible to have the O state in the phase legs. Therefore, the converter can only output P and N states resulting in two-level operation but with full modulation index.
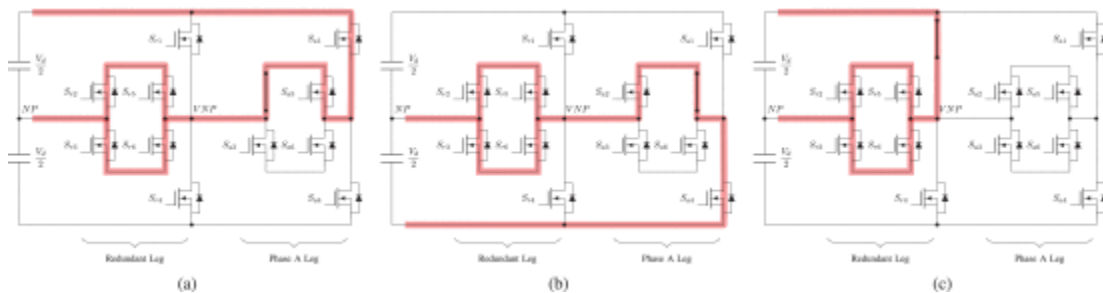

Fig. 8. Demonstration of potential short-circuit paths while having a short-circuit fault in S_{a2}, S_{a5}, or S_{r1}. (a) Short-circuit fault in S_{a2} at State P. (b) Short-circuit fault in S_{a5} at State N. (c) Short-circuit fault in S_{r1}.

C. Short Circuit in S_{a5}

Considering that in normal operation, the VNP is connected to NP through the redundant leg, short circuit in S_{a5} will cause a short if the converter outputs any of the N states. As shown in Fig. 8(b), turning ON S_{a4} in order to have one of the N states will cause a short circuit of the lower dc bus capacitors. The solution is to disconnect the VNP from the NP. In this case, the converter regains the ability to output N in the faulty phase leg but disconnecting the VNP from NP makes it impossible to have an O state in the phase legs. Therefore, the converter can only output P and N allowing full modulation index but in two-level operation.

D. Short Circuit in S_{r1}

Having a short-circuit fault in S_{r1} while the switches S_{r2}, S_{r3}, S_{r5}, and S_{r6} are ON will cause a shoot through of the upper dc bus capacitors, as shown in Fig. 8(c). The solution is to turn OFF the switches S_{r2} , S_{r3}, S_{r5}, and S_{r6} and disconnect the NP from VNP. Such action will allow the converter to function as two-level mode with full output power and modulation index.

E. Short Circuit in S_{r2}

Having a short-circuit fault in switch S_{r2} will cause a shoot through of the upper dc bus capacitors while trying to turn ON the S_{r1}. This fault will prevent the converter from performing current sharing while outputting a P state. The solution is to run the converter in normal operation without current sharing at P state. Current sharing with the N state is still maintained.

F. Short Circuit in S_{r5}

A short-circuit fault in switch S_{r5} will cause a shoot through of the lower dc bus capacitors while trying to turn ON the S_{r4}. This fault will prevent the converter from performing current sharing at output state N. However, current sharing at the state P is maintained. The solution is to run the converter in normal operation mode and only perform current sharing with the P state.

SECTION VI. Comprehensive Comparison With the Conventional T-Type Inverter

First, it is necessary to investigate the impact of the redundant leg on the inverter efficiency and compare it to the conventional T-Type inverter. To obtain the efficiency profiles of these inverters, thermal modeling of the switching devices has been conducted in PLECS simulation software. The simulation is conducted at an ambient temperature of 50 °C. In the simulation, the switching frequency of the inverter is set at 10 kHz, and the fundamental output frequency is 60 Hz. Also, the dc bus voltage is 600 V, and the rated output current is 18 A rms. CREE SiC MOSFETs C2M0025120D (1200 V/60 A) are employed to configure the inverter. The efficiency of the conventional three-level three-leg T-Type inverter and the proposed three-level four-leg A₃L-ATT inverter is simulated and compared at various output power percentages, as shown in Fig. 9(a). It can be seen that there is a slight efficiency degradation in the proposed A₃L-ATT inverter, compared with the T-Type inverter. For instance, at rated load condition (i.e., 100% load), the efficiency of the A₃L-ATT inverter is only 0.02% lower than the T-Type inverter. It should be noted that efficiency of both the inverters are based on the consideration of the total device losses and an assumption of 1% of inherent passive losses, which include filter losses and gate driver losses. There are three reasons that A₃L-ATT performs efficiently. First, the parallel connection of all the bi-directional middle devices produces lower conduction losses, compared to these in the T-Type inverter. Second, the middle bidirectional devices (S_{r2}, S_{r3}, S_{r5}, and S_{r6}) on the redundant leg are kept constant on to access the dc bus middle point, thus there are no switching losses in these devices. The total conduction losses of these middle devices are simulated and shown in Fig. 9(b), which shows that the conduction loss is only 8.3 W at rated load condition. Third, the conduction losses in the outer devices of the main phase legs of the A₃L-ATT

inverter are reduced due to the current sharing with the redundant leg at healthy condition. Fig. 10(a) shows the current sharing between the Phase-A leg and the redundant leg in both the positive and negative cycles at rated load condition. It can be seen that the redundant devices S_{r1} and S_{r4} share as much as 40% of the load current in the positive and negative cycles, respectively. In other words, the conduction losses in outer devices of the three main legs will be significantly reduced. Fig. 10(b) demonstrates such loss reduction by using the current sharing strategy with the SFO-PWM-POD strategy, compared to the losses in the outer devices in the conventional T-Type inverter. It should be noted that the outer devices in the conventional T-Type inverter dissipate more losses than the middle devices under the condition of positive power factor high modulation index condition. The current sharing capability of this proposed A₃L-ATT inverter will significantly relieve such thermal unbalance issue.
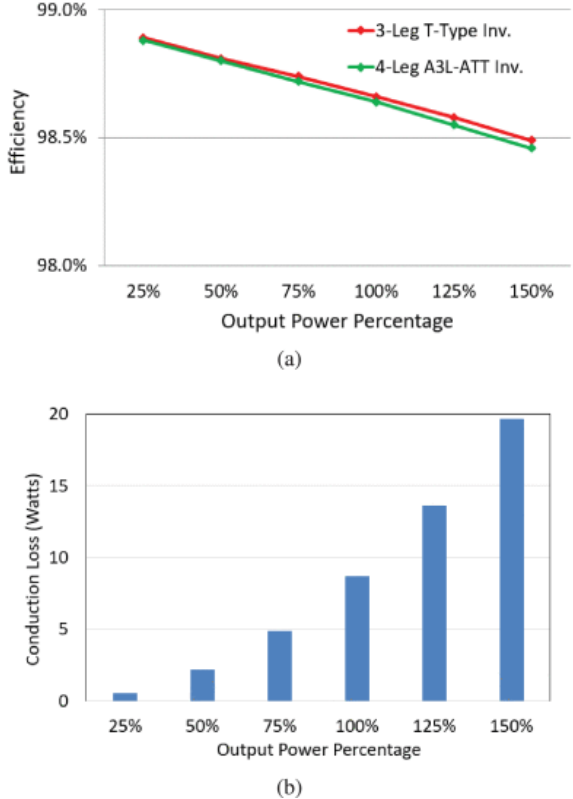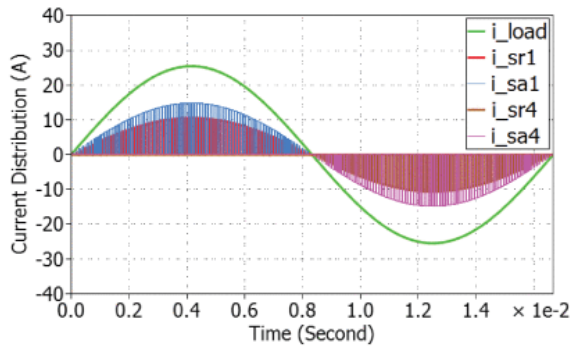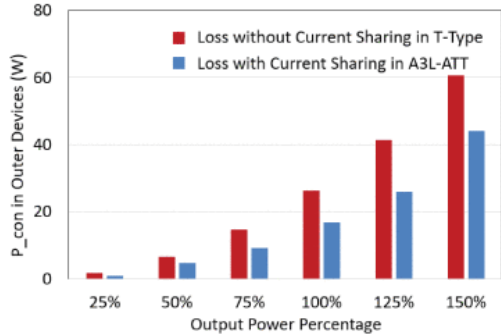

(a)

(b)

Fig. 9. Efficiency and device losses investigation in the proposed A3L-ATT inverter (ambient temperature: 50 °C). (a) Efficiency of A3L-ATT inverter versus the T-type inverter. (b) Conduction losses in all the middle redundant devices.

(a)

(b)

Fig. 10. Simulated current sharing in the proposed A₃L-ATT inverter and the related conduction loss reduction in its outer devices (ambient temperature: 50 °C). (a) Current sharing in the proposed A₃L-ATT inverter. (b) Total conduction loss reduction in the outer devices.

In addition to the efficiency comparison with the conventional T-Type inverter, all other main performance evaluation criterion such as device quantity, output power, total weight, total physical volume, fault-tolerant capability, and the balancing of loss distribution among devices are all comprehensively compared and shown in Table II. Note that the A₃L-ATT inverter has more enhanced fault-tolerant capability to both the open-circuit and short-circuit switching faults, while the output power and efficiency are similar. The addition of the redundant phase leg in the proposed A₃L-ATT inverter helps to share the overload current and eventually improve the loss distribution among the switching devices, while there is an uneven loss distribution in the conventional T-Type inverter which constrains its maximum output power and output frequency. All these performance benefits are simply achieved at the cost of adding one symmetrical phase leg. There is a slight increase in both the physical volume and weight for the proposed A₃L-ATT inverter, due to one additional phase leg and the redundant devices. In order to implement the associated fault diagnostic algorithm, one more current sensor is required to monitor the variations of the dc bus NP current. For the voltage sensing, similar to other three-level inverters in typical industrial applications, both the proposed A₃L-ATT inverter and the conventional T-Type inverter demand two voltage sensors on the dc side to monitor the balancing of dc bus voltages. Finally, it should be noted that this paper is targeted at the powertrain systems of generic EVs, in which the reliability and safety have higher priority to the cost.

TABLE II Comprehensive Comparison Between the Proposed A3L-ATT Inverter and the Conventional T-Type Inverter

| Evaluation Criterion	The Proposed A3L-ATT Inverter	The Conventional T-Type Inverter
Device Quantity	24 MOSFETs	12 MOSFETs
Output Power (kW)	13.5	13.5
Total Weight (kg)	2.15	1.7
Total Physical Volume (L)	3.31	1.50

Efficiency	98.73	98.75
Sensor Quantity	3 current sensors and 2 voltage sensors	2 current sensors and 2 voltage sensors
Microprocessor	TI DSP TMS320F28377D	TI DSP TMS320F28377D
GPIO	31	18
Tolerance to SC Fault	66.7%	No
Output Power during SC Fault-Tolerant Operation	Rated	Derated
Tolerance to OC Fault	100%	50%
Output Power during SC Fault-Tolerant Operation	Rated	Derated
Loss Distribution Among Devices	Balanced	Unbalanced

SECTION VII. Experimental Results

To verify the functionality of the proposed A₃L-ATT converter, a three-phase A₃L-ATT inverter prototype was designed and implemented in the laboratory, as shown in Fig. 11(a). The power switching devices used in the inverter prototype are SiC MOSFETs (Model No.: CREE C2M0025120D, rated at 1200 V/60 A). The microprocessor used in this prototype is a Texas Instruments digital signal processor TMS320F28377D. A three-phase *resistive-inductive* load in wye configuration, with a resistance per phase of $10\ \Omega$ and inductance per phase of $900\ \mu H$, is used as the load for this inverter. The dc bus voltage is 600 V, and the nominal output power in the test is 13.5 kW. The switching frequency is 10 kHz, and the output fundamental frequency and the modulation index are 60 Hz and 0.8, respectively.
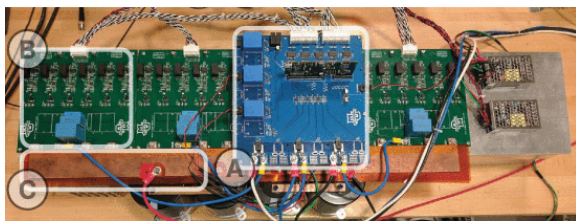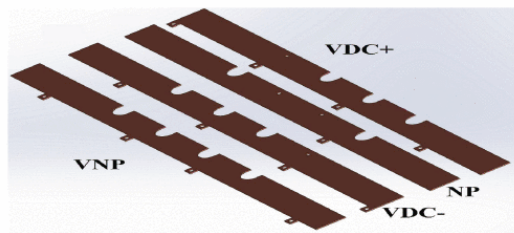
Fig. 11. Prototype of the customized three-phase SiC A₃L-ATT inverter. (a) Experimental prototype of the A₃L-ATT converter, (A) control board, (B) phase-A leg, (C) laminated dc bus bar. (b) Bus bar assembly.

There is a four-layer laminated bus bar structure designed to reduce the parasitic inductance of the commutation path, since high parasitic inductance will induce large switching voltage overshoots and the associated switching losses. The low-inductance bus bar structure is shown in Fig. 11(b). The bus bar assembly provides low inductance commutation path from dc-link capacitors to the switching devices. Also, the VNP and NP points on the different phase legs and the fault-tolerant leg are connected through the bus bars. Moreover, each phase leg has film decoupling capacitors with parasitic inductance of only a few nanohenries on the dc link to minimize the commutation loop inductance.

A. Short/Open-Circuit Faults

In the experiments, the A₃L-ATT inverter is programed to output three fundamental cycles of line currents and line-to-line voltages in normal operation, followed by another three fundamental cycles of faulty operation, and finally three fundamental cycles of fault-tolerant operation. This is in order to compare the variations of the inverter phase currents and line-to-line voltages under normal operation, faulty operation, and fault-tolerant operation. Two different modulation schemes are adopted in the tests, and the associated experimental results are acquired. All the fault scenarios presented in Fig. 12 are achieved at the SFO-PWM-PD scheme and all the other fault scenarios in Fig. 13 are achieved at the SFO-PWM-POD scheme.
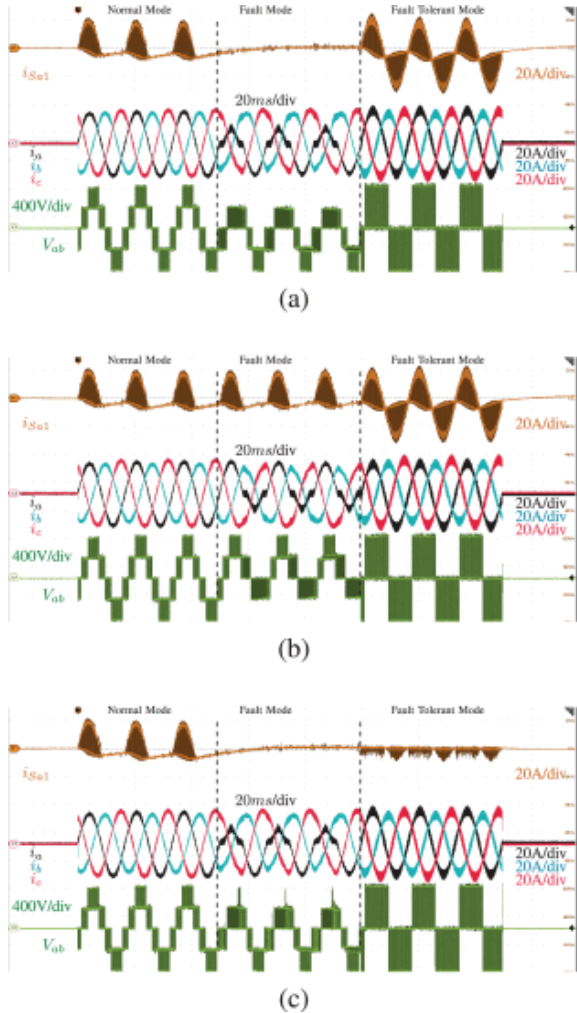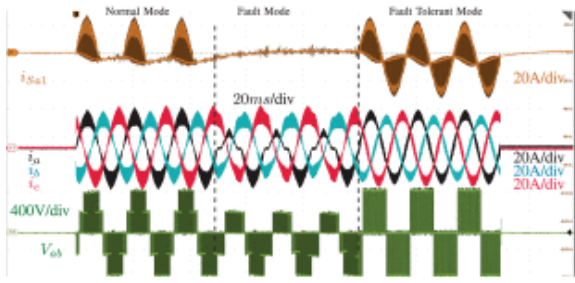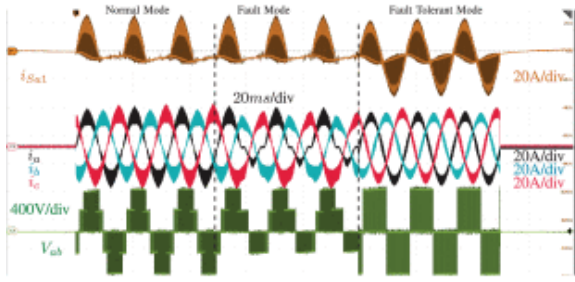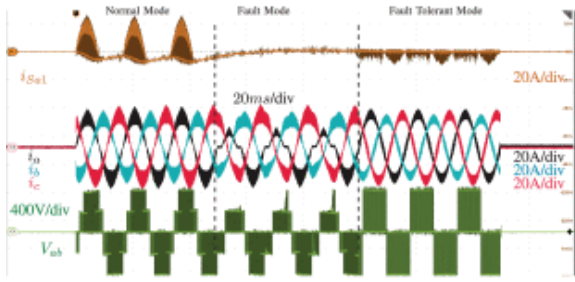

(a)

(b)

(c)

Fig. 12. Experimental results of the fault-tolerant operation of the proposed A₃L-ATT converter under various switching faults (SFO-PD modulation). (a) Short-circuit fault in S_{a2}. (b) Short-circuit fault in S_{a5}. (c) Open-circuit fault in S_{a1}.

Fig. 13. Experimental results of the fault-tolerant operation of the proposed A₃L-ATT converter under various switching faults (SFO-POD modulation). (a) Short-circuit fault in S_{a2}. (b) Short-circuit fault in S_{a5}. (c) Open-circuit fault in S_{a1}.

Fig. 12(a)–(c) illustrate the behavior of the converter under short-circuit fault in S_{a2} and S_{a5} and an open-circuit fault in S_{a1}, respectively. The converter is using the SFO-PWM-PD modulation scheme. Three-phase load currents are shown as i_a, i_b, and i_c. The current flowing through the S_{a1} is shown with i_{Sa1} and the line-to-line voltage between phase A and phase B is presented as V_{ab}. In all cases, the converter is reclaiming the output voltage with full modulation index in the two-level mode. Since the open-circuit fault in S_{a2} has no impact on the converter output performance, it is not necessary to demonstrate the related experimental results.

Fig. 13(a)–(c) depict the behavior of the converter under short-circuit fault in S_{a2} and S_{a5} and an open-circuit fault in S_{a1} , respectively. The converter is using the SFO-PWM-POD scheme. In all cases, the converter is reclaiming the output voltage with full modulation index in a two-level mode. The dc offset in the i_{Sa1} presented in Figs. 12 and 13 is due to the fact that the Rogowski coils used in the experiments cannot filter the 60 Hz low-frequency component. The noises in the i_{Sa1} waveform is caused by charging and discharging of the drain–source parasitic capacitance of the MOSFET devices. Furthermore, the load current total harmonic distortion (THD) for three-level waveform (SFO-PWM-PD scheme) is calculated to be 4.62%. Also, the load current THD for the two-level waveform is calculated to be 9.51%.

It should be noted that the open-circuit fault is implemented by interrupting the PWM pulse from that specific switch during experiments. The antiparallel body diodes of the MOSFETs do not pose any adverse effect on the

experiments. Handling a short-circuit current in the SiC MOSFETs is more challenging than the conventional Si insulated gate bipolar transistors. That is because the short-circuit current in SiC MOSFETs rises faster than that in the Si devices. Short-circuit behavior of the SiC MOSFETs are investigated in [14]–[15][16]. In [14], the authors explained the design procedure of a SiC MOSFET short-circuit protection that can act under 600 ns. The same de-saturation design process has been adopted to contain the short-circuit current in A$_3$L-ATT converter. After a short circuit in a switch is detected, the processor prevents the turn ON of any switches that can lead to a shoot-through fault that causes a waveform distortion in the output current. These cases have been illustrated in Figs. 7 and 8. This is the reason that there are not any considerable current spikes in the short-circuit output waveforms shown in Figs. 12 and 13. Also, showing the faulty mode of the inverter for three fundamental cycles (60 Hz) is only for illustration purposes. It is intended to show the distortion in the output current when a fault happens. The processor is capable of detecting a short-circuit fault in several microseconds and it can enable the inverter to enter the fault-tolerant mode immediately.

B. Current Sharing

Experimental waveforms for current sharing are provided in Fig. 14. In these results, current sharing is enabled at the P_{sh} state. The load current i_a is shown in green, the line-to-line voltage V_{ab} is shown in magenta, the current through switch S_{a1} is shown in blue, and the current through switch S_{r1} is shown in red. Two different current sharing paths are available as shown in Fig. 2. Fig. 14(a) depicts the experimental waveforms for current sharing using one path as shown in Fig. 2(a). Fig. 14(b) depicts the experimental waveforms for current sharing using two paths as shown in Fig. 2(b). Note that with both paths enabled, the current in I_{sh} is higher and i_{Sa1} is lower than that with one path enabled. Consequently, more current is being shared and the conduction losses in the SiC MOSFETs (S_{a1}, S_{a2}, and S_{a5}) are reduced.
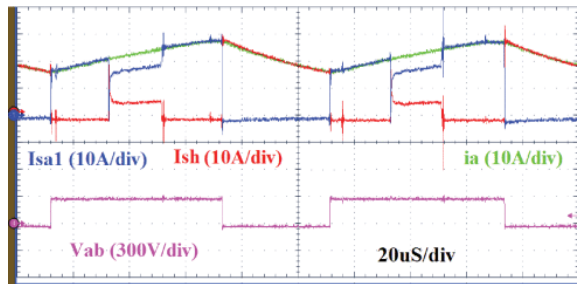
(a)
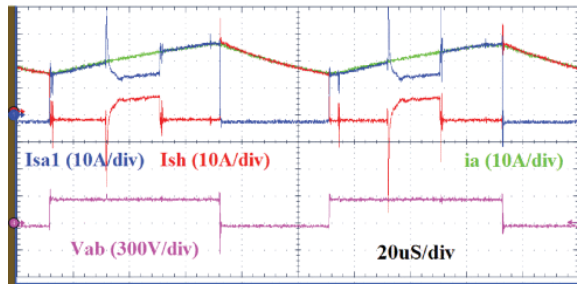
(b)

Fig. 14. Experimental results for current sharing between the redundant leg and the Phase-A leg by using one neutral path or two neutral paths. (a) Current sharing in 0° (one path). (b) Current sharing in 0° (two paths).

SECTION VIII. Conclusion

A novel fault-tolerant three-phase A$_3$L-ATT power converter topology is introduced in this paper. Fault-tolerant operation under different fault scenarios has been discussed. The topology can tolerate any open-circuit switching faults and most short-circuit switching faults, with the capability to output full voltages and currents

under the fault-tolerant operation modes. Furthermore, this new fault-tolerant topology has the ability of sharing current between the redundant leg and any of the main legs under normal healthy condition. Such current sharing increases the efficiency and the overload thermal capacity of the converter. Different modulation schemes for current sharing capability are investigated and the SFO-PWM-POD modulation strategy is proven to have the maximum current sharing duty ratio among the various modulation schemes investigated. Simulation and experimental results based on a 13.5-kW three-phase SiC A_3L-ATT converter prototype are provided, which verify all the theoretical expectations of this proposed converter. The introduction and development of this A_3L-ATT converter provides a promising fault-tolerant solution to power conversion in safety-critical applications, where the continuous operating availability of power converters under faulty conditions is given a higher priority to the system cost.

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