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Efficiency Improvement of Fault-Tolerant Three-Level Power Converters

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Abstract:

Fault-tolerant power converters play a critical role in the transportation electrification. However, fault-tolerant operation, high efficiency, and low cost usually result in design criteria that have conflicting constraints and goals. The majority of the fault-tolerant power converter topologies presented in the literature confirm these conflicts. In this paper, three types of fault-tolerant neutral-point clamped (NPC) converters are investigated. Various modulation strategies are explored to reduce the losses of the redundant phase leg. The simulation and

experimental results show that the Switching Frequency Optimal Phase opposition Disposition modulation strategy is the most effective approach in minimizing the losses in the redundant phase leg.

SECTION I. Introduction

In recent years, with the rapid development of transportation electrification, the demand for large capacity power converters has increased dramatically [1] . As an attractive solution to high power conversion, multilevel converters can withstand higher dc-bus voltage with lower harmonic distortions in the output waveforms [2] . Multilevel converters have been intensively employed in various medium-voltage high-power industrial applications. As reported in the literature, among the various multilevel power converter topologies, the Neutral Point Clamp (NPC) converter, including both the I-Type NPC converter and T-Type NPC converter, is the most widely used multilevel converter topologies in the industry. A derivative topology named Active Neutral Point Clamp (ANPC) converter has also been widely used in the industry in order to balance the loss distribution among the semiconductor devices.

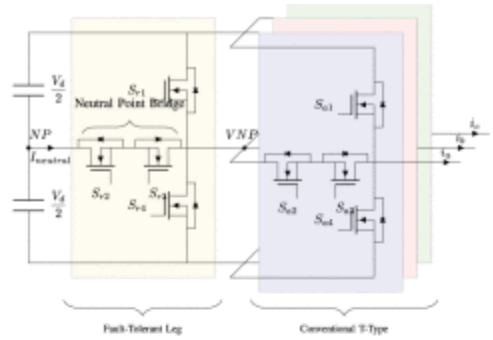
Reliability of power converters has been of paramount importance since the early stages of its development [3] , [4] . Since additional switches are utilized in multilevel power converters, the device failure probability might be higher in comparison to the conventional two-level converters. Various literature has been presented on the on-line diagnosis of switching faults in multilevel converters as well as the associated fault-tolerant operation during the post-fault stage [5] –[6][7][8][9][10][11][12] [13] .

Among the NPC multi-level converters mentioned above, the T-Type NPC converter has the least number of switching devices. Although the T-Type topology has some inherent fault-tolerant capabilities, the output voltage has to be decreased significantly during post-fault operation if any of the outer switches has an open-circuit fault [5] . Reduced output voltage is not desirable for safety-critical applications such as the propulsion systems for electric vehicles, electric aircrafts, and electric ships. In order to maintain full output voltage under fault-tolerant operation conditions, a fault-tolerant T-Type inverter has been introduced in [14] . As shown in Fig. la , a redundant and identical T-Type phase leg is added between the dc-bus capacitor bank and the conventional T-Type inverter. In this topology, the fault-tolerant leg is operated as a back-up when there is a device failure in any of the main phase legs. In addition, the redundant phase leg can be leveraged to share overload current and achieve soft-switching under normal operating conditions. The novel fault-tolerant topology enables the T-Type converter to be more resilient against open-circuit or short-circuit faults, at the cost of an additional phase leg. As it can be seen from Fig. la, due to the necessity of providing the neutral point potential, the two middle switches of the redundant leg, i.e., S_{r2} and S_{r3}, are constantly on during normal operation. As a result, the full neutral-point current always flows through these two switches under normal operation, generating significant conduction losses from the neutral-point bridge (NPB), which may cause thermal stress on these two middle devices as well as decreasing the efficiency of the T-Type converter. The fault tolerant topologies shown in Fig. lb and Fig. lc are called A3L-ANPC and A3L-ATT, respectively. These converters are having a neutral point current path through the fault tolerant leg similar to the aforementioned fault tolerant t-Type converter. This paper will investigate the mitigation of the conduction losses in the NPB through the use of different modulation strategy on the various fault-tolerant topologies shown in Fig. 1 .

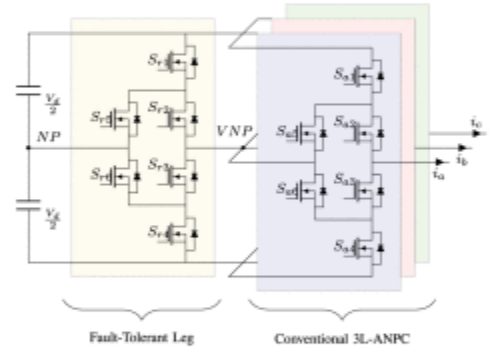
The remainder content of this paper is organized as follows: in Section II , the characteristics of the neutral-point current flowing through the NPB under various modulation strategies will be analyzed. In Section III , simulation results comparing the neutral-point current and the associated losses will be presented. In Section IV , experimental results shows the neutral-point current in each NPC fault-tolerant topology will be shown. Finally, conclusions and discussions will be given in Section V.

SECTION II. Analysis of Neutral-Point Current

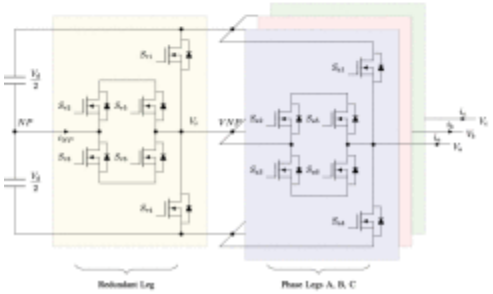
The fault-tolerant three-phase four-leg T-Type converter topology shown in Fig. la was originally introduced in [14] . The complete operating principle is described in reference [14] and will not be repeated here. This topology consists of three T-Type phase legs depicted as blue, red, and green in Fig. la, and finally an additional phase leg, depicted in yellow in Fig. la, is located in the front end of the converter. The common neutral point connection of the three phase legs is named the Virtual Neutral Point (VNP). The VNP is connected to the actual DC bus neutral point (NP) through the two middle switches of the redundant leg. Under normal operating conditions, these two switches on the NPB, S_{r2} and S_{r3}, are kept constantly on, to connect to the NP, while S_{r1} and S_{r4} are kept constantly off during normal operating condition. The NPB switches, which are located between the VNP and the NP, produce significant conduction losses under normal operation in comparison with the conventional T-Type converter.



(a) Fault-tolerant T-Type converter



(b) Fault-tolerant A3L-ANPC converter

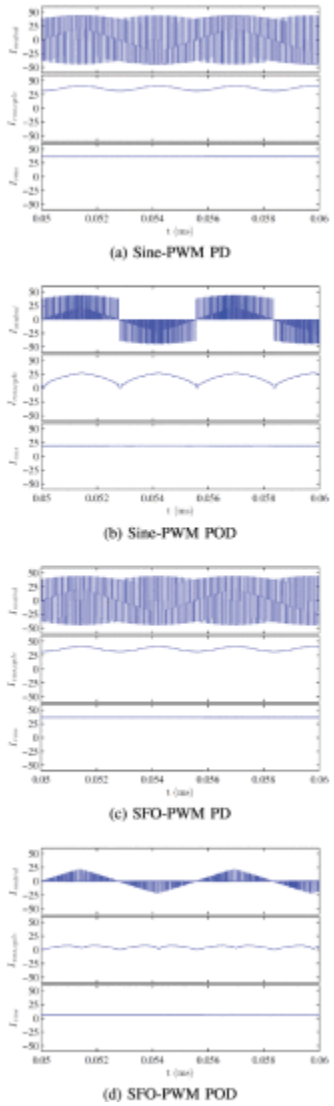


(c) Fault-tolerant A3L-ATT converter

Fig. 1. Fault-tolerant Three-level power converter topologies

In order to reduce the conduction losses in the NPB, various modulation methods are investigated in this work in an effort to find a method that has minimal increase on conduction losses compared to the traditional multilevel converter topologies. In the literature, the average neutral point current has been intensively investigated in an effort to balance the DC bus voltage [15] , [16] . However, in this paper, due to the high stress placed on switches S_{r2} and S_{r3} due to the RMS current which flows through these switches, the rms current in the NPB will

be thoroughly investigated in order to find a method to minimize the RMS current. The rms current rating of these two switches will be determined for various modulation methods and compared to other switches in the topology.



(a) Sine-PWM PD

(b) Sine-PWM POD

(c) SFO-PWM PD

(d) SFO-PWM POD

Fig. 2. Simulated neutral point current of the fault-tolerant T-Type converter under various modulation methods

To investigate the loss mitigation in the NPB, four carrier-based modulation schemes are considered in simulation to determine the rms neutral point current flowing through the NPB switches. The four modulation schemes under investigation here includes Sine-PWM in-phase disposition (PD), Sine-PWM phase opposition disposition (POD), Switching Frequency Optimal PWM (SFO) in-phase disposition (PD), and Switching Frequency Optimal PWM (SFO) phase opposition disposition (POD) [17] , [18] . The switching frequency of the modulation scheme is defined in (1) , and the output voltage frequency is defined in (2) . The neutral point current (RMS value) is calculated over a switching frequency period (3) and a fundamental output period (4) . Two distinct neutral-point RMS currents are calculated to understand the thermal cycling in the NPB semiconductor switches due to the low frequency nature of the rms current. Additionally, the current rating of the semiconductor device can be determined. The neutral point current, $I_{neutral}$, and the two rms currents, $I_{rms,cycle}$ and I_{rms}, are shown in Fig. 2 for the various modulation methods. The currents for the Sine-PWM PD and the SFO-PWM POD modulation methods are shown in Fig. 2a and Fig. 2d , respectively. As it can be seen, the neutral point current is smaller in SFO-PWM POD compared to the other three modulation methods under investigation here. Likewise,

the RMS currents in SFO-PWM POD are significantly lower than that in Sine-PWM PD method. This indicates that the conduction losses in the NPB switches, S_{r2} and S_{r3} , will be much lower with the SFO-PWM POD modulation strategy.

The nautral point current (RMS) is plotted in Fig. 3 vs modulation index and load power factor for the various modulation schemes. The simulation is done in PLECS by running the simulation for 900 different operation points. Note that the maximum modulation index for SFO modulation references are 1.15 which enables more voltage utilization of the converter. The simulation results show that the SFO-PWM-POD scheme shown in Fig. 3d is the minimum rms current of the all modulation schemes in all the modulation indices and load power factor. It is obvious that the simulation data makes the converter to be able to switch between the modulation schemes in order to balance the losses in the converter.

$$f_{sw} = \frac{1}{T_{sw}}$$

$$f_{out} = \frac{1}{T_{out}}$$

$$I_{rms,cycle} = \sqrt{\frac{1}{T_{sw}} \int_{t_o}^{t_o+T_{sw}} I_{neutral}(t)^2 dt} \quad (1)(2)(3)(4)$$

$$I_{rms} = \sqrt{\frac{1}{T_{out}} \int_{t_o}^{t_o+T_{out}} I_{neutral}(t)^2 dt}$$

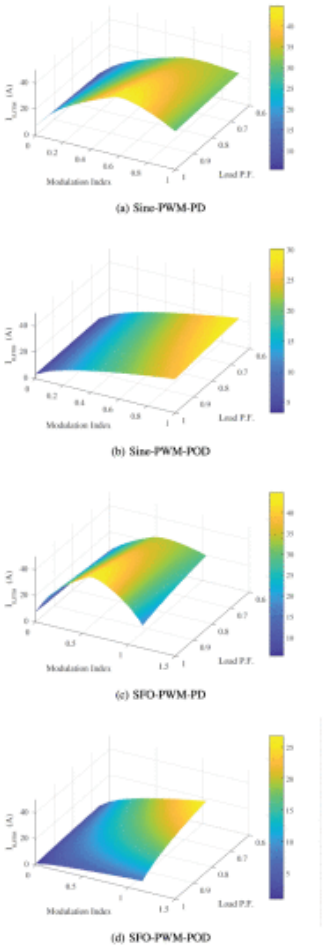


Fig. 3. Neutral-point RMS current versus various modulation indices and power factors under different modulation schemes

TABLE I Experimental Parameters of the Fault-Tolerant Converter Prototypes

Converter	Fault Tolerant T-Type	A3L-ANPC	A3L-ATT
Switching Freq. (kHz)	10	10	10
Output Freq. (Hz)	60	60	60
DC-Link Voltage (V)	600	1000	600
Output Power (kW)	15	25	13.5
Ambient Temp. (C)	20.5	20.5	20.5
Load Resistance (ohms)	5	5	5
Load Inductance (uH)	900	900	900
SiC MOSFETs	C2M0040120	C2M0040120	C2M0025120

SECTION III. Experimental Verification

A prototype of the fault-tolerant T-Type converter topology shown in Fig. 1a is implemented by using SiC MOSFETs from Cree/Wolfspeed (C2M0040120D, 1200V/40A). Prototypes of the A3L-ANPC and A3L-ATT are shown in Fig. 5 and Fig. 6 . The experimental parameters used for these prototypes are shown in Table I .

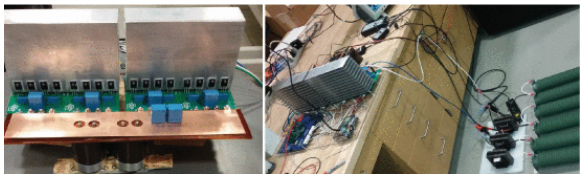


Fig. 4. Experimental prototype of the fault tolerant t-type converter

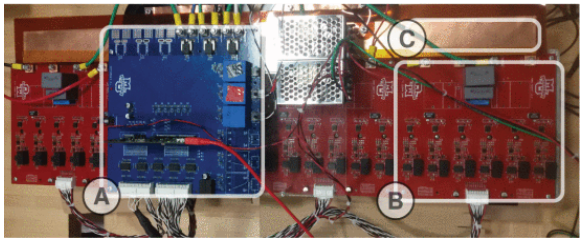


Fig. 5. Experimental prototype of the customized A3L-ANPC converter, (A) control board, (B) Phase-A leg, (C) the dc-bus bar

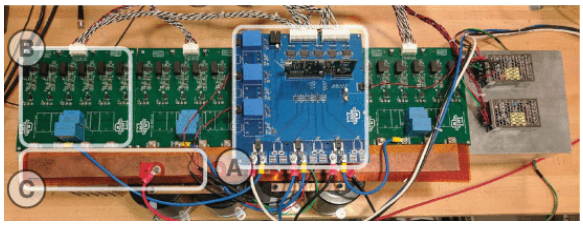
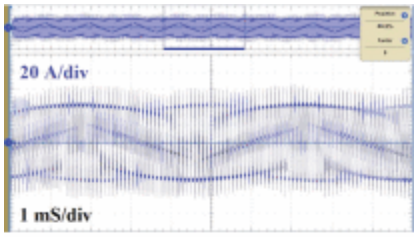
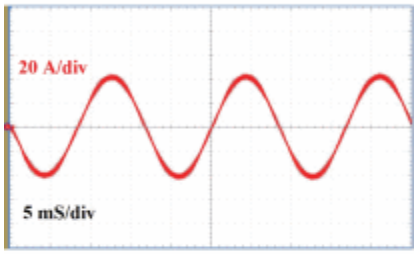


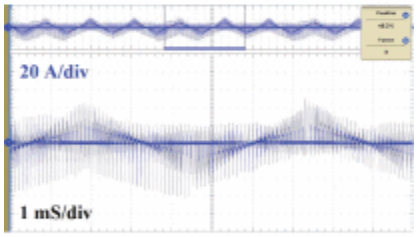
Fig. 6. Experimental prototype of the A3L-ATT converter, (A) control board, (B) Phase-A leg, (C) the dc-bus bar



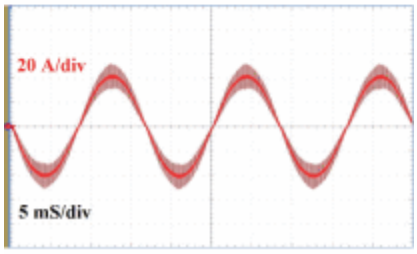
(a) Neutral-point current with Sine-PWM PD (20A/div)



(b) Load current (Phase-A) with Sine-PWM PD (20A/div)



(c) Neutral-point current with SFO-PWM POD (20A/div)



(d) Load current (Phase-A) with SFO-PWM POD (20A/div)

Fig. 7. Experimental waveforms of neutral-point-current and load current under different PWM schemes

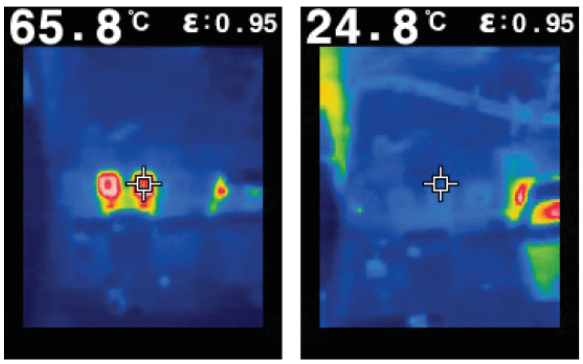
To verify the simulation results, the measured neutral-point current and load current waveforms from the experimental setupZX are shown in Fig. 7 at approximately 15kW of output power. The measured neutral point current waveforms with the Sine-PWM-PD and the SFO-PWM-POD modulation methods are shown in Fig. 7a and Fig. 7c , respectively. For comparison purposes, the current supplied to the load in both of the two modulation methods are kept the same. The load currents for Sine-PWM-PD and SFO-PWM-POD are measured and shown in Fig. 7b and Fig. 7d , respectively. The experiment results show that the neutral point current obtained with the SFO-PWM-POD is much smaller than that with the Sine-PWM-PD method, which confirm the prior analysis from the simulation results. In other words, SFO-PWM-POD is superior to the other modulation methods in terms of ensuring minimal RMS current through the NPB switches S_{r2} and S_{r3} resulting in minimized conduction losses.

Thermal images of the NPB switches (S_{r2} and S_{r3}) are captured during the experiments by using a FLIR thermal imaging infrared camera. Figure 8a shows the infrared image of the middle switches S_{r2} and S_{r3} modulated by the Sine-PWM-PD method. It can be seen that the case temperature of the switches is 65.8°*C* after running the inverter with approximately 15kW of the load for a short period of time. Similarly, Figure 8b shows the infrared image of the same switches modulated by the SFO-PWM-POD method, which demonstrates that the case temperature is 24.8°C after operating the converter for a long period of time so that steady state of the thermal

cycling can be obtained. By visual inspection of these infrared images, it is obvious that the neutral point current flowing through the S_{r2} and S_{r3} is much lower when using the SFO-PWM POD modulation method.

SECTION IV. Conclusions

The RMS current of the Neutral Point Bridge was investigated with the purpose of improving the efficiency of the fault-tolerant three-level power converter. Four different modulation methods were considered and the neutral-point currents were obtained for each modulation method. Simulation results determined that RMS current in the NPB is significantly lower when using SFO-PWM POD method, in comparison to the three other modulation methods. Prototypes of the fault-tolerant power converter topologies were implemented and the related experimental results were obtained. The experimental results validated the simulation results and confirmed that the SFO-PWM POD is the most effective modulation method in minimizing the neutral-point current and the associated conduction losses in the NPB switches. Moreover, thermal inspection of NPB switches S_{r2} and S_{r3} in the converter proved that the neutral-point current (RMS) and the related thermal stress is much lower if the converter is modulated by the SFO-PWM POD method.



(a) Sine-PWM PD (b) SFO-PWM POD

Fig. 8. Infrared Images of the NPB switches S_{r2} and S_{r3} at 15kW load under various modulation methods

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