4-2006

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IEEE Transactions on Industrial Electronics, Vol. 53, No. 2 (April 2006): 521-529. DOI.

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Abstract:

Accurate prediction of temperature variation of power semiconductor devices in power electronic circuits is important to obtain optimum designs and estimate reliability levels. Temperature estimation of power electronic devices has generally been performed using transient thermal equivalent circuits. In the presence of

varying load cycles, it has been typical to resort to a time-domain electrical simulation tool such as P-Spice or SABER to obtain a time series of the temperature profiles. However, for complex and periodic load cycles, time-series simulation is time consuming. In this paper, a fast Fourier analysis-based approach is presented for obtaining temperature profiles for power semiconductors. The model can be implemented readily into a spreadsheet or simple mathematical algebraic calculation software. The technique can be used for predicting lifetime and reliability level of power circuits easily. Details of the analytical approach and illustrative examples are presented in this paper.

SECTION I. Introduction

Design of power electronic systems involve numerous tradeoffs as is common in most engineered systems. It proceeds through a careful selection process for various parameters and technologies starting with the electrical design and culminating in manufacturing process design. The electrical-design phase results in the selection of power electronic circuit components, which is relatively mature and well established. However, rendering well-conceived electrical designs into reliable and low-cost products suitable for any application requires a substantial amount of additional engineering effort. The physical design proceeds further beyond the electronic circuit design, accounting for magnetic devices, current densities, dielectric isolation requirements, semiconductor power losses, thermal management methods, thermomechanical stresses, die-attach processes, electromagnetic interference, etc. Aforesaid factors that affect the design are coupled through complex interrelationships. Design activity encompasses several engineering domains including magnetic, electrical, mechanical, thermal, material processing, and manufacturing sciences.

Traditionally, these conditions lead to a serial approach toward product design and development. Issues related to electromagnetic design, electrical design, materials selection, mechanical layout, electromagnetic interference (EMI), thermal management, manufacturing process development, reliability, and cost strategies are addressed sequentially and often sadly in an isolated manner. By nature, such a serial process is plagued by concealed and competing tradeoffs, which obscure the path toward an optimal solution. Unfortunately, it is virtually impossible to make objective design decisions based on unified analytical solutions. Nevertheless, as economic pressures to meet stringent performance/cost ratio keep mounting, the need for a better understanding and visualization of the design space is being felt. It is therefore crucial to fill these gaps in knowledge and integrate them into the power electronics design process. Only then can modern enterprise practices like integrated product and process development be successfully applied to the field of power electronics, leading to cost reductions and performance improvements.

This paper represents a small step toward solving this fundamental issue in power electronics systems by proposing a simple evaluation tool to analyze the thermal properties of power electronics designs in a fast and accurate manner. Simple solutions of thermal equivalent circuits that are commonly used to predict maximum junction temperatures become less useful for predicting lifetime and reliability figures accurately when the operating load cycles are complicated and the design needs to be optimized for particular load cycles.

Finite-element analysis (FEA) tools can be used for obtaining detailed thermal profiles. They are generally based on computational fluid dynamics (CFD) programs such as the finite-volume method. However, for most applications, the use of FEA is limited by its difficulty of use and length of calculation time, and furthermore, the accuracy of most models have not been definitively established [1]. Many publications have implemented a time-domain electrothermal simulation of the thermal circuit concurrently with the electrical simulated circuit using time-domain circuit simulation tools [1]–[2][3][4][5][6]. However, under long time-load cycles, time-domain simulation becomes very cumbersome. The Federal Urban Driving Schedule (FUDS) cycle would be impractical to perform loss calculations using commercial electrical simulation packages due to the immense

amount of time required [7]. Furthermore, the time-series results have limited use in developing lifetime predictions.

An analytical method to evaluate transient junction temperature of semiconductor devices using Fourier techniques in frequency domain is presented in this paper. Simple mathematical analysis computer software that can solve basic mathematical functions can be used to implement the model. Frequency-domain analysis procedure resolves problems for applications with long testing cycles by modeling the effects of complicated load cycles in a relatively short amount of time. In Section II, the basis of the approach is presented using simple benchmarks. Section III validates the approach with experimental data. An application example based on a hybrid electric vehicle application is presented in Section IV. Application of results from the analytical approach toward reliability estimation is outlined in Section V, which is followed by a section with concluding remarks.

SECTION II. Fourier Analysis Methodology

A. Thermal Equivalent Circuit Analysis

Thermal analysis of power converter systems begins with determination of device power losses using device characteristics and load profile of the power converter. Once the device power losses have been established, determination of junction temperature requires knowledge of the thermal equivalent circuit. When analyzing thermal effects from a time-dependent load profile, both thermal resistance and thermal capacitance values are required to properly solve for the time-varying junction temperature.

The best, but most complicated, thermal circuit to use is the transmission-line equivalent circuit, commonly called the T-model thermal resistance–capacitance (RC) circuit. Fig. 1(a) shows an example of the T-model thermal RC circuit for an insulated gate bipolar transistor (IGBT) module representing closely the physical heat-transfer phenomenon actually occurring. In Fig. 1(a), T_j corresponds to the physical junction temperature, T_{DCB} corresponds to the physical direct copper bonding (DCB) temperature, and so on.

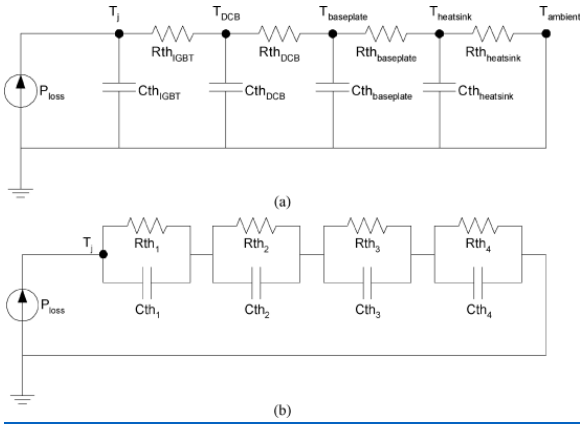

Fig. 1. Possible (a) T-model thermal equivalent circuit and (b) π-model thermal equivalent circuit for IGBT module.

The degree of accuracy depends on the number of RC combinations that are used in the thermal model. Generally, more RC combinations allow for a greater accuracy of multiple frequency phenomena. Because the transmission model represents the continuous distribution of thermal RC, each RC combination in Fig. 1(a) can be broken into more RC blocks. For an example, the thermal RC for the DCB layer of the IGBT could be broken into four RC circuit layers corresponding to the copper, substrate, copper, and solder layers of the physical device.

The π -thermal model is the most typical and easiest thermal model to obtain and is commonly found in manufacturer data sheets [8]. The π-thermal model only shows explicit junction and ambient temperatures. Intermediate nodes do not reflect the temperature at various layers in the module. Shown in Fig. 1(b) is the equivalent π -thermal RC model. Contrary to the T-model, no reference is made of actual thermal RC values, but rather, a generic numbering system is used. The junction-to-ambient thermal response in the π -thermal model is equivalent to the T-model; however, no knowledge exists of each layer in the physical device. The advantage of the π -thermal model is the ease of obtaining it compared with the complexity of obtaining the T-thermal model. There are many techniques available for determining accurate T- and π -thermal models for power devices [1]–[2][3][4][5][6] and [9]–[10][11][12].

The implementation of thermal profiling using Fourier techniques can use either the T- or π -models. Whereas the T-model retains one-to-one correspondence to the actual physical device, the π -model has fictitious nodes unrelated to the physical device and hence can be used only when the junction temperature is required. The frequency-domain representation of the thermal impedance of the system is required for application with the Fourier analysis technique presented in this paper. Fig. 2 shows the thermal impedance over frequency for the TO-247 package MOSFET used in the analysis in Sections II and IV and was derived from the π -model given by the manufacturer [8]. The π -model is appropriate because only junction temperature variations are required in this analysis.

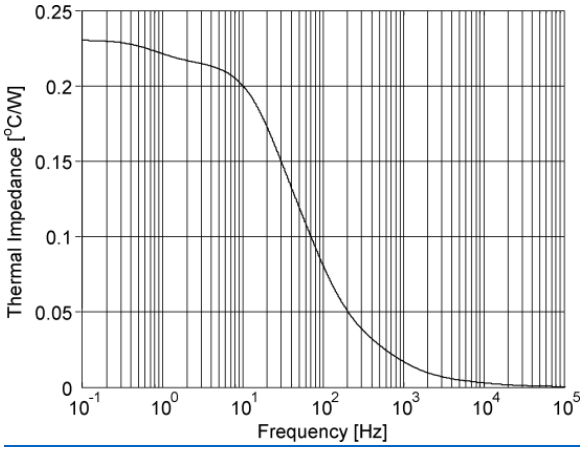

Fig. 2. Thermal impedance frequency plot of TO-247 MOSFET under test.

It is important to note that this thermal model technique still leaves several nonlinear phenomena, for instance, heat spreading, voids, crack propagation, inhomogeneous temperature distribution on the chip caused by the influence of the bond wires, and second-order effects [1], [13], [14]. However, their effects may be included through further modification of the technique using multidimensional networks and Fourier solutions of the heat-flow equations.

B. Fourier Analysis

The proposed technique transforms the time-dependent device power loss waveform to a frequency-dependent representation. The advantage of working in the frequency domain is that a long period of a load cycle can be simulated relatively quickly once represented as distinct frequency components. The Fourier exponential coefficients can be easily calculated and transposed into the exponential Fourier form as

$$a_k(k) = \frac{2}{T_0}\int_0^{T_0} P_{\text{loss}}(t)\cos(k\omega_0 t)dt$$

$$b_k(k) = \frac{2}{T_0}\int_0^{T_0} P_{\text{loss}}(t)\sin(k\omega_0 t)dt$$

$$C_n(k) = \frac{a_k(k) - jb_k(k)}{2}$$

(1)(2)(3)

where $P_{\text{loss}}(t)$ is the time-domain power loss function, ω_0 is the fundamental frequency of the power loss time function, and T_0 is the fundamental period.

With the power losses transposed into frequency domain, they can be easily combined with the thermal impedance using

$$T_{\text{jk}}(k) = C_n(k)Z_{\text{tot}}(k)$$

(4)

where $Z_{\text{tot}}(k)$ is represented by Fig. 2 to produce the frequency-domain representation of junction temperature.

To obtain the junction temperature profile in time domain, the frequency-domain coefficients can be transformed back into time domain using

$$T_j(t) = \sum_{k=-\infty}^{\infty} T_{\text{jk}}(k)e^{jk\omega_0 t}.$$

(5)

In a practical case, an infinite number of harmonics is not possible for the Fourier transformation. However, the accuracy of this transformation increases with the number of harmonics. When only insufficient data points are available, various interpolation techniques can be performed to increase the accuracy of the results by increasing the number of data points in the original data.

C. Simulation Validation Example of Fourier Technique

The thermal equivalent impedance illustrated in Fig. 2 is used for validation of the proposed rapid thermal profiling technique. Junction temperature variations to a sinusoidal power excitation, specifically, were predicted using a circuit simulation tool, SaberSketch, as illustrated in Fig. 3(a), and the results are shown in Fig. 3(b) [15]. The junction temperature was then determined using the proposed techniques, implemented using Matlab and Mathcad, whose results are shown in Fig. 4 [16], [17]. Although both Matlab and Mathcad produced identical results to the SaberSketch thermal circuit simulation, the Matlab process was faster than both other techniques using a known input function. This time difference only becomes greater when a long time-load cycle is introduced.

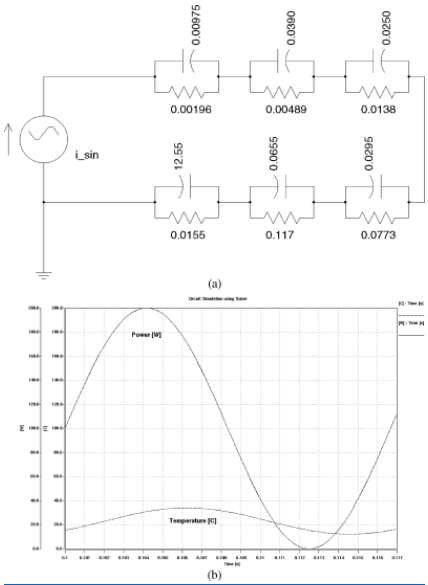

Fig. 3. (a) SaberSketch π -thermal equivalent circuit from junction-to-case of TO-247 MOSFET device under test. (b) Thermal simulation result (only a few seconds to simulate).

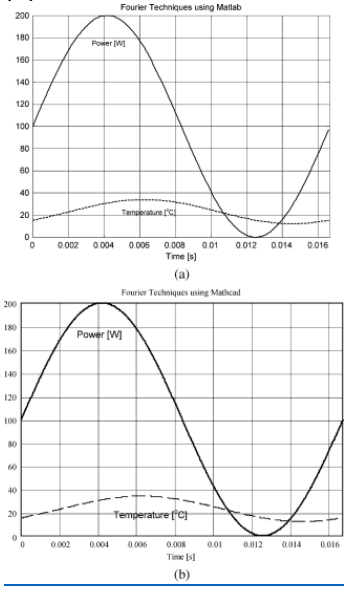

Fig. 4. (a) Using FFT method in Matlab to produce the same output as the SaberSketch equivalent circuit model (computation time was a fraction of a second to simulate). (b) Using FFT method in Mathcad to produce the same output as the SaberSketch equivalent circuit model (computation time was nearly 3 min to simulate).

The effects of thermal capacitance play an important role in time-varying loads. Fig. 5 illustrates the comparison of only considering a resistive thermal model and the complete resistive and capacitive thermal model. In both situations, the average T_j are identically $23.05°C$. However, average T_j does not provide adequate information to make proper reliability and maximum temperature analysis. When the thermal capacitance is ignored, the T_j has a temporal difference of over $45°C$. Using the more accurate model with thermal capacitance, the T_j difference lowers to below $25°C$. This has a significant impact on the reliability analysis of the power device.

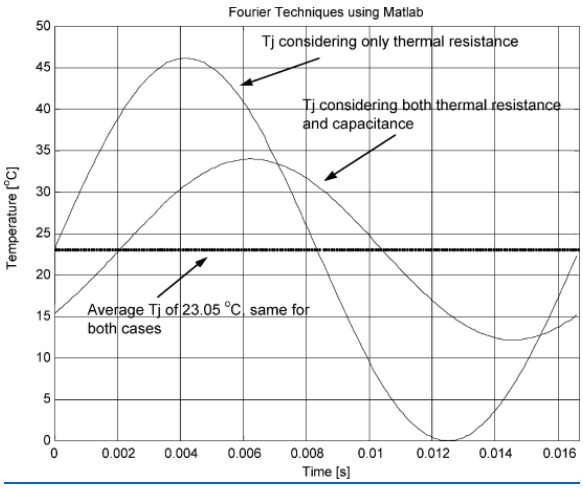

Fig. 5. Comparison of time-varying load simulation with and without thermal capacitance. Both considerations have the same average T_j of $23.05°C$.

SECTION III. Experimental Validation of the Fast Fourier Transform (FFT) Method

The described FFT method has been validated with experimental measurements. A half-bridge configured Fuji IGBT power module with two IGBTs and two antiparallel diodes was used in the validation [18]. The IGBT and diode power loss equations used are based on standard electrical loss models [19] and are used along with data from the manufacturer's data sheets. The power module input was 600 V_{DC} with a 1.2- Ω resistive load. The switching frequency was time dependent and could range from 5 to 15 kHz. The measured current and calculated power losses are shown in Fig. 6(a). The thermal lump parameter model shown in Fig. 6(b) was derived from an FEA thermal model and experimental validation of the test bed [20].

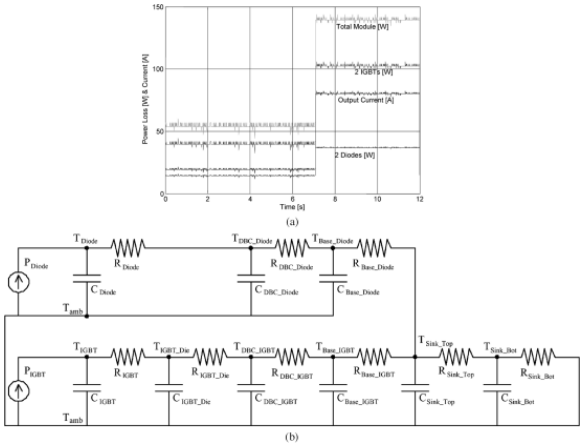

Fig. 6. (a) Diagram of the calculated power losses and the measured output current of the IGBT module. The top waveform corresponds to the total calculated power loss, the next corresponds to both IGBT calculated power losses, the next waveform to the measured output current, and the bottom waveform to both diode calculated power losses. (b) Equivalent thermal T-model for diode and IGBT used in evaluation [20].

Fig. 7(a) shows nearly perfect agreement between the experimental junction temperature and the calculated junction temperature using the FFT method. Because of the fast nature of this method, the effects of changing the heat sink can easily be performed without much effort. With a 100 times increase in the heat sink thermal

capacitance, the temporal temperature delta lowers by less than $1°C$. A 50% reduction in the heat sink thermal resistance provides nearly $20°C$ drop in absolute maximum temperature, but presents roughly no change in the temporal temperature delta. Fig. 7(b) shows the simulated effect of ignoring the spatial temperature effect from the antiparallel diode.

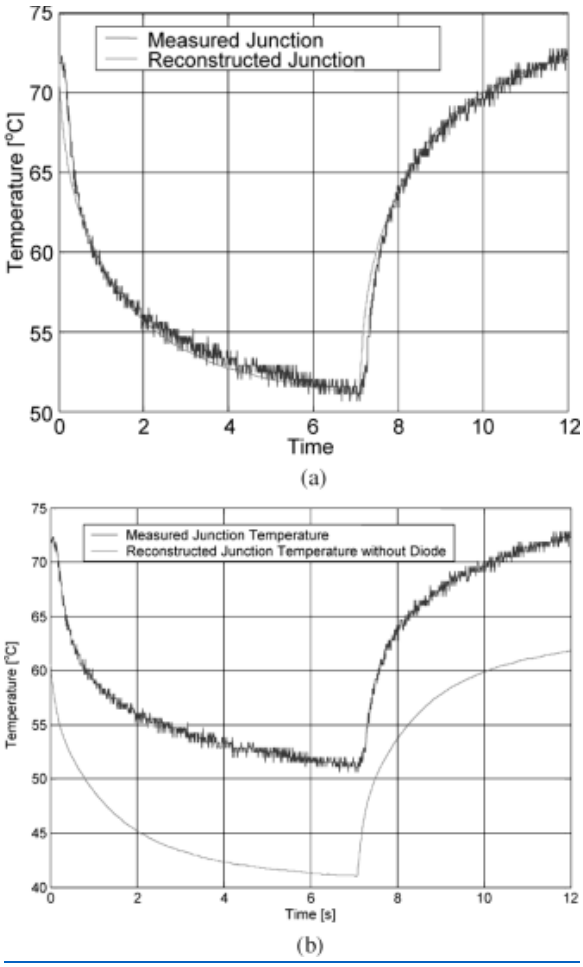

Fig. 7. (a) Measured IGBT junction temperature compared with calculated IGBT junction temperature using the FFT method. (b) Comparing the effect of simplifying the model such that the spatial temperature effect of the diode is ignored.

SECTION IV. Practical Case for Hybrid Electric Vehicles

This rapid temperature profiling technique is ideally suitable for many applications with long testing cycles such as machine tool spindle drives, elevator drives, and automotive driving cycles. The example presented here focuses on the application of the technique to a hybrid electric vehicle drive. The drive uses a three-phase converter feeding an interior permanent magnet starter–alternator machine with a 42-V power system [21]. The converter consists of six power switches composed of two devices in parallel per switch producing a total of 12 MOSFET devices with 12 antiparallel body diodes. The simulated load profile is the FUDS cycle shown in Fig. 8 and is composed of the Urban Dynamometer Driving Schedule (UDDS) repeated by the first 505 s, again of the UDDS. Using the load profile in Fig. 8 in combination with power speed curves, the output mechanical speed, power factor, and power are calculated [21].

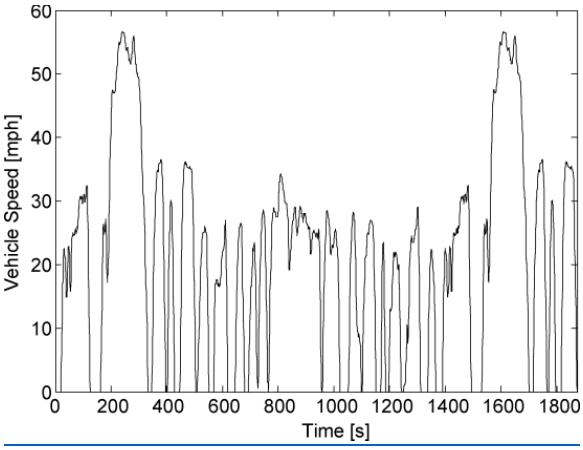

Fig. 8. The Federal Test Procedure (FTP) made up of the UDDS repeated by the first 505 s, again of the UDDS.

From these output values and information regarding the devices from the data sheets, the power losses for each device can be calculated as shown in Fig. 9 [7], [22]. The power loss waveforms in Fig. 9 represent the total losses of the MOSFET and body diode for one of the devices in parallel. Because of a varying modulation index and power factor, power loss analyses of the top and bottom switches of the inverter leg are computed separately. In this particular case, the machine has an efficiency of 90% and the inverter of 92%. The heat sink was assumed to be a constant temperature sink maintained at the liquid coolant's temperature of $0°C$ to monitor relative temperature, rather than absolute temperature, with infinite heat rejection.

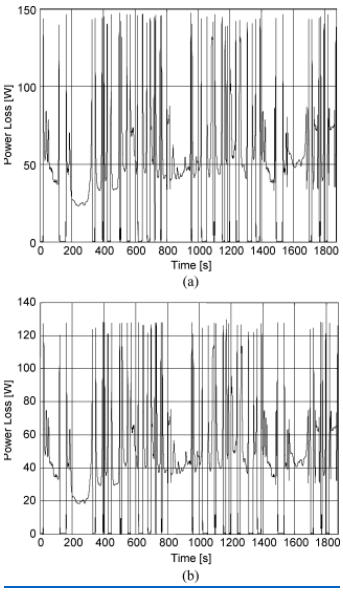

Fig. 9. Power losses for a single MOSFET/body diode device from the (a) top and (b) bottom switches.

Fig. 10 shows the reconstructed variation of junction temperature as a function of time during a FUDS cycle using the Fourier techniques described previously. Because of the required modulation index and power factors, the top switches produce slightly larger junction temperatures. The results indicate a maximum temporal junction temperature delta of $34°C$ produced under the given load cycle for the top devices. The maximum temporal junction temperature delta for the bottom devices was $29°C$, composing a spatial junction temperature difference of $5°C$ between the top and bottom switches. Because the heat sink in the simulation was preformed assuming infinite heat rejection, spatial temperature difference has no influence. In a real heat sink, the location of the devices plays an important role in spatial junction temperature in which temperatures

of one device can affect other devices in close proximity. Once the heat sink temperature is known, an absolute maximum junction temperature evaluation can be conducted.

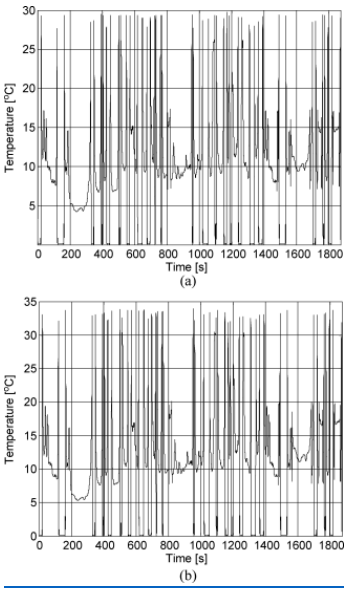

Fig. 10. Junction temperature for a single MOSFET/body diode device from the (a) top and (b) bottom switches.

This application was modified to accommodate a real heat sink as previously shown in Fig. 6. In this case, spatial temperature effects were considered only for a diode and MOSFET, but not for any other devices. Fig. 11 shows the MOSFET junction temperature, assuming an ambient temperature of $25°C$, of the top leg of the inverter with the same power losses shown in Fig. 9(a). In this case, the maximum temperature is approximately $92°C$, and the maximum temporal junction temperature delta increased to $63°C$.

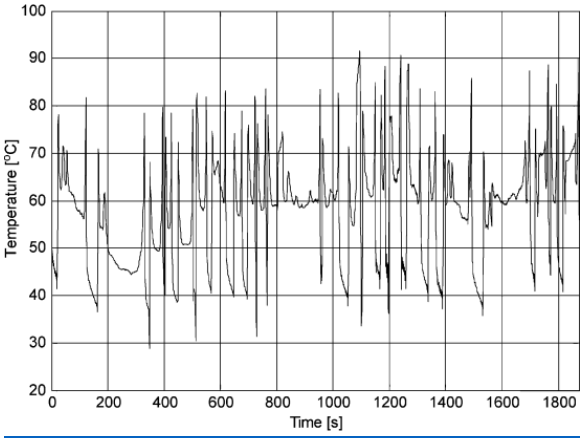

Fig. 11. Junction temperature for a single MOSFET/body diode device from top switches utilizing the thermal model of Fig. 6 and at $25°C$ ambient temperature.

SECTION V. Reliability Analysis

The number of power cycles attainable from a power module is a measure of reliability. As illustrated in Fig. 12, at a mean temperature of $80°C$, a device would not be expected to fail for over 2 million power cycles if the temporal junction temperature variation is less than $40°C$ [23]. Examination of the junction temperature variation of the device from Fig. 10 shows that there are about 60 cycles over a period of 1800 s. Assuming that the vehicle is driven for 3 h per day, it can be estimated that the device would see 2 million cycles at the end of

15 years. Thus, the results in Fig. 10 used with Fig. 12 suggest that the lifetime of the power devices is typically greater than that of the vehicle. These results are consistent with other investigations of power devices showing that a temporal junction temperature delta under $40°C$ results in highly reliable IGBT module power cycling [20]. However, increased number of hours of operation and highway driving cycle, etc., would affect the lifetime estimate considerably depending on the corresponding junction temperature variations.

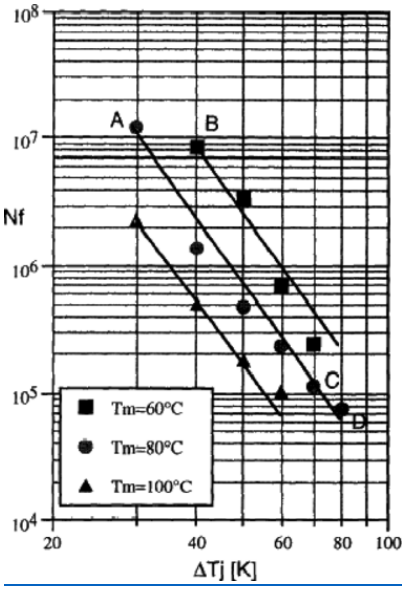

Fig. 12. Power cycling results for IGBT module showing the number of cycles to failure N_f as a function of mean temperature T_m and delta junction temperature ΔT_j [23].

SECTION VI. Conclusion

This paper has presented a fast thermal profiling method of power semiconductor devices using Fourier techniques. The method relies on the use of the classical transient thermal equivalent circuit to predict junction temperature variations in the presence of varying load cycles common with power converters. Transient thermal impedances developed from such equivalent circuits have been used in the past for thermal design under pulsed loading of semiconductors. They have also been used in conjunction with time-domain simulation techniques to obtain a time-series solution of junction temperatures. On contrast, the approach presented here uses a frequency-domain representation of the semiconductor power loss along with the thermal equivalent circuit to represent the temperature profile also in the frequency domain. The model can be implemented using general-purpose mathematical analysis software. A practical load cycle example of a hybrid vehicle application was used to demonstrate the application of the technique. Although only MOSFETs were used in the illustrative example, the technique can be extended for analysis of other devices and more complex geometries of thermal management systems. The technique can be used in conjunction with Fourier methods for heat conduction and convection studies to develop fast solutions of thermal system to allow optimization of design parameters. Furthermore, statistical analysis techniques can be coupled with the frequency-domain model to obtain reliability distributions.

ACKNOWLEDGMENT

The authors thank the Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC) and the Graduate School of the University of Wisconsin, Madison, for providing support for the project and D. Murdock from the University of Wisconsin, Madison.

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