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Abstract:

A novel hybrid circuit breaker for medium voltage dc (MVDC) electric shipboard power systems is proposed. The breaker combines the benefits of the efficiency of a mechanical breaker and the interruption speed of a solid-state breaker. The proposed breaker utilizes a fast-ramping current source with a fast-actuating vacuum interrupter (VI) to provided ultra-fast response time and high on-state efficiency. During normal operation, nominal load current flows through the vacuum interrupter in the main conduction branch, providing a low-resistance path with negligible losses. During a fault, a current zero crossing is achieved by the use of a controllable resonant current source (RCS). By leveraging the high switching frequency capabilities of Silicon Carbide (SiC) devices, the current source achieves higher frequency of resonance than previously possible with the silicon counterparts. After interruption, the surge arrester in the energy absorption branch clamps overvoltages and dissipates all residual system energy. Simulation results from the PLECS software environment are presented to verify the functionality of this proposed breaker in a 20 kV MVDC system for electric shipboard applications.

SECTION I. Introduction

Medium voltage dc (MVDC) systems have been proposed as a promising technology in future aircraft and shipboard systems [1] [2]. MVDC has several advantages over conventional ac systems such as reduced cable weight and cost, improved efficiency due to the elimination of ac losses, and higher power density. A significant technical barrier for the widespread implementation of MVDC is the challenge of developing suitable circuit protection. Regardless of how fast two current-carrying switch contacts open, an arc will be established that will continue to conduct. This arc requires a current zero crossing to quench and establish an open circuit. In a conventional ac system, circuit breakers (CB) rely on repetitive current zero crossings inherent to the system. For instance, for a 60 Hz system, a zero crossing occurs every 8.3 ms. In a dc system, no such zero crossings exist, so artificial zero crossings must be produced to guarantee fault interruption. Furthermore, the impedance due to system inductance is minimal at dc, so any short circuit currents increase more rapidly than in ac systems. Therefore, it is necessary to achieve interruption within a few milliseconds [3].

There are several different solutions on the market that do not provide adequate protection. In [4] [5], a passive resonant dc CB is presented, and its topology is shown in Fig. 1(a). It utilizes the resonance of reactive elements in parallel with the mechanical switch in the conduction branch to achieve current zero. Since the sole device in the conduction branch is the mechanical switch, this CB has the benefit of high efficiency. However, due to the time needed to build up the resonant current, this topology suffers long interruption times of typically 10-100 ms [6]. Fig. 1(b) shows the general topology of a purely solid-state CB [7] [8]–[9]. Due to the use of semiconductor switching devices in the main conduction path, this CB can interrupt currents within 100 µs. Nonetheless, this breaker has high on-state losses resulting in low efficiency, due to the fact that a number of semiconductor devices are typically series connected for blocking the high dc voltage. The conventional hybrid CB [10], shown in Fig. 1(c), is a compromise between purely mechanical and solid-state breakers. The number of semiconductor devices, such as Insulated Gate Bipolar Transistors (IGBTs), in the main conduction path is reduced and used alongside a mechanical switch. Current commutation is aided by semiconductor devices in parallel with the conduction path. Therefore, the interruption time is decreased to several

ms and the on-state losses are reduced, but they still are not negligible. In this paper, a novel resonant hybrid CB is proposed that achieves ultra-fast interruption time and high efficiency. Its general topology is shown in Fig. 1(d), where it features a vacuum interrupter for high on-state efficiency and a parallel resonant current source module to achieve zero crossings, which will be elaborated next.

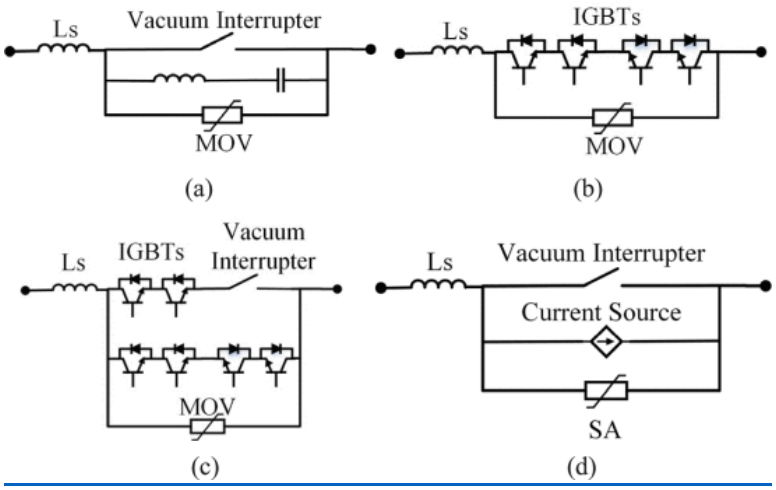

Fig. 1. Circuit breaker topologies: (a) mechanical passive resonant, (b) solid state, (c) conventional hybrid, and (d) proposed resonant breaker.

SECTION II. Operating Principle

A. Modes of Operation

The detailed topology of the proposed breaker is provided in Fig. 2. This breaker has three branches: commutation, main conduction path, and energy absorption. During normal operation, the nominal steady state load current will flow through the vacuum interrupter (VI) in the main conduction path. Since the vacuum interrupter has very low contact resistance, the breaker's losses during this time are negligible. The resonant current source(RCS) modules in the commutation branch do not conduct any current during this time, and the surge arrester (SA), or array of arresters, in the energy absorption branch appear as a high impedance. No fault has occurred yet, so only a negligible leakage current will flow through the energy absorption branch, appearing as a near-open circuit. Once a fault occurs (i.e., the dc bus is shorted) the CB begins its fault operation. The line current will flow through the VI and increase only being limited by the line resistance and inductance. The VI is commanded to open, and as its mechanical contacts spread apart an arc is established across them. This creates a low-resistance path for the fault current to still flow; current will continue to flow unless this arc is quenched. The purpose of the RCS module is to oppose this fault current and quench the established arc. The equation for the current through the interrupter at this time is:

$$i_{sw} = i_{load} - i_{res}$$

(1)

- i_{sw}: main conduction branch current
- i_{load}: line current to load
- i_{res}: resonant commutation current from the RCS

The currents generated by the RCS and flowing through the vacuum interrupter are shown in Fig. 3(a). It is apparent by equation (1) that the current through the VI will be zero if the RCS current is to meet the magnitude of the fault current. In doing so, an artificial zero crossing is forced in the VI current. This quenches the arc and allows the VI to become an open circuit and withstand the nominal voltage of the dc bus. The fault has now been interrupted and the breaker enters post-fault operation. The RCS now ceases its oscillations. Because of the interruption in current, an overvoltage is induced by the line inductance. If this overvoltage was allowed to occur unhindered, the CB would likely be damaged and there would be a danger that the arc could reestablish, thus resuming the fault. Therefore, the duty of the SA is to clamp this overvoltage and dissipate all residual energies still left in the system, namely from the line and resonant components in the RCS. This clamping can be seen in Fig. 3(b). Once the knee voltage of the SA is surpassed, the arrester will clamp at this voltage and conduct significant current. Once all leftover energy is dissipated, the voltage across the CB returns to the nominal bus voltage and the SA in the absorption branch appears again as a near-open circuit. At this point, the fault is considered fully isolated.

The construction of the proposed breaker is done in modules to easily scale to any system rating. For instance, Fig. 2 depicts a breaker with two RCS modules in parallel. This doubles the fault current capabilities of the CB. Likewise, a higher voltage rating can be achieved by adding more SAs in the energy dissipation branch.

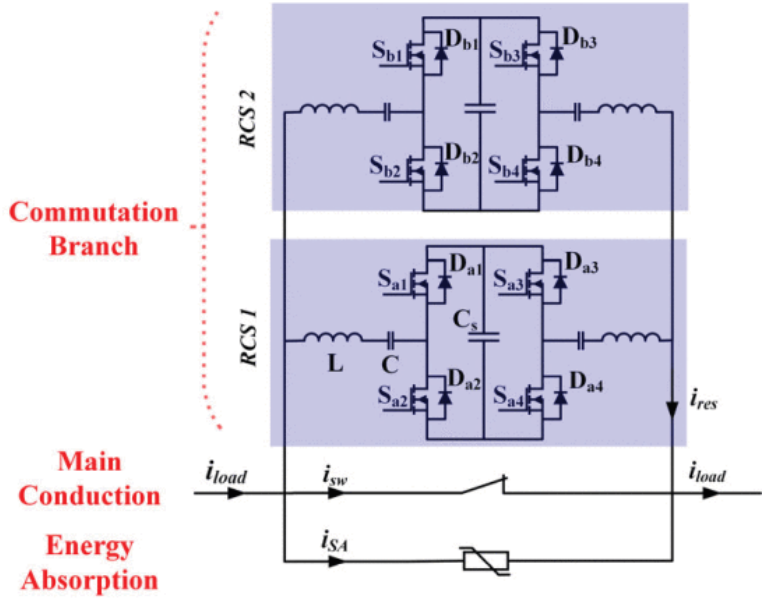

Fig. 2. Modularized parallel RCS Hybrid CB showing the labels of each parallel branch.

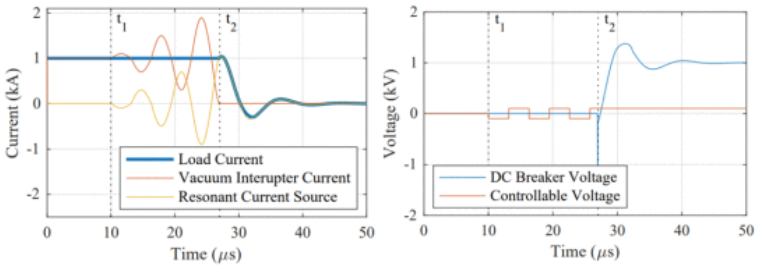

Fig. 3. RCS and CB operation, (a) fault interruption currents, and (b) pre and post interruption voltages.

B. Resonant Current Source Commutation

The topology of the RCS modules can be viewed in Fig. 2 under RCS 1 and RCS 2. The circuit is composed of resonating inductors and capacitors, an H-bridge configuration, and a source capacitor. The source capacitor, denoted C_s, is preemptively charged to an initial voltage before a fault. The H-bridge then alternatively applies this voltage at the damped radian frequency of the resonant components, denoted as L and C, to create the fast ramping commutation current. This alternating voltage can be seen in Fig. 3(b). The high switching frequency capabilities of SiC allow for high resonant frequencies, and consequently, ultra-fast response time as well as physically small inductors and capacitors. The damped radian frequency can be calculated as:

$$\omega_d = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}$$

(2)

$$\alpha = \frac{R}{2L}$$

(3)

- ω_d: damped radian frequency (rad/s)
- L: equivalent inductance of RCS (H)
- C: equivalent capacitance of RCS (F)
- R: equivalent resistance of RCS (Ω)
- α: damping constant

Once excited by alternating voltages, the current through the RCS will oscillate and its magnitude will grow linearly with time. Each half period of this resonance is referred to as a reversal of current. Depending on the choice of source capacitance, resonant components, and on-resistance of switching devices, the magnitude will eventually saturate and start to decrease at a certain high number of reversals. It is preferable that the RCS successfully interrupt the fault within the section that the oscillation appears to grow linearly. The time at which the first peak occurs, and all subsequent peaks, is given by the following:

$$t_{peak,1} = \frac{1}{\omega_d} \arctan\left(\frac{\omega_d}{\alpha}\right)$$

(4)

$$t_{peak}(n) = (n-1)\frac{\pi}{\omega_d} + t_{peak,1}$$

(5)

- $t_{peak,1}$: 1^{st}, reversal peak (s)
- $t_{peak}(n)$: n^{th} reversal peak (s)
- n: corresponding peak number

The magnitude at each reversal peak can be defined by:

$$i_{peak}(n) = B(n)e^{-\alpha t_{peak,1}} sin(\omega_d t_{peak,1})$$

(6)

$$B(n) = \frac{V_d(-1^{n-1}) - V_c(n-1)}{L\omega_d}$$

(7)

- $i_{peak}(n)$: magnitude of n^{th} reversal peak (A)
- $B(n)$: underdamped ringing coefficient

Larger magnitudes of commutation current can be achieved by either increasing the number of reversals performed or by increasing the initial source voltage. By increasing the number of reversals the required initial voltage will decrease, and vice versa. The equation that describes the peak-by-peak voltage stored in the source capacitor is:

$$V_c(n) = B(n)\frac{1}{C}\frac{a)d}{\alpha^2 + \omega_{d^2}}(e^{-\alpha\frac{\pi}{\omega_d}} + 1) + V_c(n-1)$$

(8)

- $V_c(n)$: source capacitor voltage (V)

SECTION III. Modeling of Key Breaker Components

High fidelity modeling is essential to validate the performance of the proposed resonant hybrid CB during the transient and steady states. The modeling of key components (e.g. SiC devices, VI, and SA) are detailed in following sections.

C. SiC Devices-Thermal Modeling

It is important to model the thermal performance of the SiC switches, as the maximum fault current capabilities are limited mainly by the maximum junction temperature of the devices. Using the information specified on the Cree CAS325M12HM2 (1. 2kV, 256 A continuous) half-bridge module datasheet [11], a thermal model was created that takes conduction losses, switching losses, and transient thermal impedance into consideration.

In operation, the lifetime and efficiency of the CB is dominated by the normal operation mode (e.g. nominal load current flows through VI). Fault operation is a very small proportion of the CB lifetime, therefore the losses and efficiency during this phase can be neglected. Instead, the safety and reliability during fault interruption must be analyzed to ensure minimal damage or thermal stress occurs. In the simulation, the worst case scenario is used in which the ambient temperature is set at 50°C.

The maximum allowable junction temperature listed on the datasheet is relatively high at175°C. To leave sufficient safety margin, the junction temperature of the devices is limited below 100°C. Due to the nature of the resonant current waveform generated, where the devices switch at each current zero, conduction dominates the losses. This creates a tradeoff between the number of current reversals by the RCS and the specified peak current. Utilizing more reversals causes higher peak junction temperatures, increases the ramping time of the RCS, and decreases the initial source voltage required. For a given fault current, the reversal count should be chosen such that it does not create damaging conditions for the device. If too few reversals are used, then the initial source voltage will exceed the SiC devices' rated drain-to-source voltage. If too many are used, then the peak junction temperature will exceed the rated maximum. It should also be noted that the suitable number of reversals possible is limited by when the RCS current saturates This is dependent on the choice of resonant capacitors and inductors.

Per each leg of the RCS H-bridge, two Cree half-bridge SiC devices are employed in parallel. This limits the junction temperature of the devices below 100°C and ensures safe fault operation.

D. Vacuum Interrupter - Black Box Arc Modeling

For dc conditions above a few tens of amperes and a few volts, an arc will be established across two current carrying contacts separating [12]. Though the contacts are separated, the current will flow through this arc and will continue to do so until quenched. It is crucial that the arcing time is kept to an absolute minimum. The longer an arc is established the greater the damage to the surfaces of the metal contacts of a switch [13]. When contacts are first separated, a molten bridge of contact material connects the separate surfaces. Eventually, as the contacts continue to separate, this bridge will rupture and release metal vapor into the surrounding medium (i.e. air, SF6, vacuum, etc). This metal vapor provides the conditions for the arc to first establish. After this, the arc may stabilize to a columnar or diffuse arc. If the medium inside the interrupter is gaseous, then it will convert to a low-resistance plasma through which current flows. Once stable, the arc will appear as a low voltage drop.

This behavior is physically complex and largely stochastic. Despite this, electrical models exist that simplify the arc's behavior and replicate the effects they have on a circuit's current and voltage. Black box arc models make it possible to analyze arcing phenomena (i.e. arc resistance, voltage transients, failure to quench, etc.). There are many models that vary in their accuracy and complexity. In their general form, they describe the arc as a voltage dependent conductance. This relationship can be easily manipulated with Ohm's Law to represent the arc as a voltage dependent current source. The Mayr and Cassie models are two popular and widely-used models which have many derivatives that improve upon them. The models are based on a series of assumptions and the energy conservation principle [14]. The equation for the Cassie model is given as follows:

$$\frac{1}{g}\frac{dg}{dt} = \frac{1}{\tau}\left(\frac{u_{arc}^2}{u_0^2} - 1\right)$$

(9)

- g: arc conductance (S)
- τ: arc time constant (s)
- u_{arc}: instantaneous arc voltage (V)

- u_0: arc reference voltage (V)

The equation for the Mayr model is as follows:

$$\frac{1}{g}\frac{dg}{dt} = \frac{1}{\tau}\left(\frac{gu_{arc^2}}{P_{out}} - 1\right)$$

(10)

- P_{out}: cooling power of the arc (W)

The Mayr and Cassie model can be thought of as complimentary to each other. Some derivative models exploit this relationship to increase accuracy. The Mayr model is most suited for high voltages arcs in the low current regime, below 500 A in vicinity of current zero. The Cassie model is most suited for high voltage arcs in the high current regime, above 500 A and away from current zero. These models are heavily simplified descriptions of arcing, so they are not very quantitatively accurate and do not replicate experimental data well. Instead, they are good qualitative descriptions of how arcs behave and affect circuits [15].

The Schwarz model is one such widely used derivative that improves on both the Mayr and Cassie models. It can be thought of as a combination of the two models; both the Mayr and Cassie equations can be found by changing parameters of the Schwarz model. Also, the Schwarz model is flexible enough to perform well in both the high and low current regimes [16]. Schwarz model's equation and assumptions [17] are:

$$\frac{1}{g}\frac{dg}{dt} = \frac{1}{\tau_0 g^{\alpha}}\left(\frac{gu_{arc}^2}{P_0 g^{\beta}} - 1\right)$$

(11)

- P_0: constant factor of cooling power (W)
- τ_0: constant factor of arc time constant (s)
- α: exponential term of time constant.
- β: exponential term of cooling power

Assumptions:

- temperature of arc varies exponentially with time.
- cross-sectional area of arc is constant.
- power loss in the arc column is constant.
- arc time constant and cooling power are exponential functions of conductance.

The assumption that the arc time constant and cooling power are exponential functions of conductance is what makes this model easily match experimental results. There is no physical justification for this relationship, however, it is purely mathematically convenient. The Schwarz model

is used in the upcoming simulation for its relative simplicity and accuracy in modeling arcing phenomena.

Varying the parameters of the Schwarz model will change certain behaviors of the arc. For instance, τ_0 and α control the initiation time and delay of the established arc. P_0 and β are similar to u_0 in the Cassie model in that they control the peak value of the arc voltage. By increasing P_0 or β, it is easier to quench the arc. τ_0 is akin to the insulation level of the interrupter, and P_0 is analogous to the maximum current breaking capacity [18] [19].

In the simulation, the parameters for an arbitrary VI were derived via parameter sweep method. The parameters used in the simulation were such that it modeled a VI that created a stable arc upon separation and was quenched at a forced current zero.

E. Surge Arrester-IEEE Model

It is difficult to appropriately size a metal oxide varistor (MOV) device in order to safely dissipate the required energy during faults at 20 kVdc. Doing so would require layering many devices in both series and parallel. Surge arresters, however, are more suited to dissipating high amounts of energy safely at the expense of a lower safety margin (e.g. higher clamping voltages). Both are made of metal-oxide disks. In the upcoming simulation, a surge arrester is utilized in the energy dissipation branch to clamp overvoltages seen at current interruption.

These devices are utilized to protect systems from transient overvoltages, such as those during switching surges or lightning strikes, and protect any vital or sensitive equipment. By suppressing an overvoltage, a SA will also prevent the restriking of any arcs across open mechanical contacts immediately after fault interruption. The general current-voltage (IV) curve of an SA is provided in Fig. 4. Below its knee voltage, the SA appears as an open circuit as it conducts a very small, negligible leakage current. As voltage increases, the arrester's impedance decreases, and it conducts significant current. This highly nonlinear region is responsible for its clamping and dissipative behavior. For very high voltages, the SA appears as a low-valued resistance of a few ohms.

Various models can be used to imitate the voltage clamping and energy dissipating characteristics of the SA. These models can be split into two types: frequency dependent and frequency independent. An important characteristic in these devices is the fact that the current lags the voltage, resulting in higher peak voltages the more drastic the lag. With very fast transient overvoltages (a few μs), this frequency dependence is crucial to model since these fast transients have non-negligible current lags affecting peak voltage. This frequency dependence can be neglected with slower overvoltages such as switching surges where the current lag is not as significant to the overall waveform. Therefore, frequency independent models can be used for slower transients (several tens of μs and above). Frequency independent models include the ideal model, Fig. 5(a), and the IV model, Fig. 5(b). The IV model is most suited to modeling the behavior of an MOV with parasitic impedances and requires IV curve samples [20] [21]–[22]. The ideal model is composed of anti-series Zener diodes that are reverse biased to the clamping voltage of the device. It is the simplest model and has benefits in ease of implementation and non-resource intensive in simulations, but it is a drastic simplification that approximates only the ideal clamping behavior. Frequency dependent models include the IEEE

model [23] or any of its derivatives [24]. In the upcoming simulation, the IEEE model was utilized for its accuracy, ease of implementation, and tuning.

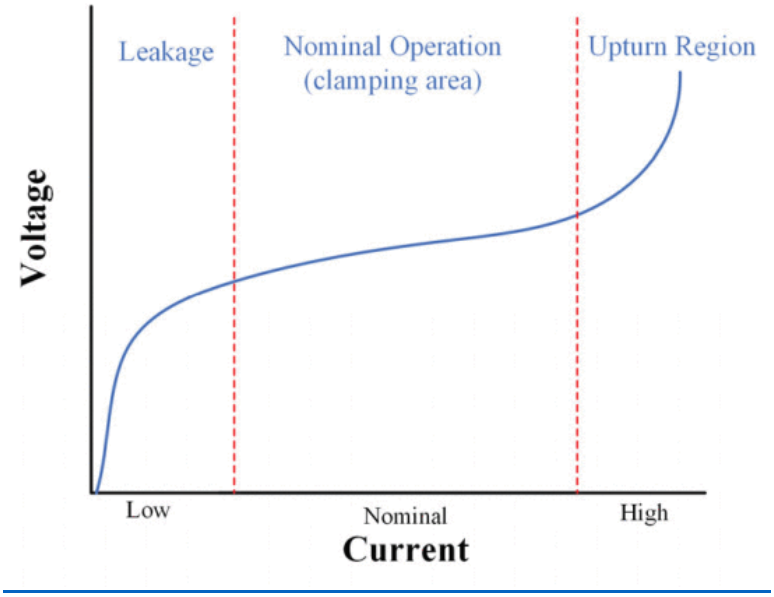

Fig. 4. Generalized MOV and SA current-voltage curve regions.

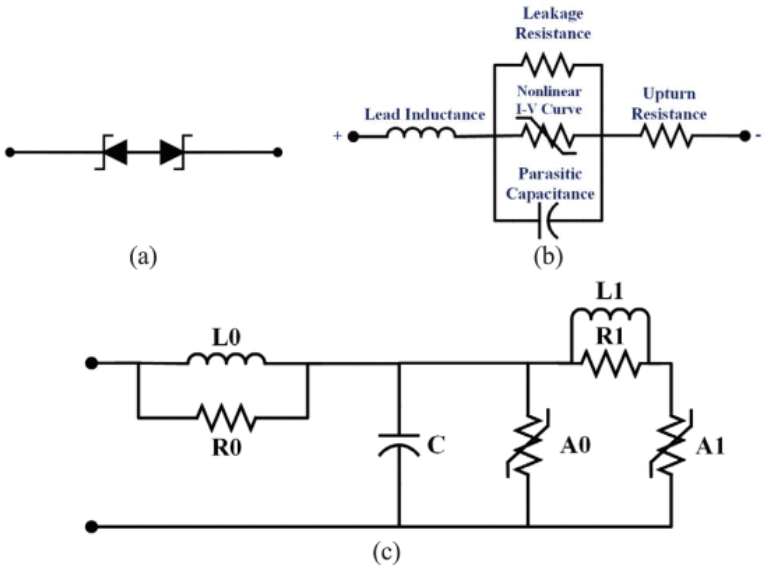

Fig. 5. MOV and SA models (a) Zener diode approximation, (b) IV model, (c) IEEE model.

The IEEE model, provided in Fig. 5(c), accomplishes its frequency dependence through RL filters. The voltage clamping characteristics are accomplished by the nonlinear resistors A0 and Al. The RL filters are low-impedance for slow transients, so A0 and A1 are essentially in parallel. For fast transients, the L1 and R1 filter is high-impedance and the surge flows through A0 only. A0 has higher voltage characteristics than Al, which results in higher peak voltages for fast transients.

In normal operation of the CB, the SA acts like a near-open circuit conducting negligible leakage current. Once the knee voltage of the arrester is surpassed during fault interruption, the arrester starts to conduct significant current. Meanwhile, the arrester dissipates all residual system energies and

clamps the overvoltage across the breaker. In doing so, the arrester will dissipate the line current to zero for post-fault isolation.

In the simulation, an ABB POLIM-H (4. 7kV MCOV) [25] surge arrester is modeled. The IEEE model is tuned such that it replicates the rated peak voltage during an 8/20 waveform at 20 kA. Considering the rated MCOV, five arresters are required in series. This results in peak overvoltage clamping at approximately 3.1 pu dc bus voltage.

SECTION IV. Simulation Model

The proposed breaker is to be installed on a20 kV dc bus of an electric shipboard power system, as shown in Fig. 6. Here, the CB protects the dc bus from any faults and is between the AC/DC rectifier and any shipboard loads (i.e. radar, railgun, etc.). This environment was modeled in PLECS, and its high level circuit schematic of the test circuit is shown in Fig. 7. The dc bus is modeled as an ideal voltage source with line resistance and inductance. The line resistance represents the ohmic losses of the bus. The line inductance represents the overall bus inductance. This is the main contributor to the post-fault dissipation waveforms for the SA. When a fault occurs, it is limited in magnitude by the line resistance and in rise time by the inductance. The value for line resistance is set such that it limits the peak magnitude of the fault current. Note that this limitation in magnitude could also be done with a sufficient current choke, i.e. varying the line inductance. This approach is favorable in a physical application since it decreases the power loss of the dc bus. However, since the focus of this study is on the successful interruption of a chosen magnitude of fault current, limitation via varied resistance is sufficient. The shipboard load is a 3-phase voltage source inverter which has a nominal current of 600 A. The topology for the simulated breaker is given and labeled in Fig. 2. Two RCS modules were utilized in the commutation branch and five in-series surge arresters in the energy dissipation branch.

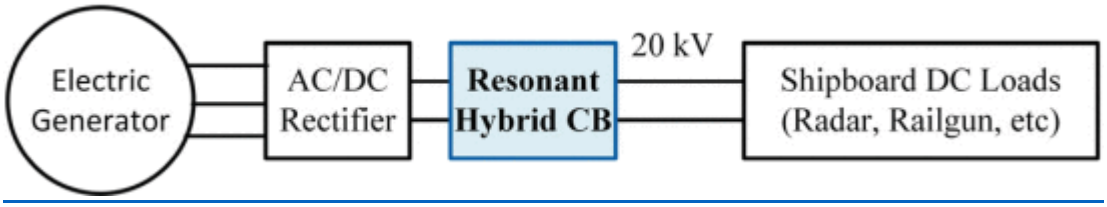

Fig. 6. The proposed CB protecting a 20kV dc shipboard power system.

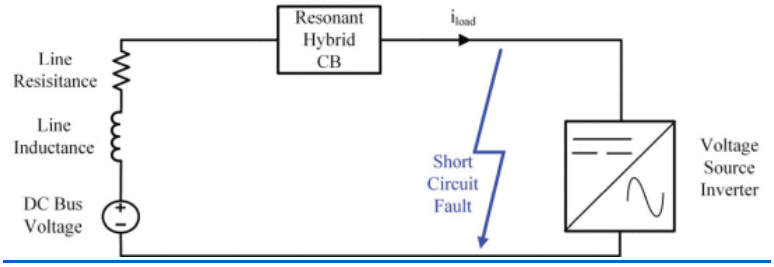

Fig. 7. High level circuit schematic of simulation model.

The overall response time of the proposed circuit breaker is limited by how fast the VI can open. This is because the oscillation and ramping of the RCS is much faster than the opening speed of the mechanical contacts. Utilizing a combination of Thomson coils and permanent magnets, the fast-actuator will open the VI in sub-500 µs. Once a fault occurs, the RCS will coordinate the peak of its

current magnitude, which occurs on a preset reversal, with the fully open point of the VI. This is the point where the dielectric recovery of the interrupter is greatest. Since the opening time of the VI is so much longer compared to the oscillation speed of the RCS, many reversals may be utilized to meet the magnitude of the fault. Using parameters listed in Tables II and IV, the RCS can realistically perform a maximum of 100 reversals during the window that the VI is opening. This is disregarding any saturation of the RCS current which would limit the achievable reversal count further.

In the simulation, the dc-bus voltage is 20 kV, the line inductance is 111 µH, the peak fault current is 19 kA, and the fault initiation time is 10 ms. The parameters of other key components and models are listed in Tables I, II, and III.

TABLE I RCS Parameters

RCS Parameters			
Source Capacitance, Cs	6.0 mF	Equivalent Capacitance	1.00 µF
Cs Initial Voltage	540.0 V	Resonant Frequency	100 kHz
Equivalent Inductance	2.53 µH	Number of Reversals	15

TABLE II SA Parameters

IEEE Model Parameters	
L1	0.28 µH
R1	13.65 Ω
L0	0.042 µH
R0	21 Ω
C	476.19 pF

TABLE III VI & Schwarz Arc Model

VI & Schwarz Arc Model	
Opening Time	500 µs
τ_0	20 ns
α	0.2
P_0	260 kW
β	0.5

SECTION V. Simulation Results

The proposed breaker has been simulated in the PLECS software environment using the test simulation circuit and key models described in previous sections. The results of the simulation are provided in Fig. 8 and 9. Note that the SiC devices referred to as S_{a1}, S_{a2}, D_{a1}, and D_{a2} are labelled in Fig. 2. Since there are multiple parallel half-bridge devices in each leg of the H-bridge, only the top and bottom devices of one parallel path are chosen. This is because all other devices' waveforms are either identical or inverted.

1. *Normal operation mode* (*0-10ms*): steady state nominal load current flows through the vacuum interrupter. Since the interrupter has low contact resistance, here it is set to 1 μΩ, the losses at this stage are negligible and leads to high efficiency. The RCS waits for a fault to occur. The SA appears as a high impedance and only conducts micro-Amps of current.
2. *Fault operation mode* (*10-10.5ms*): A fault occurs, which triggers the VI to commence opening. An arc is formed, and it stabilizes to a low voltage arc with 0.08 Ω resistance. The fault current continues to conduct through this arc and it is only limited by the line inductance, line resistance, and arc resistance. The RCS coordinates the peak of its current, being preset on the 15th reversal, with the fully open point of the VI, 500 μs after the fault. RCS oscillation starts at 10.428 ms where changes in arc resistance can be seen in Fig. 9. The RCS is excited by alternating dc voltages as shown in Fig. 8(c). During oscillation, the SiC FETs reach a peak junction temperature of approximately 80°C shown in Fig. 8(d).
3. *Arc extinguishment* (*10.5ms*): once the magnitude of the RCS current is equivalent or slightly exceeds that of the fault current, a zero crossing is achieved in the VI current. This drastically increases the resistance of the arc, changing from 0.08 Ω to 250 M Ω, and quenches it; here the fault is interrupted within 500 μs. With the VI now an open circuit, the fault current can now commutate into the RCS briefly, recharging it through the antiparallel diodes. This causes the diodes' junction temperature to increase. Ultimately, the current will commutate into the SA. The voltage across the breaker increases as the current interruption induces an overvoltage across the breaker.
4. *SA absorbs the residual energy and the fault is isolated* (*10.5-10.56ms*): Once the overvoltage crosses the knee point of the SA, it switches to low impedance and conducts significant current. Here, the surge current somewhat resembles an 8/20 waveform with a ripple imposed by the dissipation of energy in the RCS resonant components. The frequency dependence of the SA can be seen from the current lag of the surge behind the CB voltage. The peak voltage across the breaker is approximately the rated 8/20 at 20kA voltage from the POLIMH datasheet increased by a factor of five, which is the number of arresters in series in the absorption branch. Once all the energy is dissipated, the SA resumes near-open circuit high impedance with leakage current. The voltage across the breaker will level out to the nominal dc bus voltage. At this point the fault is considered fully isolated.

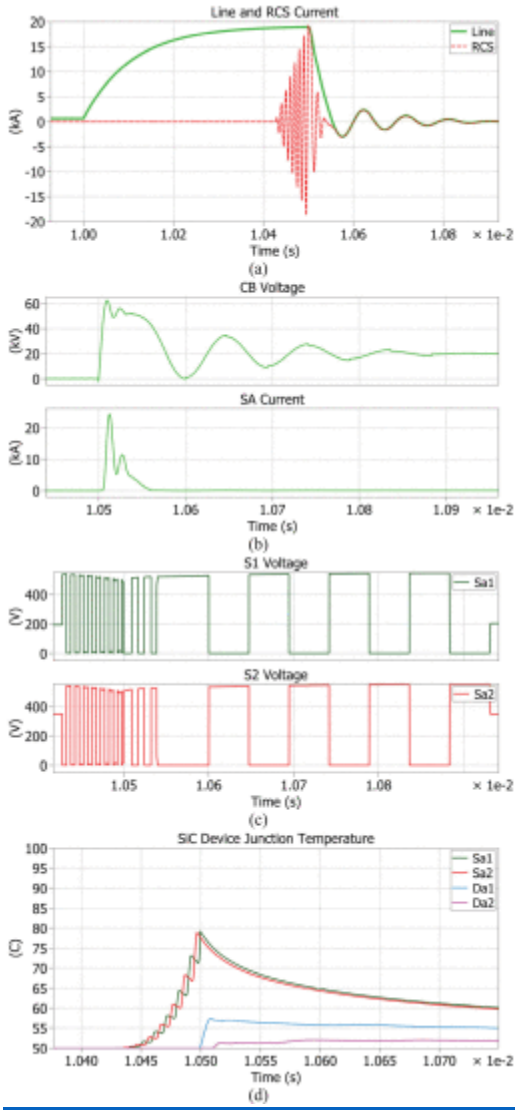

Fig. 8. Simulation results of the proposed breaker (a) line and RCS current, (b) breaker voltage and current through SA, (c) alternating voltage across SiC switches, and (d)junction temperature of the RCS SiC switches.

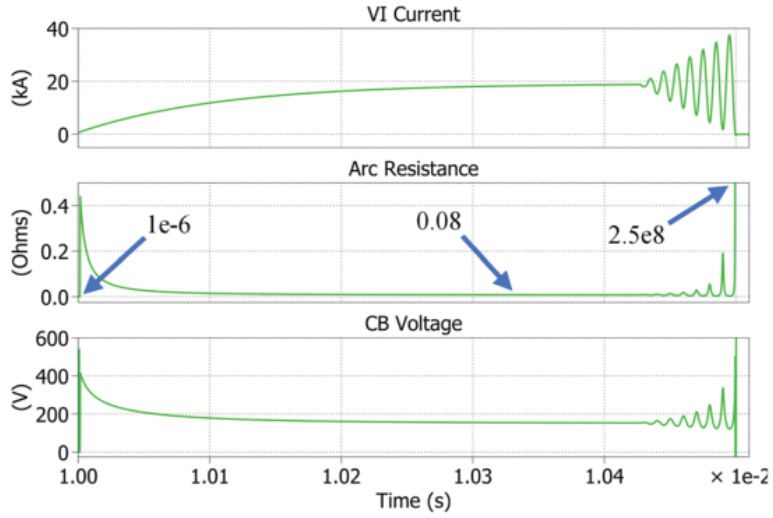

Fig. 9. Simulation results of the arcing behavior of the VI during fault operation.

SECTION VI. Conclusion

A novel 20 kV MVDC ultra-fast resonant hybrid circuit breaker was modeled and simulated in the PLECS software environment. A Schwarz model and IEEE model were utilized to provide high fidelity results of the vacuum interrupter and surge arrester respectively. SiC power modules were utilized to achieve high resonant frequencies in the resonant current source module. The junction temperature of the SiC devices were provided to verify the secure operation. Fault interruption was achieved in 500µs during a pole-to-pole fault simulation. The proposed dc breaker concept is modular and scalable, and is very suitable for MVDC applications.

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