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Abstract:

The concept of More Electric Aircraft (MEA) has gained a lot of attention from researchers recently. For such an application, two of the pivotal requirements are having a power dense and energy efficient propulsion system. To that end, in the design procedure of the electric motor and its drive system, high power density and efficiency over the entire operating range is the ultimate goal. Thus, the integration of the electric motor and drive system into a single unit has been introduced as an effective method to meet the design objectives. Therefore, this paper presents the design procedure of a module of an Integrated Modular Motor Drive (IMMD). Electrothermal design of the GaN single phase full bridge inverter module has been conducted and the results are discussed. The analysis includes the thermal investigation of the WBG semiconductors by sweeping the number of parallel devices in each switch position at different switching frequencies. Furthermore, a single drive PCB module is designed and evaluated in ANSYS Q3D for parasitic extraction. Finally, double pulse test (DPT) is performed to verify the optimal design of PCB busbar.

SECTION I. Introduction

In the recent decade, the electrification of aerial transportation has garnered the attention of researchers towards a more robust, fault tolerant and power dense design of electric motors and drive systems. In the More Electric Aircraft (MEA) application, the volume and weight of the motor-drive system are crucial parameters that ultimately affect the flight time. In other words, enhanced power density plays an elemental role in the feasibility of MEA concept [1]. To that end, Integrated Modular Motor Drive (IMMD) in which the motor and drive system are integrated as a single structure [2]–[4], is being studied extensively. The emergence of the Wide Band Gap (WBG) devices with their unique properties, such as the ability to function at higher junction temperature, low on state resistance, and high efficiency [5], increases the practicality of IMMDs. Utilizing WBG devices would decrease the passive element size [6] and brings the ability for the Power Electronic (PE) interface to operate at a higher ambient temperature. This, in turn, would relax the cooling requirements of PEs, reduce the aerial load factor, and will result in a more cost effective flight solution.

The integration of motor and the drive system brings some technical challenges, including proper functioning of power electronic devices under harsh thermal conditions, vibrations, and electromagnetic fields [7], [8]. For instance, thermal characteristics of semiconductors and their performance under high ambient temperature play important role in the successful implementation of the IMMD concept [9]. In that regard, utilizing WBG devices and specifically GaN switches could be a good solution considering their high junction temperature capabilities and low on state resistance. In addition, high current ratings of IMMD makes PCB design problem even more complex. In other words, an optimally designed PCB should be able to perform as a low stray inductance busbar with high current handling capability. Cooling system design is another challenging aspect of IMMDs which is out of the scope of this article.

In this paper, the electrothermal design of a GaN-based Axially Stator iron-Mounted (ASM) IMMD is presented. The presented IMMD is depicted in Fig. 1a, which includes 18 individual inverter modules that drive 18 coils of a three phase Surface Mounted Permanent Magnet (SPM) machine (6 coils per phase). The electrothermal design is comprised of factors such as optimal component selection, PCB design, parasitic and current density evaluation, and thermal assessment of the H-bridge module. Design considerations for each of these factors will be considered in the subsequent sections. In Section II, the design of a single phase full bridge converter, including switch selection and configuration, is presented. In Section III, the PCB design considerations are discussed and the designed PCB is evaluated through ANSYS Q3D parasitic extraction software. Finally, the extracted parasitic inductances are used in LTSPICE simulation software to detect the expected over and undershoots on the device voltages via a Double Pulse Test (DPT).

TABLE I: Nominal System Parameters

Parameters	Value	Parameters	Value
V_{dc}	1 kV	f_{rated}	1250 Hz
I_{coil}	268.12 Arms	PF	0.8
P_{rated}	250 kW	$\lambda_{\mathrm{pm,max}}$	60.6 mWb
R_{s}	46 Ω	η	$\geq$ 98%
L_{s}	137 µH	$T_{\mathrm{j,max}}$	125° C/W

TABLE II: Candidate Semiconductors Specifications

Parameters	EPC2034C	IRF678MTRPbF
Voltage (V)	200	200
Current (A)	48	19
$R_{\mathrm{ds,on}}$ (mΩ)	8	100
C_{oss} (pF)	641	69
FOM	0.0107	0.0086

SECTION II. GaN Single Phase Full Bridge Inverter Module Design

The three phase IMMD is illustrated in Fig. 1a in which it is located on the stator of a Surface Mounted Permanent Magnet machine (SMPM). Each phase is comprised of 6 coils, and each coil is driven by a GaN based single phase full bridge converter, leading to 18 individual drive modules in total. An individual drive module along with a motor segment and their cooling system are depicted in Fig. 1b. Each drive module includes a stack up of three PCBs: 1) GaN full bridge board (Bottom); 2) DC link capacitor board (Mid); 3) Communication board (Top). The heat sink is Incorporated in the cooling jacket that lies between the motor coils and the drive module. The GaN full bridge board is mounted on top of the heat sink and is connected to the coil terminals. The complete topology of the drive system is shown in Fig. 1c. The six GaN full bridge converters for each phase are connected in series, and thus, they all carry the same current (motor's phase current). The phase back emf will be the summation of individual coil emf.

Based on the symmetry and modularity of the design concept, the design of one individual drive module is studied in this paper. Regarding the high power and ratings of the system, the first step is to select the semiconductors that matches the requirements. Also the thermal performance of the selected semiconductor should be evaluated for the cooling system design purposes. Both of these procedures are explained in detail in the following subsections.

A. Switch Selection

The specifications of the SMPM motor are listed in Table I. A variety of WBG devices are available that match the specifications listed in the aforementioned table. In order to select between viable candidates, it is necessary to introduce a Figure Of Merit (FOM) that projects the properties of the device which are crucial to its performance. The FOM can help to choose the semiconductor which matches the desired requirements the best.

Considering the desired voltage and current ratings, and efficiency, the ultimate goal is to choose a switch with the lowest possible losses. In other words, the semiconductor with lower conduction and switching losses would be the optimal choice. In [10], Anderson *et al.* specified that a semiconductor's losses are influenced by $R_{\mathrm{ds,on}}$ and C_{oss}, where $R_{\mathrm{ds,on}}$ is the on-state drain to source resistance and

In this study, the same FOM is utilized to choose a viable candidate switch. The higher the FOM, the better the switch meets the desired specifications. Based on this study, two candidates were selected as specified in Table II. Since EPC2034C exhibits better FOM compared to its counterpart this device was selected for further evaluation [11].

B. Paralleling Switching Devices

Based on the coil current requirements of individual drive module as listed in Table I, and EPC2034C current ratings, it is evident that multiple EPC2034C switches are required in parallel to meet the current rating for every switch position. To that end, a single phase full bridge inverter is simulated in PLECS software. In Fig. 2 thermal equivalent circuit model of semiconductor heat dissipation is presented. In the equivalent circuit, P_{Loss} represents the summation of switching and conduction losses of a GaN semiconductor as it is shown in (2). The factor $R_{\theta,\mathrm{jc}}$ is the junction-case thermal resistance, $R_{\theta,\mathrm{cs}}$ is the thermal resistance of the Thermal Interface Material (TIM), and $R_{\theta,\mathrm{sa}}$ is the heatsink-ambient thermal resistance. Also, T_{j}, T_{c}, T_{s}, and T_{a} are the junction, case, heatsink, and ambient temperature, respectively.

The thermal model of EPC2034C (that is generated based on the provided data by the manufacturer) is used in the simulation in order to assess the performance of the active switches. Three parameters of interest swept in the simulation include: Switching frequency (f_{sw}), number of parallel devices (N_{par}), and heatsink-ambient thermal resistance ($R_{\theta,\mathrm{sa}}$). Simulation results are presented in Fig. 3, in which Fig. 3a represents the effect of swept parameters on the efficiency of the inverter, while, Fig. 3b exhibits the effect on the device's junction temperature. The 2D red plane shown in Fig. 3a shows the cut off boundary in terms of desired efficiency while the red plane shown in Fig. 3b exhibits the cut off boundary in terms of device absolute junction temperature. Any $N_{\mathrm{par}} - f_{\mathrm{sw}}$ combination resulting in an efficiency lower or a junction temperature higher than either cut off limits is automatically discarded.

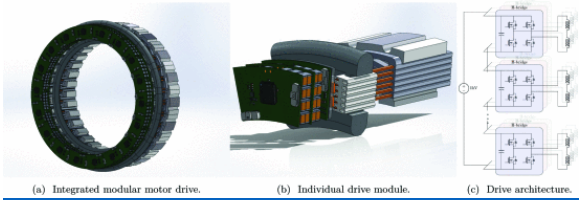


Fig. 1: Integrated Modulated Motor Drive. 1a) Axially stator iron-mounted fully integrated modular motor drive. 1b) One single inverter module ($\frac{1}{18}$th of the whole drive system) including, motor coil and cooling system, GaN full bridge inverter board, DC link capacitor bank, and control board. 1c) Complete drive system architecture.

Owing to the device physics, for GaN semiconductors, switching loss has a minor contribution towards the overall losses in the switch [12]. Thus, conduction loss could be considered as the main contributor, where the effect of conducted current by the switch is quadratic as is shown below:

$$P_{\mathrm{Loss}} = P_{\mathrm{swt}} + P_{\mathrm{cond}}$$
$$P_{\mathrm{cond}} = R_{\mathrm{ds,on}} I_{\mathrm{rms}}^2$$

(2)(3)

where P_{swt} is the switching loss, P_{cond} is the conduction loss, $R_{\mathrm{ds,on}}$ is the GaN switch on state resistance and I_{rms} is the rms value of the conducted current by the switch. As an expected outcome, by increasing the number of parallel devices the efficiency increases which is verified by Fig. 3a.

Thermal resistance of heatsink-ambient ($R_{\theta,\mathrm{sa}}$) represents the cooling requirements of the PE system. For instance, a low $R_{\theta,\mathrm{sa}}$ translates to a more aggressive cooling system and vice versa. In Fig. 3b, device junction temperature is depicted along the *z*-axis with f_{sw} and N_{par} on the *x* and *y*-axis respectively. The ascending planes on the graph represent different temperature profiles obtained for five different $R_{\theta,\mathrm{sa}}$ values through f_{sw}-N_{par} combinations. The the top most plane is obtained through the highest $R_{\theta,\mathrm{sa}}$ value and vice versa. As it can be seen in Fig. 3b, by increasing the heatsink-ambient thermal resistance (relaxing cooling constraints), device's junction temperature is increased.

C. Final Design

In order to find a solution for the design problem, first, the input variables need to be narrowed down. In this study, among the three input variables (N_{par}, f_{sw}, $R_{\theta,\mathrm{sa}}$), the first two are determined based on electrical constraints. Since this is a drive application, 20 kHz is chosen as the switching frequency to avoid further concerns regarding insulation degradation [1]. It is worth mentioning that, lower switching frequencies will increase the current ripple which is not desirable. Using the presented data in Fig. 3, number of parallel devices in a switching position are chosen to be 8. The total power loss per device (i.e., summation of conduction loss and switching loss) in steady state against the swept $R_{\theta,\mathrm{sa}}$ are shown in Fig. 4. Inspection of the losses confirms that conduction loss is the major contributor to the overall semiconductor losses in the chosen GaN device. The average device junction temperature and the drive efficiency against the swept $R_{\theta,\mathrm{sa}}$ are shown in Fig. 5.

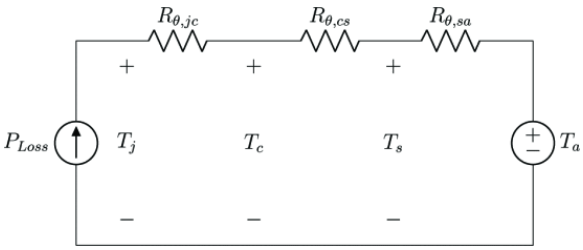
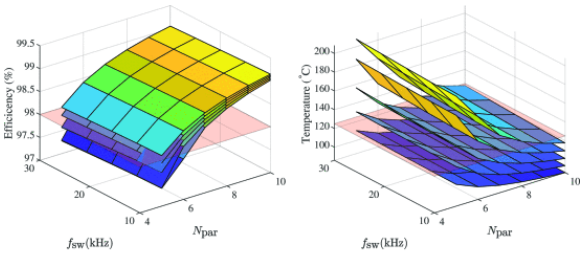


Fig. 2: Thermal equivalent circuit of GaN semiconductor to ambient.

The results presented in Fig. 4 and 5 reveal that with 8 parallel devices in each switch position (N_{par} = 8) and with f_{sw} of 20 kHz, for any R_{sa} smaller than 0.2°*C/W* both efficiency and maximum junction temperature constraints are well satisfied.

SECTION III. PCB Design

A picture of the GaN based single-phase full bridge is shown in Fig. 6. The PCB is composed of individual half-bridges on each side that are physically symmetric with respect to each other. The layer stack up is made up of 16 layers, with 2 oz of copper per layer. The dimensions are 2.92 x 2.26 x 0.08 in (LxWxH), leading to a peak power density of 26.13 kW/in^3.



(a) Efficiency analysis. (b) Temperature analysis.

Fig. 3: Thermal performance study results for single phase GaN full bridge inverter. 3a) Efficiency vs. N_{par} and f_{sw} ($R_{\mathrm{ds,on}}$ increases from top plane to bottom plane). 3b) Device junction temperature vs. N_{par} and f_{sw} ($R_{\mathrm{ds,on}}$ decreases from top plane to bottom plane).

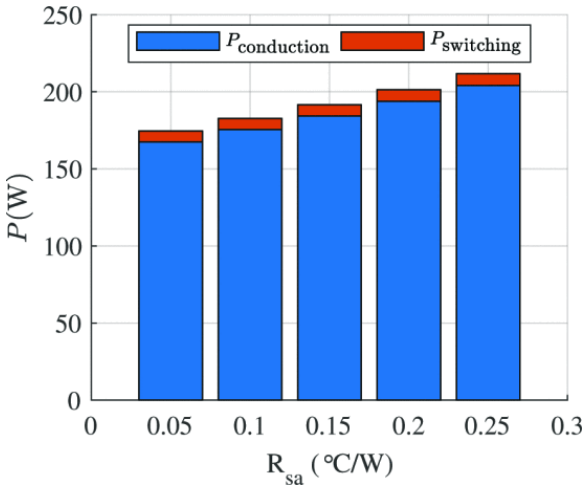


Fig. 4: GaN devices conduction and switching losses for N_{par} = 8 & f_{sw} = 20kHz.

Fig. 6a shows the top side view of the GaN board in which various components can be identified. Active GaN switches (EPC2034C) can be seen as discrete components in blue, the gate driver circuitry utilizing the TI 200V LMG1210 gate driver is shown in the yellow box, and a non-invasive hall effect based current sensor (ACS37612) used for phase current measurement is enclosed in the solid green box. A primary design objective is to minimize the voltage overshoots during the switch commutation process. Three main contributors that dictate the voltage overshoots are: 1) Power loop inductance, 2) Gate loop inductance, and 3) Common source inductance. The chip-scale package of the eGaN FETs eliminates any inductance within the package leaving the aforementioned parameters as the main contributors. Power loop inductance is dictated by the position of High Frequency (HF) decoupling capacitors, GaN power pole, and the mutual inductance that is formed between the go and return path of the HF currents. To minimize the power loop inductance, the HF decoupling capacitors are placed close to the drain of the High Side (HS) FET. The Low Side (LS) FET is placed beside the high side FET, thus, forming a power pole. PCB vias connect the ground of HF capacitors to the low side source through the first inner layer, where the dielectric thickness is kept thin to increase the cancellation effects of mutual inductance [13]. Following these optimal layout guidelines, in Fig. 6a, the high side FETs are shown with a shaded red box, the low side FETs are shown with the green box, while, the decoupling capacitors are shown in the shaded magenta box. Gate loop inductance is determined by the position of gate driver with respect to the power poles, and the mutual inductance between the go and return path of the gate drive currents. To minimize the gate loop inductance, the gate driver must be placed as close as possible to the gate and source terminal of each transistor that it drives. Finally, the common source inductance can be minimized by orienting the decoupling/bootstrap capacitors, as well as the gate drive resistances in a way that the gate current direction is always orthogonal to the direction of main power loop current. Fig. 6b shows the zoomed in view of the GaN PCB, in which, the direction of the gate loop currents are shown in blue, and power loop currents are shown in black. Solid lines indicate that the gate drive/power loop currents are flowing in a particular layer, while, the dashed lines indicate that these loop currents flow through the vias, and return through layers placed adjacent to the primary current flow layer.

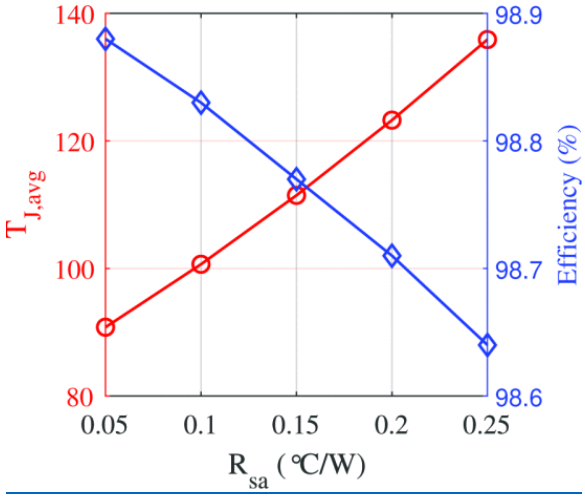


Fig. 5: Devices junction temperature and GaN full bridge efficiency for N_{par} = 8 & f_{sw} = 20kHz.

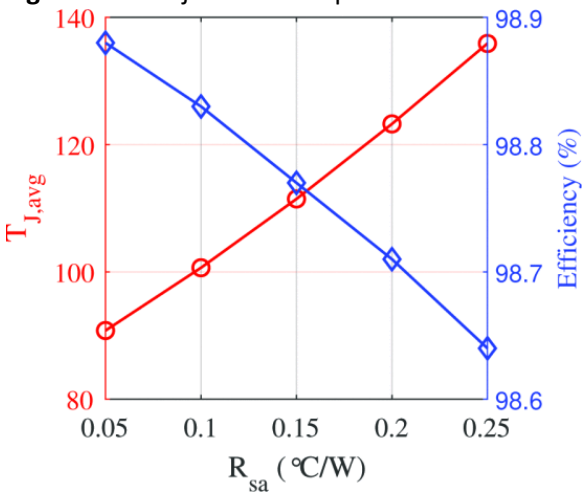


Fig. 6: Rendering of the 16-layer optimized GaN PCB: a) High side GaNs are shown in shaded red; Low side GaNs are shown in shaded green; The decoupling capacitors are shown in shaded magenta; Current sensor is shown in green box while the associated gate drive circuitry is shown in the yellow box; b) Zoomed in view of the power poles: The gate drive loop is shown in blue while the power loop is shown in black.

The HF commutation loop and parasitic inductances for a half bridge is shown in Fig. 8. The commutation loop contains 2 GaN switches (shown in green color), HF dc-link capacitors, and 3 interconnecting busbars components. The total loop inductance of the HF loop is evaluated using theory of partial inductances. Each component in the loop is characterized by its Self Partial Inductance (SPI) and a Mutual Partial Inductance (MPI), e.g., the SPI of interconnecting busbar between the HF capacitor and drain of the HS FET is represented by L_{P}, while the MPI between busbar component L_{P} and L_{N} is represented by $M_{\mathrm{P-N}}$. The HF capacitors and GaN switches are not modeled in this study. For sake of convenience, their SPI's are assumed to be 0.1 nH each.

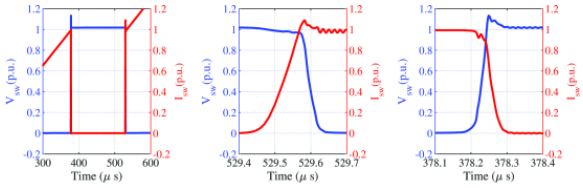
The parasitic inductances of the busbar components are extracted using ANSYS Q3D FEM software. The simulation is setup (via 1A current injection) by assigning sources and sinks in the busbar geometry to mirror the HF current flow according to the commutation loop. The overall loop inductances is given by,

$$L_{\mathrm{Loop}} = L_{\mathrm{BB}} + L_{\mathrm{C}} + 2L_{\mathrm{SS}} \tag{4}$$

where L_{BB} is the parasitic inductance of the busbar to be estimated by Q3D software and includes the effect of all SPI's and MPI's of the busbar, excluding the dc-link caps and power switches. The inductance estimation is carried out at a particular frequency called the evaluation frequency ($f_{\mathrm{eval}} = 1/2\pi t_{\mathrm{f}}$), where t_{f} is the fall time of the GaN switch. The fall time for the FET under consideration (EPC2034C) is calculated to be 10 ns, thus, giving f_{eval} = 15.9 MHz [12]. At f_{eval} , the parasitic inductance of the busbar is evaluated to be L_{BB} = 0.39 nH, thus, giving a total loop inductance of L_{Loop} = 0.7 nH.

SECTION IV. Simulation Test Results

Once the extraction of parasitic inductance is accomplished, simulations are conducted in LTSPICE simulation environment to model the voltage overshoot on the active switches during the switch commutation process. The simulation were conducted using accurate eGaN model from the manufacturer, while, the high frequency decoupling capacitor's inductance was modeled using assumption made in Section III with a turn-on and turn-off gate resistance of 4.7 Ω. The simulation results for a double pulse test conducted at rated condition as specified in Table. I are shown in Fig. 7. Figure 7a shows the current flowing through test inductor (L_{DPT} = 100 μH) in red, while, the switch voltage of the bottom eGaN is shown in blue on the y-axis. Figure 7b and Fig. 7c show the zoomed in view of switch turn-on and turn-off transients. It can be seen that during the turn-on process there is very minimal undershoot on the switch voltage while during the turn-off process the switch voltage is limited to 13% above the rated voltage. This corresponds to a voltage overshoot of 21V for a rated module DC-bus voltage of 166V. The presented results verify the optimal design of the PCB busbar by limiting the overshoot to within 15% band during rated test conditions.



(a) Simulation results of double pulse test. (b) Switch turn-on transient. (c) Switch turn-off transient.

Fig. 7: Double pulse test results at rated test conditions.

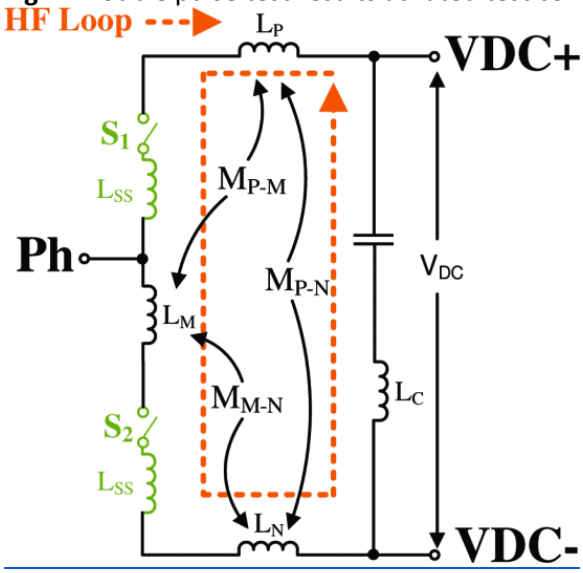


Fig. 8: High frequency current commutation loop in a half-bridge.

SECTION V. Conclusion

This paper presents a design procedure of a single module for an IMMD system intended to be used in an MEA application. The topology of the drive system is modular, based on using six single phase full bridge GaN converters (modules) connected in series (for each phase) to fulfill the DC-link requirements. The design procedure begins by selecting the optimal active switch based on a figure-of-merit (FOM) that incorporates the device output capacitance and on-state resistance. Next, the optimal number of switches to be connected in parallel are determined to meet the phase current requirements. The analysis is conducted by sweeping the number of devices to be connected in parallel against switching frequency (f_{sw}) to determine the efficiency and expected junction temperature rise of the devices. In the next section, a PCB is designed taking into account design considerations to maximize the mutual partial inductances among various components in the high frequency power loop. The analysis to detect self and mutual partial inductances is conducted in ANSYS Q3D environment. Systematic placement of the high frequency decoupling capacitors, GaN power pole and the gate driver ensures minimum interaction between the gate drive loop and the main power loop. The result of Q3D analysis shows a busbar parasitic inductance of L_{BB} = 0:39 nH which is within the suggested range by the manufacturer. Finally, the extracted parasitic inductance are used in LTSPICE simulation software to detect the voltage over/undershoots on the GaN switches. In the future, the PCB busbar will be tested experimentally at rated test conditions to verify the simulated results.

References

1. S. Yin, K. J. Tseng, R. Simanjorang, Y. Liu and J. Pou, "A 50-kw high-frequency and high-efficiency sic voltage source inverter for more electric aircraft", *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9124-9134, 2017.

2. W. Lee, S. Li, D. Han, B. Sarlioglu, T. A. Minav and M. Pietola, "A review of integrated motor drive and wide-bandgap power electronics for high-performance electro-hydrostatic actuators", *IEEE Transactions on Transportation Electrification*, vol. 4, no. 3, pp. 684-693, 2018.

3. H. Zeng, J. Swanke, T. M. Jahns and B. Sarlioglu, "Modular modeling and distributed control of permanent-magnet modular motor drives (mmds) for electric aircraft propulsion", *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 4598-4605, 2021.

4. A. H. Mohamed, H. Vansompel and P. Sergeant, "An integrated modular motor drive with shared cooling for axial flux motor drives", *IEEE Transactions on Industrial Electronics*, vol. 68, no. 11, pp. 10 467-10 476, 2021.

5. A. H. Mohamed, H. Vansompel and P. Sergeant, "Electrothermal design of a discrete gan-based converter for integrated modular motor drives", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 5, pp. 5390-5406, 2021.

6. R. A. Torres, H. Dai, T. M. Jahns, B. Sarlioglu and W. Lee, "Thermal analysis of housing-cooled integrated motor drives", *2021 IEEE Transportation Electrification Conference Expo (ITEC)*, pp. 1-6, 2021.

7. J. Wang, Y. Li and Y. Han, "Integrated modular motor drive design with ¡roman¿ganj/roman¿ power ¡roman¿fetsj/roman¿", *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3198-3207, 2015.

8. L. Verkroost, J. Van Damme, D. V. Bozalakov, F. De Belie, P. Sergeant and H. Vansompel, "Simultaneous dc-link and stator current ripple reduction with interleaved carriers in multiphase controlled integrated modular motor drives", *IEEE Transactions on Industrial Electronics*, vol. 68, no. 7, pp. 5616-5625, 2021.

9. R. A. Torres, H. Dai, T. M. Jahns, B. Sarlioglu and W. Lee, "Cooling design of integrated motor drives using analytical thermal model finite element analysis and computational fluid dynamics", *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1509-1509, 2021.

10. J. Azurza Anderson, G. Zulauf, J. W. Kolar and G. Deboy, "New figure-of-merit combining semiconductor and multi-level converter properties", *IEEE Open Journal of Power Electronics*, vol. 1, pp. 322-338, 2020.

11. *Datasheet: Epc2034c*, 2020, [online] Available: https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2034datasheet.pdf.
12. A. Lidow et al., GaN Power Devices and Applications, London:Wiley, 2015.
13. "How to design an egan fet-based power stage with an optimal layout", *EPC Tech. Rep.*, 2021, [online] Available: https://epc-co.com/epc/Portals/0/epc/documents/application-notes/How2AppNote007%20-%20Design%20an%20eGaN%20FET%20Based%20Power%20Stage%20with%20an%20Optimal%20Layout.pdf.