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Active Voltage Balancing of Integrated Modular Drive with Series DC-Link Capacitors

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# Abstract:

In order to reduce the size and weight of transmission cables, high direct current (DC) bus voltage is desired for electrical machine drives used in the hybrid powertrains of more-electric aircraft (MEA). An integrated modular machine drive (IMMD) with DC-link capacitors connected in series is adopted to break down the supply voltage for each drive unit. With lower electrical stress, partial discharge (PD) risks at high altitudes can be significantly reduced. This paper deals with the challenge of active DC-link voltage balancing control in a megawatt-level integrated modular machine drives. Voltage closed-loop control is developed under the challenges of high electrical frequency and limited switching frequency. The impact of drive unit count and component parameter variations has been investigated, highlighting the design tradeoffs of the IMMD with series DC-link capacitors.

# SECTION I. Introduction

Megawatt-level lightweight and ultra-efficient electrical machine drives used in hybrid propulsion systems are critical components for decarbonized passenger commercial aircraft. Due to partial discharge (PD) at altitude/lower air pressure, the supply voltage of commercial machine drives used in aerospace applications is currently limited to ±270 Vdc / 540 Vdc [1], [2]. However, this limit results in large cable sizes when designing megawatt-level machine drives.

In order to increase the DC-link voltage to 2kV or higher while preventing insulation failure and equipment malfunction, a segmented stator and modular power electronics design can be implemented to reduce voltage stress in each drive units. One promising design approach is the integrated modular machine drive (IMMD) [3], [4]. Fig. 1 shows the cross section of a 1 MW, 20,000 r/min, 18-slot/12-pole fractional-slot concentrated winding surface permanent magnet (FSCW-SPM) machine [5]. The stator winding is grouped into 6 three-phase winding sets. Each three-phase winding set is fed by a three-phase drive unit. By connecting the DC bus terminals of the six drive units in series, each of the three-phase inverters and associated phase windings is only required to withstand 333 Vdc differential voltage (absolute voltage will be higher depending on the reference point/ground arrangement), which can significantly reduce the risk of PD and insulation failures at high altitudes.

[Fig. 1. - 
Cross section of 1 MW, 20,000 r/min 18-slot/12-pole FSCW-SPM machine with distributed power electronics [1].
](https://ieeexplore.ieee.org/mediastore_new/IEEE/content/media/9235288/9235325/9236275/wu1-p8-wu-large.gif)

**Fig. 1.** Cross section of 1 MW, 20,000 r/min 18-slot/12-pole FSCW-SPM machine with distributed power electronics [1].

[Fig. 2. - 
Dynamic terminal voltage of 6 series DC-link capacitors at full speed (20,000 r/min), full power (1 MW), without anti-windup.
](https://ieeexplore.ieee.org/mediastore_new/IEEE/content/media/9235288/9235325/9236275/wu2-p8-wu-large.gif)

**Fig. 2.** Dynamic terminal voltage of 6 series DC-link capacitors at full speed (20,000 r/min), full power (1 MW), without anti-windup.

However, even with strictly consistent design parameters for all drive units, the terminal voltage of the DC-link capacitors cannot be passively balanced. Fig. 2 shows the terminal voltage profile when the PM machine operates at 477.5 Nm, 20,000 r/min (1 MW). During the first 0.02 s, the voltages are balanced at ~333 Vdc. They gradually separate and reach unbalanced steady-state voltages after the transient state (0.02 s to 0.06 s). One of the capacitors (Cap #5) carries 718.0 Vdc while each of the remaining five capacitors has 255.8 Vdc terminal voltage. The severe voltage imbalance is due to the conflicts of dynamic current regulation between the 6 drive units. The severity of the voltage imbalance is dependent on the operating condition (speed and torque) as well as PI gains. The voltage imbalance results in a significant decrease of the output torque.

[Fig. 3. - 
Dynamic terminal voltage of 6 series DC-link capacitors at full speed (20000 r/min), full power (1 MW), with anti-windup.
](https://ieeexplore.ieee.org/mediastore_new/IEEE/content/media/9235288/9235325/9236275/wu3-p8-wu-large.gif)

**Fig. 3.** Dynamic terminal voltage of 6 series DC-link capacitors at full speed (20000 r/min), full power (1 MW), with anti-windup.

Fig. 3(a) shows that adopting the anti-windup method can mitigate the voltage imbalance when the six modules have identical parameters. This is because the integrator saturation due to imbalance can be discharged. However, typical tolerances for electrolytic and metallized polypropylene film (MPPF) capacitors are ± 10% and ± 5%, respectively. In addition, there can be further capacitance changes due to performance degradation or temperature variation during their lifetimes [6]. Fig. 3(b) shows a specific case of voltage imbalance when one of the 6 DC-link capacitors has 1% higher capacitance value than the others. Load imbalance due to machine asymmetry or module inconsistency can make the situation even worse.

Voltage balance can be achieved by adopting either large shunt resistors connected in parallel with the capacitors or active balancing circuit consisting of power switches and inductors. However, these solutions result in extra weight/volume, potential resonance, as well as extra losses in the auxiliary resistors or circuits.

Series-connected DC links are also discussed for offshore wind farm power systems, in which the voltages from multiple wind turbines with integrated generators and inverters are summed to high grid-side values [7]. In [8], a DC-link voltage balancing controller is developed for six-phase induction machines with two DC link capacitors connected in series. The drift of the DC link midpoint voltage is addressed by regulating currents in the *xy* plane to balance the power sharing of the three-phase winding sets. Active DC-link voltage balancing is also used in multilevel converters [9], [10]. [11] discusses the DC link voltage balancing control of a cascaded multilevel rectifier by tracking the DC capacitor voltage of each individual cell and biasing the power distribution among all cells.

[Fig. 4. - 
Control model with six stator winding/drive modules and six series DC-link capacitors.
](https://ieeexplore.ieee.org/mediastore_new/IEEE/content/media/9235288/9235325/9236275/wu4-p8-wu-large.gif)

**Fig. 4.** Control model with six stator winding/drive modules and six series DC-link capacitors.

The objective of this paper is to explore the active voltage balancing control algorithm for IMMDs with series DC-link capacitors, highlighting its feasibility and robustness. This paper is arranged as follows: Section II covers the development of the control model; Section III discusses the sensitivity analysis based on switching frequency, capacitance tolerances, and shunt resistors; Section IV compares designs with different number of modular drive units; Section V covers an approach extended to IPM machine drives; and conclusions are drawn in Section VI.

# SECTION II. Control Algorithm and Modeling

This section discusses the design and building of the control model. Fig. 4 shows the high-level control model used in this study. The 2kV DC power source is distributed to the 6 modules by six series-connected DC-link capacitors. Each module uses a discrete closed-current-loop field-oriented control (FOC) algorithm. The clamping anti-windup method (based on condition integration) is used to prevent integration wind-up in the PI controller. SIMULINK was used to simulate the IMMD, and the block diagram for one of the drive modules is provided in Fig. 4(b). The key parameters used in the simulation are summarized in TABLE I.

***Sizing of series capacitors***: In order to maintain low voltage ripple (Δ*V0.5t = Vbus /* (32 \* *L* \* *C* \* *f*2)) with the given machine and control parameters, a 400 μF, 600 Vdc MPPF capacitor is used in each dc link, which can theoretically limit the voltage ripple to < 1%.

**TABLE I:**Machine Drive Module Parameters Used in Simulation

|  |  |  |  |
| --- | --- | --- | --- |
| **Dimensions/Parameters** | **Value** | **Dimensions/Parameters** | **Value** |
| *d*-axis, *q*-axis inductance [μH] |  | DC link capacitance [μF] | 400 |
| PM-generated flux linkage [Wb] | 0.0645 | Phase winding resistance [Ω] | 0.0012 |
| PWM switching frequency [kHz] | 20 | Module DC bus voltage [] | 333 |
| Excitation frequency [kHz] | 2 (at 20,000 r/min) | Current command at peak power [A] | . |

[Fig. 5. - 
Active voltage balance achieved by adjusting q-axis current reference with DC-link voltage feedback.
](https://ieeexplore.ieee.org/mediastore_new/IEEE/content/media/9235288/9235325/9236275/wu5-p8-wu-large.gif)

**Fig. 5.** Active voltage balance achieved by adjusting *q*-axis current reference with DC-link voltage feedback.

***Sizing of shunt resistors***: For passive voltage balancing, a 100 kΩ, 25 W shunt resistor is connected across the terminals of each dc link capacitor. The sizing is based on the rule of thumb that the balancing shunt resistor value should be 10% of the calculated capacitor shunt DC resistance value, *RDC* = rated voltage / leakage current.

***Current sampling***: Winding current sampling is triggered when the PWM carrier waveform reaches its peak values (maximum and minimum). This means that the PWM output will be calculated/updated twice per PWM period. This helps to increase the controller bandwidth and reduce current ripple.

***Active voltage balancing***: Two of the 8 PWM vectors used in the SVPWM algorithm are shown in Figs. 5(a) and (b). Zero vectors V7(111) and V8(000) (all upper/lower switches are on/off) represent "charge only" states while the other 6 vectors are associated with both "charge" and "discharge" states. In this regard, the DC-link voltage error is used to manipulate the *q-*axis command (Fig. 5(c)) so that the time period for the zero vectors will be increased when the DC-link voltage is low. The major challenges for active voltage balancing control are: **(i)** the switching frequency (20 kHz) is relatively low compared to the maximum excitation frequency (2 kHz); and **(ii)** the winding inductance is low due to the large equivalent machine airgap.

# SECTION III. Impact of Switching Frequency, Shunt Resistor, and Capacitor Torlerances

The details of the tuning of the PI gains of the voltage loop are included in the Appendix Fig. A1 and TABLE A1. In order to minimize the voltage and current ripple while maintaining balanced DC link voltages, the PI gains of the voltage loop are set to be KaV = 3 and KbV = 0. Fig. 6 shows the module simulation results for an ideal case where all DC-link capacitor values are equal. A *q*-axis current step change from 404 A to 808 A is initiated at 0.3 s to observe the dynamic performance. Fig. 6(a) shows that the capacitor voltages are actively balanced with negligible pulsations. Due to low winding inductances, large current ripple is present in both the *d*- and *q*-axis currents (Fig. 6(b)). The *d*-axis and *q*-axis current ripple observed in Fig. 6(b) correspond to ~120 Apk phase winding current ripple at full load. With balanced DC link voltages, 477 Nm torque and 1 MW power are delivered as shown in Figs. 6(c).

[Fig. 6. - 
Terminal voltage of capacitors and current waveforms. (400μF capacitor, 100 kΩ shunt resistors, 20 kHz switching frequency, no capacitance tolerances).
](https://ieeexplore.ieee.org/mediastore_new/IEEE/content/media/9235288/9235325/9236275/wu6-p8-wu-large.gif)

**Fig. 6.** Terminal voltage of capacitors and current waveforms. (400μF capacitor, 100 kΩ shunt resistors, 20 kHz switching frequency, no capacitance tolerances).

**TABLE II:**Impact of Capacitance Tolerances for 6 Modules

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Case** | **Capacitance Tolerances Δ*C* (%)** |  |  |  |  |  | **ΔUdc (V)** |  | **Voltage Balance** |
|  | **Cap#1** | **Cap#2** | **Cap#3** | **Cap#4** | **Cap#5** | **Cap#6** | **0s~0.3s** | **0.3s~1.5s** |  |
| #1 | +1% | 0% | 0% | 0% | 0% | 0% | 0.91 (Cap #1)  0.18 (Caps #2~6) | 0.46 (Cap #1)  0.45 (Caps #2~6) | balanced |
| #2 | +5% | 0% | 0% | 0% | 0% | 0% | 1.09 (Cap #1)  0.22 (Caps #2~6) | 0.54 (Cap #1)  0.40 (Caps #2~6) | balanced |
| #3 | +5% | +5% | +5% | 0% | 0% | 0% | 0.62 (Caps #1~3)  0.62 (Caps #4~6) | 0.38 (Caps #1~3)  0.38 (Caps #4~6) | balanced |
| #4 | +1% | 0% | -1% | +1% | 0% | -1% | 0.74 (Caps #1,4)  0.45 (Caps #2,5)  0.68 (Caps #3,6) | 0.37 (Caps #1,4)  0.38 (Caps #2,5)  0.38 (Caps #3,6) | balanced |
| #5 | +5% | 0% | -5% | +5% | 0% | -5% | 0.60 (Caps #1,4)  0.32 (Caps #2,5)  0.39 (Caps #3,6) | 0.58 (Caps #1,4)  0.49 (Caps #2,5)  0.63 (Caps #3,6) | balanced |
| #6 | +10% | 0% | -10% | +10% | 0% | -10% | 0.66 (Caps #1,4)  0.51 (Caps #2,5)  0.64 (Caps #3,6) | 0.66 (Caps #1,4)  0.59 (Caps #2,5)  0.63 (Caps #3,6) | balanced |

Notes: Switching frequency = 20kHz:

DC link capacitors have no shunt resistors;

Module DC link voltages for all cases are balanced at 333V;

Current references:

**TABLE III:**Summary of Parameter Sensitivity Study Results for 6 Modules

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **(kHz)** | **(kΩ)** | **Cap. tolerance Δ*C* (%)** | **Active voltage balance** |  | **Average torque (per unit)** |  | **Transient after**  **step change/current ripple** |
|  |  |  |  | **0~0.3s** | **0.3s~1.0s** | **0~0.3s** | **0.3s~1.0s** |  |
| #1 | 20 | 100 | 400μF  0%, 0%, 0%  0%, 0%, 0% | balanced ( | balanced | 0.50 p.u. | 1.00 p.u. | **transient time:** 0.02s |
| #2 | 20 | w/o | 400μF  0%, 0%, 0%  0%, 0%, 0% | balanced ( | balanced ( | 0.50 p.u. | 1.00 p.u. | **transient time:** 0.02s |
| #3 | 20 | 100 | 400μF  +1%, 0%, -1%,  +1%, 0%, -1%. | balanced, :  0.69 (Caps #1,4)  0.49 (Caps #2,5)  0.47 (Caps #3,6) | balanced, :  0.37 (Caps #1,4)  0.36 (Caps #2,5)  0.32 (Caps #3,6) | 0.49 p.u. | 0.99 p.u. | **transient time:** 0.03s |
| #4 | 20 | w/o | 400μF  +1%, 0%, -1%,  +1%, 0%, -1%. | balanced, :  0.74 (Caps #1,4)  0.45 (Caps #2,5)  0.68 (Caps #3,6) | balanced, :  0.37 (Caps #1,4)  0.38 (Caps #2,5)  0.38 (Caps #3,6) | 0.49 p.u. | 0.98 p.u. | **transient time:** 0.06s  **0~0.3s:**  **0.3s~1.0s:** |
| #5 | 18 | w/o | 400μF  +1%, 0%, -1%,  +1%, 0%, -1%. | balanced, :  0.64 (Caps #1,4)  0.74 (Caps #2,5)  0.73 (Caps #3,6) | balanced, :  0.52 (Caps #1,4)  0.47 (Caps #2,5)  0.49 (Caps #3,6) | 0.49 p.u. | 0.95 p.u. | **transient time:** 0.13s  **0~0.3s:**  **0.3s~1.0s:** =410A, =353A |
| #6 | 18 | w/o | 400μF  +10%, 0%, -10%,  +10%, 0%, -10%. | balanced, :  0.62 (Caps #1,4)  0.66 (Caps #2,5)  0.92 (Caps #3,6) | balanced, :  0.55 (Caps #1,4)  0.60 (Caps #2,5)  0.65 (Caps #3,6) | 0.49 p.u. | 0.95 p.u. | **transient time:** 0.23s  **0~0.3s:**  **0.3s~1.0s:** |

Notes: : switching frequency; : capacitor shunt resistance; ΔC: percentage capacitance tolerances; : DC link peak-to-peak voltage ripple.

Current references:

First, the impact of capacitor tolerances is explored. TABLE II summarizes the key characteristics of 6 selected cases with different combinations of capacitance tolerances up to ±10%. The PWM switching frequency is fixed at 20 kHz while the DC-link voltages are balanced in all 6 cases. The definition of Δ*Udc* and the value of the current step changes are specified in the figure below TABLE II.

In Cases #1 and #2, only 1 out of the 6 capacitors has higher capacitance. When the capacitance tolerance increases from 1% to 5%, Δ*Udc* slightly increases. Capacitor #1 (1% higher capacitance: 404 uF) has modestly higher voltage ripple compared to Capacitors #2~#6 (with 0% capacitance tolerance). Also, the voltage ripple is lower at full load (1 MW, 0.3~1.0s) compared to partial load (500 kW, 0~0.3s) because the phase current ripple at full load is lower than at partial load.

In Case #3, 3 capacitors have 5% higher capacitances (420 uF) while the other 3 capacitors have 0% tolerances. In this case, the voltage ripple is nearly equal for all capacitors.

[Fig. 7. - 
Three drive units with series-connected DC link capacitors
](https://ieeexplore.ieee.org/mediastore_new/IEEE/content/media/9235288/9235325/9236275/wu7-p8-wu-large.gif)

**Fig. 7.** Three drive units with series-connected DC link capacitors

[Fig. 8. - 
Terminal voltage of capacitors and current waveforms (800 μF capacitor, 100 kΩ shunt resistors, no capacitor tolerances).
](https://ieeexplore.ieee.org/mediastore_new/IEEE/content/media/9235288/9235325/9236275/wu8-p8-wu-large.gif)

**Fig. 8.** Terminal voltage of capacitors and current waveforms (800 μF capacitor, 100 kΩ shunt resistors, no capacitor tolerances).

In Cases #4~#6, a mixture of positive, negative and zero tolerances is adopted. Similar to Case #3, all units have the same voltage ripple amplitude. As the tolerance increases from ±1% to ±10%, the impact on voltage ripple is negligible. The difference of DC link current ripple amplitude among Cases #1~#6 is very little.

TABLE III summarizes the results of a sensitivity analysis carried out for several parameters including switching frequency (*fpwm*), capacitor shunt resistors (*Rparallel*), and capacitor tolerances (Δ*C*). Key insights are summarized below:

* Comparing Cases #1 and #2, capacitor shunt resistors are not required for the active DC-link capacitor voltage balancing control. When capacitance differences occurs, parallel resistors can help balance the DC link voltage, so that the transient time will be slightly shortened compared to the case without shunt resistors (Case #3 vs. Case #4).
* Cases #3 and #4 also show that capacitor tolerances could result in DC bus voltage fluctuation, 1~2% lower output power, as well as dynamic performance degradation.
* The PWM switching frequency is gradually reduced to explore its impact on the stability of the system. Case #5 shows that, at lower switching frequency (18 kHz), the major penalty is significantly higher *d*-axis and *q*-axis current ripple while the impact on voltage balancing and voltage ripple is low.
* Case #6 shows that both the voltage ripple and transient time period after the step change increase when the capacitor tolerances are higher. In addition, the winding current ripple as well as the torque ripple increase as well.

# SECTION IV. Design With Reduced Drive Unit Count

The 18-slot/12-pole machine can also be reconfigured as 3 segments/drive units as shown in Fig. 7. Each consists of 6 adjacent stator teeth/coils. One benefit of using fewer drive units is hardware simplification, but the DC link voltage rises to 667 V for each drive unit. For each of the three modules, the PM flux linkage, *Ld*, *Lq*, and winding resistance values are doubled compared to the 6 module case. The DC link capacitance should be doubled as well to keep the current ripple at the same level with respect to the design with 6 drive units.

The PI gains of the voltage loop are re-tuned to minimize voltage ripple (see Appendix, TABLE AII). The optimal P gain is inversely proportional to the capacitance of the DC link capacitors, which means that longer charging time is required for higher capacitance values. In addition, simulation results show that the integral gain can trigger system instability under some conditions, so *KbV* was set to be 0. Based on the simulation results, an empirical formula for the proportional gain has been developed as

(1)

where *KaV* is the proportional gain; *C* is the DC link capacitance.

Fig. 8 shows the simulation results with 3 drive units. Again, the *q*-axis current reference is stepped from from 404 A to 808 A at 0.3 s to observe the dynamic response. The Fig. 8 waveforms show that active voltage balancing, as well as current, torque and power targets are achieved when all capacitors are equal. The *d*- and *q*-axis current ripple in Fig. 8(b) are comparable to those in Fig. 6(b) with 6 drive units.

**TABLE IV:**Summary of Parameter Sensitivity Study Results for 3 Module Case

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | ***fpwm* (kHz)** | ***Rparallel***  **(kΩ)** | **Cap. tolerance Δ*C* (%)** | **Active voltage balance** |  | **Current Ripple (A)** |  | **Transient after**  **step change** |
|  |  |  |  | **0~0.3s** | **0.3s~1.0s** | **0~0.3s** | **0.3s~1.0s** |  |
| #1 | 20 | 100 | 400 μF each  0%, 0%, 0% | balanced (negligible ripple, **ΔUdc**:< 0.01V) |  | Δid: 504  Δiq: 509 | Δid: 316  Δiq: 330 | 0.03s |
| #2 | 20 | -- | 400 μF each  0%, 0%, 0% | balanced (negligible ripple, **ΔUdc**:< 0.01V) |  | Δid: 505  Δiq: 510 | Δid: 316  Δiq: 330 | 0.04s |
| #3 | 20 | 100 | 400 μF each  +1%, 0%, -1% | balanced (**Δ**: 1.2V) | balanced (**Δ**: 0.87V) | Δid: 508  Δiq: 511 | Δid: 320  Δiq: 331 | 0.03s |
| #4 | 20 | -- | 800 μF each  +1%, 0%, -1% | balanced (**Δ**: 0.95V) | balanced (**Δ**: 0.44V) | Δid: 506  Δiq: 499 | Δid: 317  Δiq: 336 | 0.04s |
| #5 | 20 | -- | 800 μF each  +10%, 0%, -10% | balanced (**Δ**: 1.12V) | balanced (**Δ**: 0.55V) | Δid: 507  Δiq: 507 | Δid: 319  Δiq: 340 | 0.04s |
| #6 | 18 | -- | 800 μF each  +1%, 0%, -1% | balanced (**Δ**: 0.97V) | unbalanced (**Δ**: 0.47V) | Δid: 731  Δiq: 750 | Δid: 355  Δiq: 411 | 0.05s |

**TABLE V:**Impact of Adding 60 HZ Voltage Fluctuation with Amplitude Δ to DC Link Voltage For 3 Module Case

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Drive**  **units** | ***fpwm***  **(kHz)** | **Cap. tolerance**  **Δ*C* (%)** | ***Rparallel***  **(kΩ)** | **DC link**  **voltage** | **Active voltage balance** |  | **Steady torque (per unit)** |  | **Transient after**  **step change** |
|  |  |  |  |  | **0~0.3s** | **0.3s~1.5s** | **0~0.3s** | **0.3s~1.5s** |  |
| 3 | 20 | 800 μF each  +1%, 0%, -1% | w/o | 2000 Vdc  **Δ**: 0.5%, 60Hz | balanced (**Δ**: 7.17V) | balanced (**Δ**: 6.87V) | Δid: 511  Δiq: 516 | Δid: 320  Δiq: 348 | 0.03s |
| 3 | 20 | 800 μF each  +10%, 0%, -10% | w/o | 2000 Vdc  **Δ**: 0.5%, 60Hz | balanced (**Δ**: 7.53V) | balanced (**Δ**: 7.27V) | Δid: 512  Δiq: 517 | Δid: 320  Δiq: 350 | 0.04s |
| 3 | 30 | 800 μF each  +10%, 0%, -10% | w/o | 2000 Vdc  **Δ**: 0.5%, 60Hz | balanced (**Δ**: 7.38V) | balanced (**Δ**: 7.10V) | Δid: 99  Δiq: 104 | Δid: 98  Δiq: 135 | 0.02s |
| 6 | 20 | 400 μF each  +1%, 0%, -1%  +1%, 0%, -1% | w/o | 2000 Vdc  **Δ**: 0.5% 60Hz | balanced (**Δ**: 3.64V) | balanced (**Δ**: 3.39V) | Δid: 500  Δiq: 518 | Δid: 310  Δiq: 335 | 0.03s |
| 6 | 20 | 400 μF each  +10%, 0%, -10%  +10%, 0%, -10% | w/o | 2000 Vdc  **Δ**: 0.5% 60Hz | balanced (**Δ**: 3.98V) | balanced (**Δ**: 3.57V) | Δid: 501  Δiq: 519 | Δid: 310  Δiq: 337 | 0.04s |
| 6 | 30 | 400 μF each  +10%, 0%, -10%  +10%, 0%, -10% | w/o | 2000 Vdc  **Δ**: 0.5% 60Hz | balanced (**Δ**: 3.69V) | balanced (**Δ**: 3.42V) | Δid: 96  Δiq: 98 | Δid: 95  Δiq: 132 | 0.02s |

TABLE IV summarizes the sensitivity analysis for switching frequency, shunt resistors, and capacitance tolerances. Key observations are summarized as follows:

* Compared to 6 drive units, 3 drive units can significantly reduce the complexity of hardware design, manufacturing, and signal synchronization. However, in comparison to the results shown in TABLE III (6 drive units), TABLE IV (3 drive units) shows that the DC link voltage ripple and current ripple are relatively higher in amplitudfge.
* With fewer drive units, the voltage rating of each drive unit is higher. Thus, lower PWM switching frequency may be required, which could make the active voltage balancing control more difficult.

The impact of adding a low-frequency (60Hz) AC voltage fluctuation with amplitude D=0.5% to the total DC-link voltage (2000 Vdc) has been investigated with results presented in TABLE V. Six cases are compared. Each one has a different combination of drive units (3 or 6), capacitance tolerances (up to 10%) and PWM switching frequency (20 or 30 kHz). It can be concluded from TABLE V that all six designs can withstand this 0.5% AC voltage ripple added to the DC link voltage at 60 Hz. The amplitude of the module DC link voltage ripple Δ*Udc* as a percentage of the nominal module DC link voltage is changed very little for the 3-module and 6-module cases.

Ultimately, the choice of the number of modules is a multifaceted system decision that involves a significant number of tradeoffs between important drive system metrics including power density, control complexity, component count, fault tolerance, and failure rates. These tradeoffs extend well beyond the scope of this investigation.

# SECTION V. More General Approach

Since a surface-mounted PM (SPM) machine was selected for this investigation in which the *q*-axis current alone controls the torque production, adding the voltage PI control loop to manipulate the *q*-axis current command is sufficient to achieve the desired active voltage balancing. However, a more general approach that addresses both SPM and IPM machines is to implement voltage balancing control for both the *d*- and *q*-axes.

In Fig. 9, both the *d*- and *q*-axis current references are scaled by the same ratio. Fig. 10 shows examples of simulation results comparing the predicted performance of this more general approach manipulating both *id* and *iq* with the previous approach manipulating only *iq*. It is assumed that there are 3 modules, and the capacitance tolerances of the 800μF DC link capacitors are +10%, 0%, -10%, respectively. The SPM machine is operating at 20,000 r/min and the switching frequency is 20 kHz. In order to balance the DC link voltage while minimizing the DC link voltage ripple, the PI gains are re-tuned for the new approach (KaV=1.2, KbV=0) as indicated in the Fig. 10(a) heading.

[Fig. 9. - 
Active voltage balance achieved by adjusting d- and q-axis current references with DC-link voltage feedback.
](https://ieeexplore.ieee.org/mediastore_new/IEEE/content/media/9235288/9235325/9236275/wu9-p8-wu-large.gif)

**Fig. 9.** Active voltage balance achieved by adjusting *d*- and *q*-axis current references with DC-link voltage feedback.

[Fig. 10. - 
DC link voltage profile with active voltage balance control (capacitance tolerances: +10%, 0%, -10%) Current references: id = -113.5A, iq = 404A (0~0.3s); id = -113.5, iq = 808A (0.3~1.5s).
](https://ieeexplore.ieee.org/mediastore_new/IEEE/content/media/9235288/9235325/9236275/wu10-p8-wu-large.gif)

**Fig. 10.** DC link voltage profile with active voltage balance control (capacitance tolerances: +10%, 0%, -10%) Current references: *id* = -113.5A, *iq* = 404A (0~0.3s); *id* = -113.5, *iq* = 808A (0.3~1.5s).

In comparison to only manipulating the *q*-axis current reference, adding the voltage control loop for both the *d*- and *q-*axis currents reduces the DC link voltage ripple because of the flux weakening effect of the negative *d-*axis current. Although the amplitude of the voltage ripple reduction is minor for full-load conditions, the effect is more apparent for partial loads (0~0.3s: ~500kW, *id* = -113.5A, *iq* = 404A) where the voltage ripple is reduced by 22%~36%.

# SECTION VI. Conclusions

This paper discusses active DC link capacitor voltage balancing control for a 1 MW IMMD intended for aerospace applications. Key findings are summarized as follows:

* The feasibility of active voltage balancing using voltage closed-loop control has been confirmed for this application. Other than the voltage sensor needed for each DC-link capacitor, this technique does not require the addition of either capacitor shunt resistors or dedicated voltage balancing circuits separate from the machine controls.
* The robustness of the control model has been investigated with consideration of practical implementation issues including variations of switching frequency, capacitance tolerances, shunt resistor values, and DC-link voltage fluctuations. The high *d*-axis and *q*-axis current ripple resulting from low inductance and low switching frequency have little impact on the performance of the active voltage balancing control.
* The active voltage balancing control reduces the voltage stress on the IMMD power modules and machine windings by minimizing any large voltage excursions. This is beneficial for reducing the risk of PD damage to both the winding insulation and module power electronics.
* The investigation results identified some modest voltage balancing performance benefits associated with increasing the number of series-connected drive modules, but they were not large enough to suggest that they would be a major factor in choosing the "optimum" IMMD module number for a particular application.

# Appendix

Fig. A1 shows the modeling of active balancing voltage loop in each individual drive unit.

[Fig. A1. - 
Model of active balancing voltage loop
](https://ieeexplore.ieee.org/mediastore_new/IEEE/content/media/9235288/9235325/9236275/wuA1-p8-wu-large.gif)

**Fig. A1.** Model of active balancing voltage loop

TABLE AI summarizes the impact of the PI gains of the voltage loop on voltage ripple, current ripple, and system stability. In order to have low DC link voltage ripple, low current ripple, and good system stability, (KaV=3, KbV=0) is used in the simulation.

**TABLE A I:**Tuning of PI Gains in Voltage Loop (6 Drive Units)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **KaV, KbV** | **ΔUdc (V)** |  | **Current Ripple (A)** |  | **Voltage Balance** |
|  | **0s~0.3s** | **>0.3s** | **0s~0.3s** | **>0.3s** |  |
| 5, 0 | 114.8 (Cap #1)  25.5 (Caps#2~6) | 60.0 (Cap #1)  12.1 (Cap#2~6) | id: 1010  iq: 689 | id: 572  iq: 425 | balanced 0~1.5s |
| 4, 0 | 1.57 (Cap #1)  0.32 (Caps#2~6) | 0.96 (Cap #1)  0.61 (Caps#2~6) | id: 501  iq: 510 | id: 319  iq: 333 | balanced 0~1.5s |
| 3, 0 | 0.91 (Cap #1)  0.18 (Caps#2~6) | 0.46 (Cap #1)  0.45 (Caps#2~6) | id: 499  iq: 508 | id: 313  iq: 334 | balanced 0~1.5s |
| 2, 0 | 0.89 (Cap #1)  0.18 (Caps#2~6) | 0.58 (Cap #1)  0.55 (Caps#2~6) | id: 507  iq: 504 | id: 320  iq: 334 | balanced 0~1.5s |
| 1, 0 | 0.71 (Cap #1)  0.14 (Caps#2~6) | 0.64 (Cap #1)  0.13 (Caps#2~6) | id: 493  iq: 505 | id: 314  iq: 332 | unbalanced at 0.94s |

*Note:* Capacitance tolerances: Cap#1: +1%; Caps#2~#6: 0 %.

Similarly, TABLE AII summarizes the PI gain tuning for the design with three drive units. Based on the results, (KaV=1.5, KbV=0) is adopted.

**TABLE A II:**Tuning of PI Gains in Voltage Loop (3 Drive Units)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **KaV, KbV** | **ΔUdc (V)** |  | **Current Ripple (A)** |  | **Voltage Balance** |
|  | **0s~0.3s** | **>0.3s** | **0s~0.3s** | **>0.3s** |  |
| 5, 0 | 40.9 (Cap #1)  20.9 (Caps#2,3) | -- | id: 785  iq: 667 | -- | unbalanced 0.3~1.5s |
| 3, 0 | 1.76 (Cap #1)  0.89 (Caps#2,3) | 0.77 (Cap #1)  0.43 (Caps#2,3) | id: 501  iq: 512 | id: 313  iq: 336 | balanced 0~1.5s |
| 2, 0 | 1.13 (Cap #1)  0.56 (Caps#2,3) | 0.53 (Cap #1)  0.27 (Caps#2,3) | id: 502  iq: 507 | id: 315  iq: 335 | balanced 0~1.5s |
| 1.5, 0 | 0.79 (Cap #1)  0.40 (Caps#2,3) | 0.47 (Cap #1)  0.24 (Caps#2,3) | id: 500  iq: 508 | id: 314  iq: 334 | balanced 0~1.5s |
| 1, 0 | 0.89 (Cap #1)  0.45 (Caps#2,3) | 0.3 (Cap #1)  0.25 (Caps#2,3) | id: 504  iq: 513 | id: 317  iq: 334 | balanced 0~1.5s |
| 0.5, 0 | 0.6 (Cap #1)  0.31 (Caps#2,3) | -- | id: 509  iq: 507 | -- | unbalanced 0.3~1.5s |

*Note:* Capacitance tolerances: Cap #1: +1%; Caps #2, 3: 0 %.

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